

**SMPS MOSFET IRFBC40AS**

HEXFET® Power MOSFET

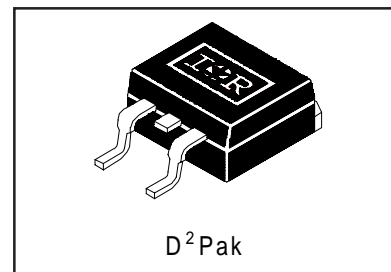
**Applications**

- Switch Mode Power Supply ( SMPS )
- Uninterruptable Power Supply
- High speed power switching

<b>V<sub>DSS</sub></b>	<b>R<sub>ds(on)</sub> max</b>	<b>I<sub>D</sub></b>
<b>600V</b>	<b>1.2Ω</b>	<b>6.2A</b>

**Benefits**

- Low Gate Charge Q<sub>g</sub> results in Simple Drive Requirement
- Improved Gate, Avalanche and dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective Coss Specified ( See AN 1001)



**Absolute Maximum Ratings**

	<b>Parameter</b>	<b>Max.</b>	<b>Units</b>
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>⑥</sup>	6.2	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V <sup>⑥</sup>	3.9	
I <sub>DM</sub>	Pulsed Drain Current <sup>①⑥</sup>	25	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Power Dissipation	125	W
	Linear Derating Factor	1.0	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt <sup>③⑥</sup>	6.0	V/ns
T <sub>J</sub>	Operating Junction and	-55 to + 150	°C
T <sub>STG</sub>	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	

**Typical SMPS Topology:**

- Single transistor Forward

Notes <sup>①</sup> through <sup>⑤</sup> are on page 9

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# IRFBC40AS

International  
IR Rectifier

Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	600	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.66	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$ ⑥
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	1.2	$\Omega$	$V_{GS} = 10V, I_D = 3.7A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	25 250	$\mu A$	$V_{DS} = 600V, V_{GS} = 0V$ $V_{DS} = 480V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

Dynamic @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$g_{fs}$	Forward Transconductance	3.4	—	—	S	$V_{DS} = 50V, I_D = 3.7A$
$Q_g$	Total Gate Charge	—	—	42	nC	$I_D = 6.2A$ $V_{DS} = 480V$ $V_{GS} = 10V$ , See Fig. 6 and 13 ④
$Q_{gs}$	Gate-to-Source Charge	—	—	10		
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	20		
$t_{d(on)}$	Turn-On Delay Time	—	13	—		
$t_r$	Rise Time	—	23	—	ns	$V_{DD} = 300V$ $I_D = 6.2A$ $R_G = 9.1\Omega$ $R_D = 47\Omega$ , See Fig. 10 ④
$t_{d(off)}$	Turn-Off Delay Time	—	31	—		
$t_f$	Fall Time	—	18	—		
$C_{iss}$	Input Capacitance	—	1036	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0\text{MHz}$ , See Fig. 5
$C_{oss}$	Output Capacitance	—	136	—		
$C_{riss}$	Reverse Transfer Capacitance	—	7.0	—		
$C_{oss}$	Output Capacitance	—	1487	—		
$C_{oss}$	Output Capacitance	—	36	—		
$C_{oss}$	Output Capacitance	—	—	—		
$C_{oss\ eff.}$	Effective Output Capacitance	—	48	—		

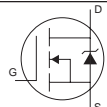
## Avalanche Characteristics

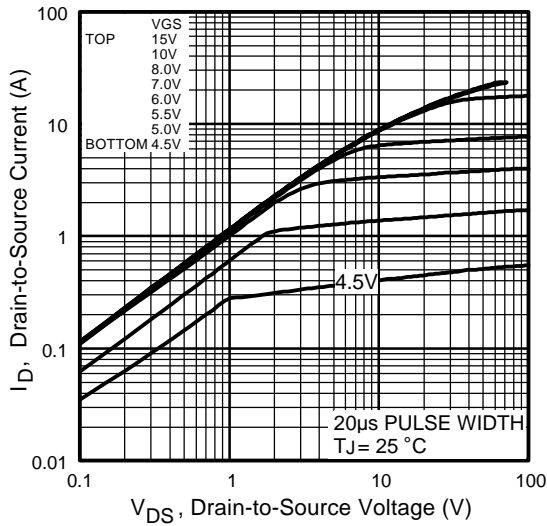
	Parameter	Typ.	Max.	Units
$E_{AS}$	Single Pulse Avalanche Energy ②	—	570	mJ
$I_{AR}$	Avalanche Current ①	—	6.2	A
$E_{AR}$	Repetitive Avalanche Energy ①	—	13	mJ

## Thermal Resistance

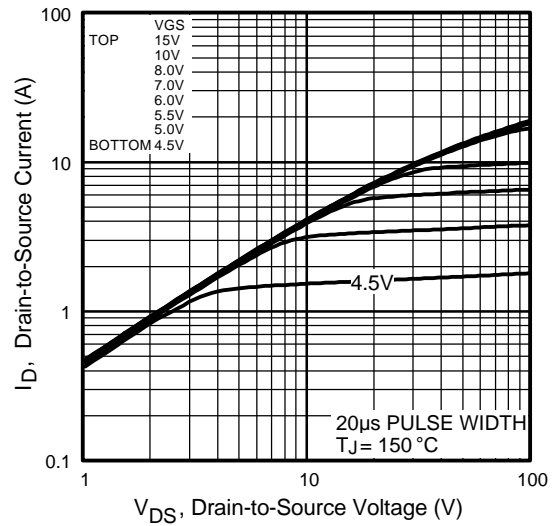
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.0	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted, steady-state)*	—	40	

## Diode Characteristics

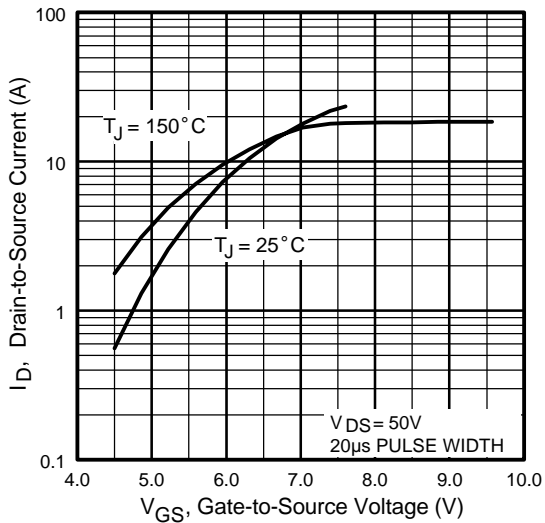
	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	6.2	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	25		
$V_{SD}$	Diode Forward Voltage	—	—	1.5	V	$T_J = 25^\circ\text{C}, I_S = 6.2A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	431	647	ns	$T_J = 25^\circ\text{C}, I_F = 6.2A$
$Q_{rr}$	Reverse Recovery Charge	—	1.8	2.8	$\mu C$	$di/dt = 100A/\mu s$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$ )				



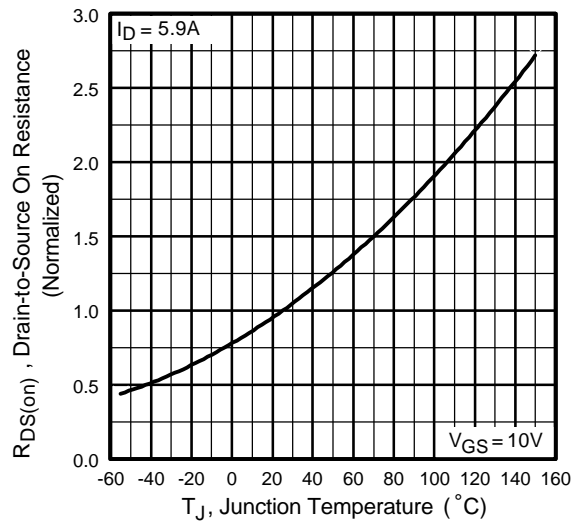
**Fig 1.** Typical Output Characteristics,



**Fig 2.** Typical Output Characteristics,

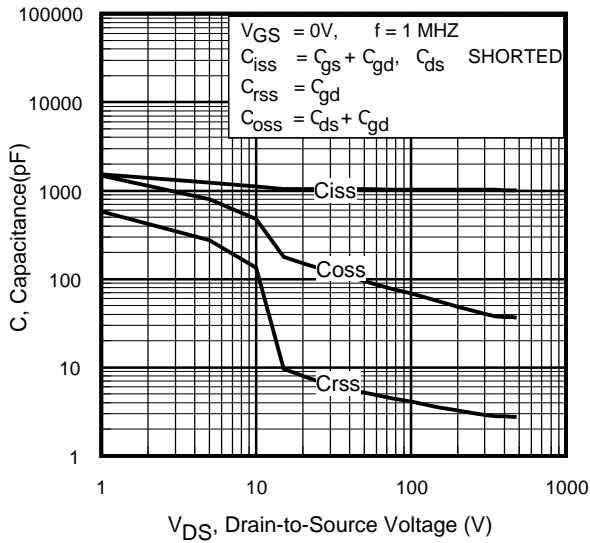


**Fig 3.** Typical Transfer Characteristics

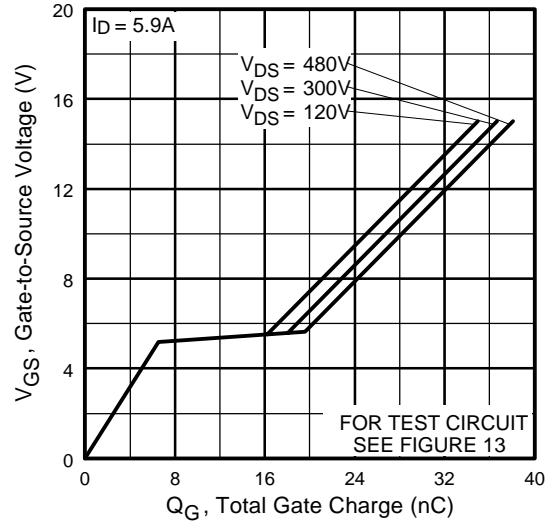


**Fig 4.** Normalized On-Resistance  
Vs. Temperature

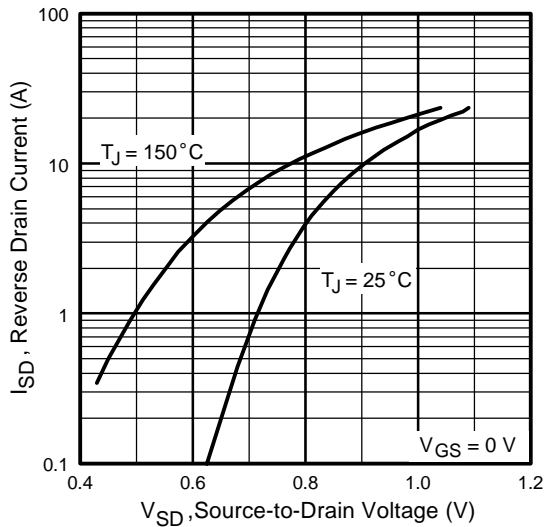
# IRFBC40AS



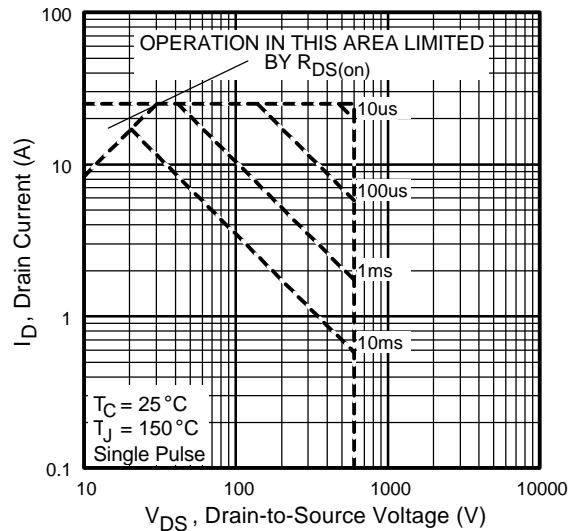
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



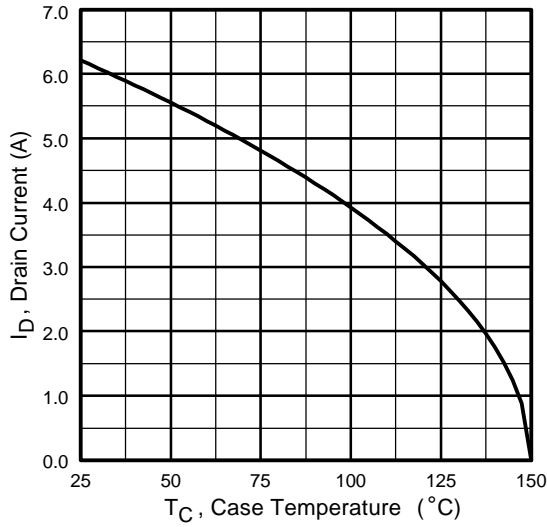
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



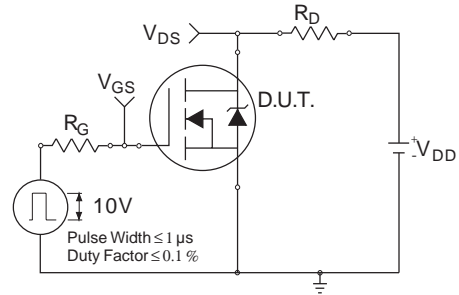
**Fig 7.** Typical Source-Drain Diode Forward Voltage



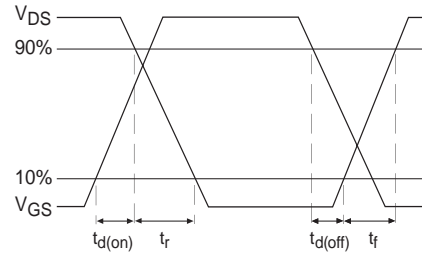
**Fig 8.** Maximum Safe Operating Area



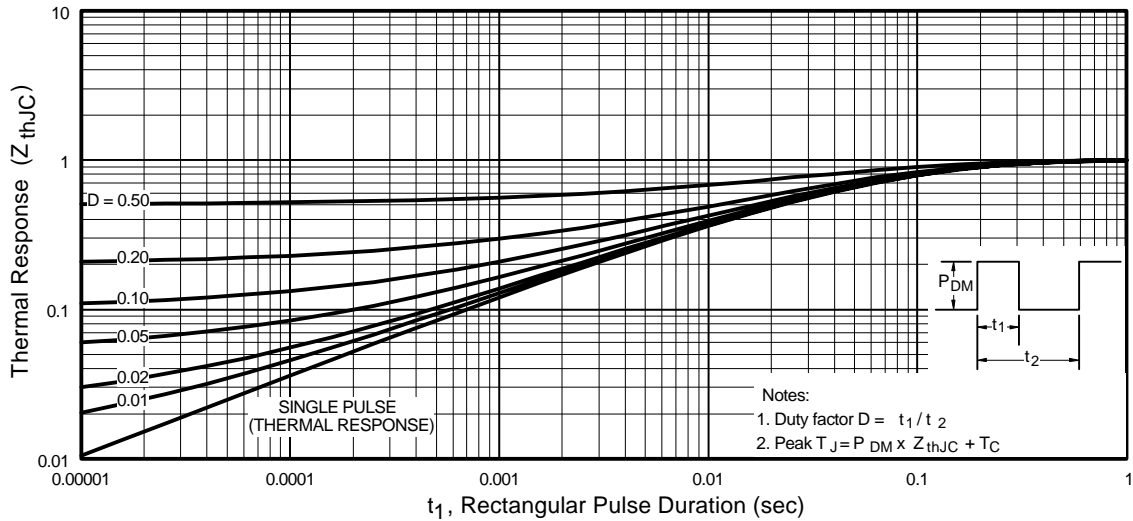
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit



**Fig 10b.** Switching Time Waveforms



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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**Fig 12a.** Unclamped Inductive Test Circuit



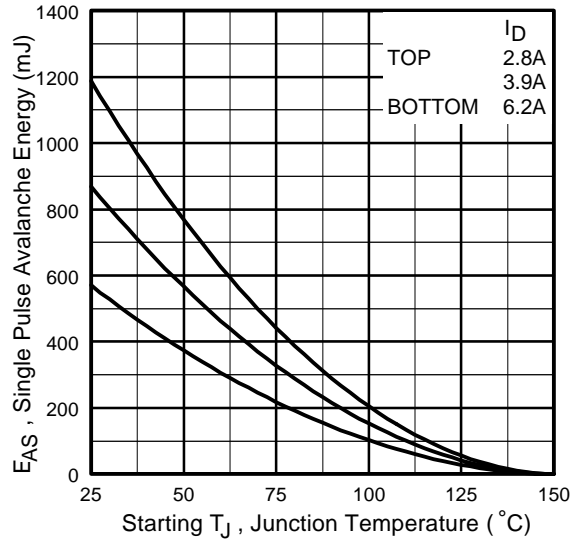
**Fig 12b.** Unclamped Inductive Waveforms



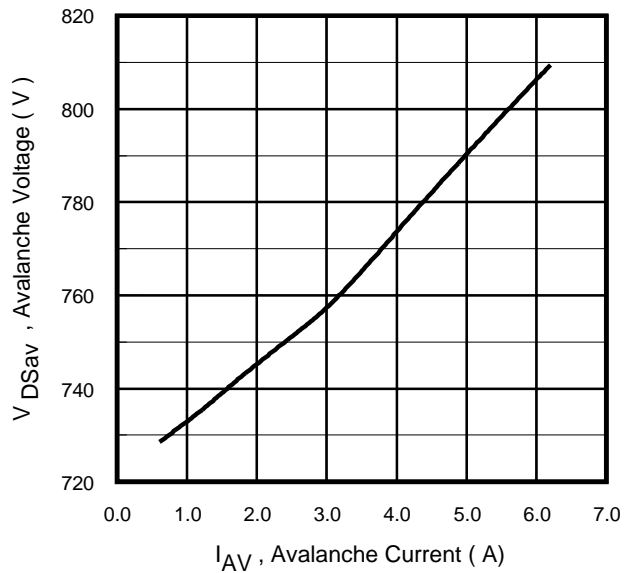
**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 12d.** Typical Drain-to-Source Voltage Vs. Avalanche Current

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## Peak Diode Recovery dv/dt Test Circuit



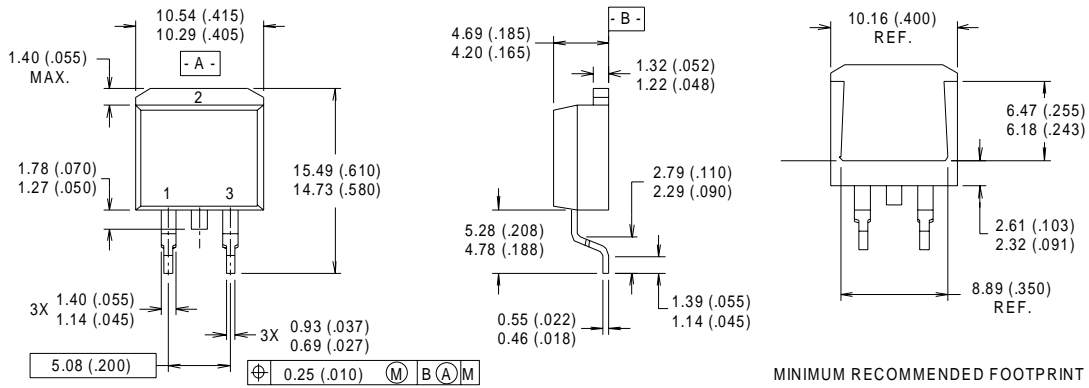
\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 14.** For N-Channel HEXFETS

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## D<sup>2</sup>Pak Package Outline



**NOTES:**

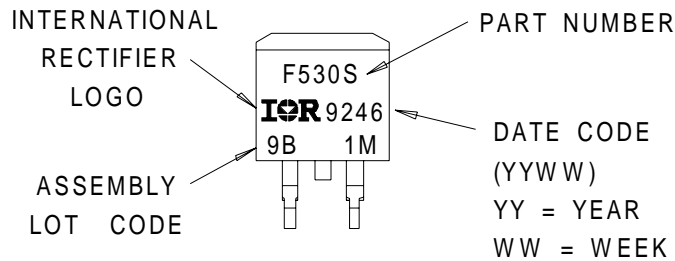
- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

**LEAD ASSIGNMENTS**

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

## Part Marking Information

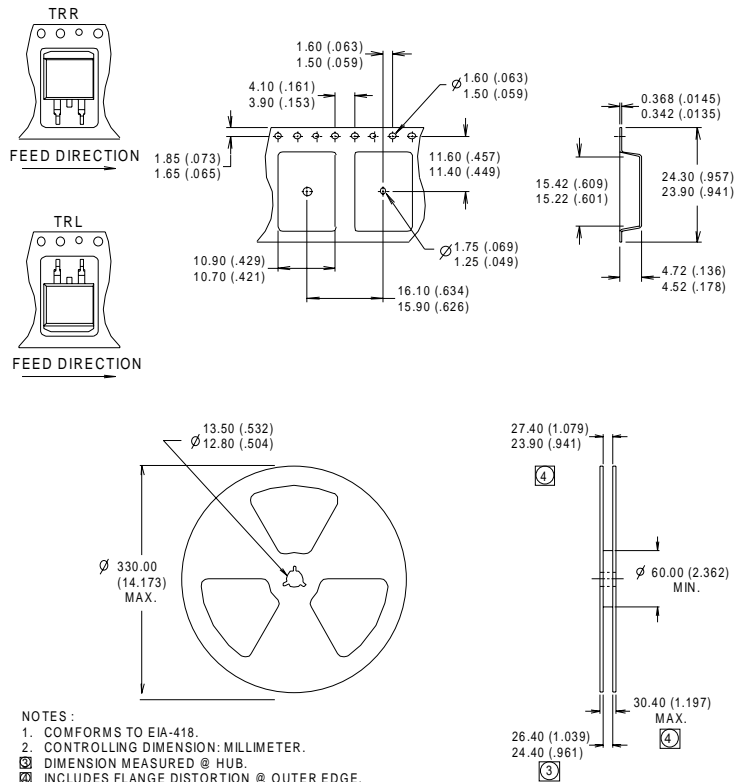
### D<sup>2</sup>Pak





## Tape & Reel Information

### D<sup>2</sup>Pak



### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 29.6\text{mH}$   
 $R_G = 25\Omega$ ,  $I_{AS} = 6.2\text{A}$ . (See Figure 12)
- ③  $I_{SD} \leq 6.2\text{A}$ ,  $di/dt \leq 88\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  
 $T_J \leq 150^\circ\text{C}$
- ④ Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{oss}$  eff. is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$
- ⑥ Uses IRFBC40A data and test conditions

\* When mounted on FR-4 board using minimum recommended footprint.  
For recommended footprint and soldering techniques refer to application note #AN-994.