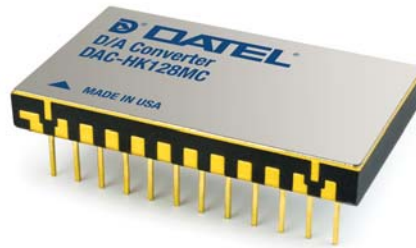


FEATURES

- 12-Bit resolution
- Integral nonlinearity error $\pm 1/2$ LSB, max.
- Differential nonlinearity error $\pm 3/4$ LSB, max.
- MIL-STD-883 high-reliability versions available
- Input register
- 3 μ s fast settling time
- Guaranteed monotonicity over full temperature range



PRODUCT OVERVIEW

The DAC-HK Series hybrid D/A converters are highperformance 12-bit devices with a fast settling voltage output. They incorporate a level-controlled input storage register and are specifically designed for systems applications such as data bus interfacing with computers. When the "load" input is high, data in the storage register is held, and when the load input is low, data is transferred through to the DAC. There are two basic models available by coding option: binary and two's complement. The output voltage ranges are externally pinprogrammable and include: 0 to +5V, 0 to +10V, ± 2.5 V, ± 5 V and ± 10 V.

The DAC-HK Series contains a precision zener reference circuit. This eliminates code-dependent ground currents by routing current from the positive supply to the internal ground node as determined by the R-2R ladder network. The internal feedback resistors for the on-board amplifier track the ladder network resistors, enhancing temperature performance. The excellent tracking of the resistors results in a differential nonlinearity tempco of ± 2 ppm/ $^{\circ}$ C maximum. The temperature coefficient of gain is ± 20 ppm/ $^{\circ}$ C maximum, and the tempco of zero is ± 5 ppm/ $^{\circ}$ C maximum.

| INPUT/OUTPUT CONNECTIONS | | | |
|--------------------------|--------------|-----|------------------|
| PIN | FUNCTION | PIN | FUNCTION |
| 1 | BIT 1 (MSB) | 24 | REFERENCE OUT |
| 2 | BIT 2 | 23 | GAIN ADJUST |
| 3 | BIT 3 | 22 | +15V SUPPLY |
| 4 | BIT 4 | 21 | GROUND |
| 5 | BIT 5 | 20 | SUMMING JUNCTION |
| 6 | BIT 6 | 19 | 20V RANGE |
| 7 | BIT 7 | 18 | 10V RANGE |
| 8 | BIT 8 | 17 | BIPOLAR OFFSET |
| 9 | BIT 9 | 16 | LOAD |
| 10 | BIT 10 | 15 | VOLTAGE OUTPUT |
| 11 | BIT 11 | 14 | -15V SUPPLY |
| 12 | BIT 12 (LSB) | 13 | +5V SUPPLY |

BLOCK DIAGRAM

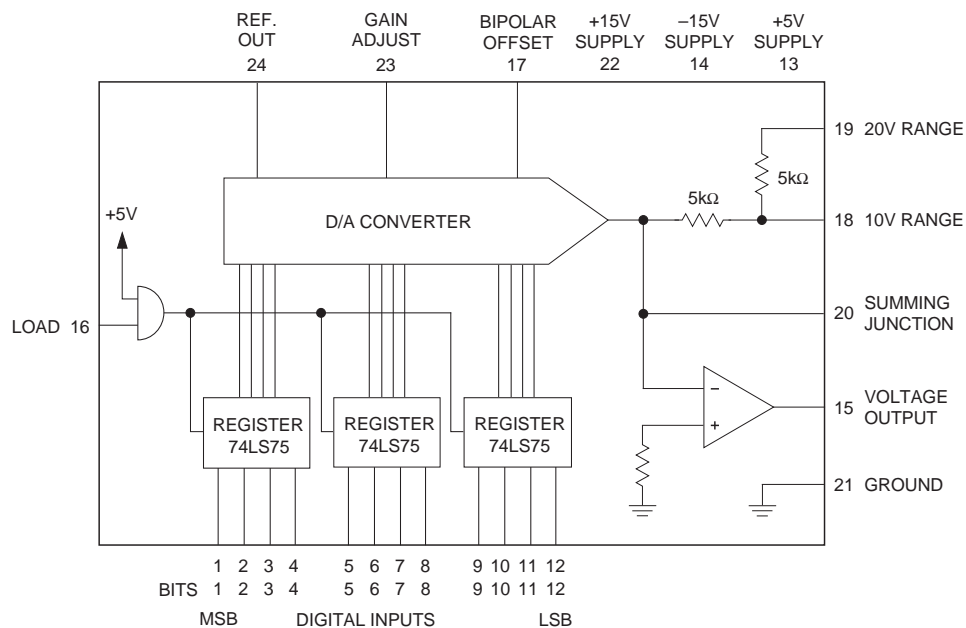


Figure 1. DAC-HK Functional Block Diagram

FUNCTIONAL SPECIFICATIONS

(Typical at +25°C and ±15V and +5V supplies unless otherwise noted.)

| DESCRIPTION | |
|---------------------------------------|---|
| INPUTS | |
| Resolution | 12 bits |
| Coding, Unipolar Output | Straight binary |
| Coding, Bipolar Output | Offset binary, two's complement ① |
| Input Logic Level, Bit ON ("1") | +2.0V to +5.5V |
| Input Logic Level, Bit OFF ("0") | 0V to +0.8V |
| Logic Loading | 1 LSTTL load |
| Load Input ② | High ("1") = hold data Low ("0") = transfer data |
| Load Input Loading | 3 LSTTL loads |
| PERFORMANCE ④ | |
| Nonlinearity Error, max. | ±1/2LSB |
| Differential Nonlinearity Error, max. | ±3/4LSB |
| Gain Error, Before Trimming | ±0.1% ③ |
| Zero Error, Before Trimming | ±0.1% of FSR ③ |
| Gain Tempco, max. | ±20ppm/°C |
| Zero Tempco, Unipolar, max. | ±5ppm/°C of FSR |
| Offset Tempco, Bipolar, max. | ±10ppm/°C of FSR |
| Diff. Nonlinearity Tempco, max. | ±2ppm/°C of FSR |
| Monotonicity | Guaranteed over temperature |
| Settling Time, 5V Change | 3µs |
| Settling Time, 10V Change | 3µs |
| Settling Time, 20V Change | 4µs |
| Settling Time, 1LSB Change | 800ns |
| Slew Rate | ±20V/µs |
| Power Supply Rejection | ±0.002%FSR/% |
| OUTPUTS | |
| Output Voltage Ranges, Unipolar ⑤ | 0 to +5V, 0 to +10V |
| Output Voltage Ranges, Bipolar ⑤ | ±2.5V ±5V ±10V |
| Output Current | ±5mA min. |
| Output Impedance | 0.05Ω |
| POWER REQUIREMENTS | |
| Power Supply Voltages ⑥ | +15V, ±0.5V at 15mA -15V, ±0.5V at 30mA +5V, ±0.25V at 65mA |
| PHYSICAL/ENVIRONMENTAL | |
| Operating Temperature Range, Case | 0°C to +70°C (BGC/BGC-C, BMC,BMC-C) -40°C to +85°C (BME, BME-C) -55°C to +125°C (BMM, BMM-C, 883,-C/883) |
| Storage Temperature Range | -65°C to +125°C |
| Package Type | 24-pin DDIP |
| Weight | 0.22 ounces (6.3 grams) |

Footnotes:

- ① For two's complement coding, order the "-2" model as described in Ordering Information.
- ② Logic levels are the same as for data inputs.
- ③ Initial errors are trimmable to zero. See Connection Diagram.
- ④ FSR is full scale range and is 10V for 0 to +10V output range, 20V for ±10V output range, etc.
- ⑤ By external pin connection.
- ⑥ For ±12V, +5V operation, contact factory.

ABSOLUTE MAXIMUM RATINGS

| PARAMETERS | LIMITS | UNITS |
|---------------------------------------|--------|-------|
| Positive Supply, Pin 22 | +18 | Volts |
| Negative Supply, Pin 14 | -18 | Volts |
| Logic Supply, Pin 13 | +5.25 | Volts |
| Digital Input Voltage, Pins 1-12 & 16 | +5.5 | Volts |
| Output Current, Pin 15 | ±20 | mA |
| Lead Temperature (soldering, 10s) | 300 | °C |

TECHNICAL NOTES

1. It is recommended that these converters be operated with local supply bypass capacitors of 1µF (tantalum type) at the +15V, -15V and +5V supply pins. The capacitors should be connected as close to the pins as possible. In high RFI noise environments, these capacitors should be shunted with 0.01µF ceramic capacitors.
2. The analog, digital and power grounds should be separated from each other as close as possible to pin 21 where they all must come together.
3. The "load" control pin is a level-triggered input which causes the register to hold data with a high input and transfer data to the DAC with a low input.
4. A setup time of 50ns minimum must be allowed for the input data. The DAC output voltage begins to change when the register output changes.
5. If the reference output terminal (pin 24) is used, an operational amplifier in non-inverting mode should be used as a buffer. Current drawn from pin 24 should be limited to ±10µA in order not to affect the T.C. of the reference.

CALIBRATION PROCEDURE

Select the desired output voltage range and connect the converter as shown in the Output Range Selection Table and the Connection Diagrams. Refer to the Coding Tables.

Unipolar Operation

1. **Zero Adjustment.** Set the input digital code to 0000 0000 0000 and adjust the ZERO ADJ. potentiometer to give 0.0000V output.
2. **Gain Adjustment.** Set the input digital code to 1111 1111 1111 (straight binary) and adjust the GAIN ADJ. potentiometer to give the full-scale output voltage shown in Table 1.

Bipolar Operation

1. **Offset Adjustment.** Set the digital input code to 0000 0000 0000 (offset binary) or 1000 0000 0000 (two's complement) and adjust the OFFSET ADJ. potentiometer to give the negative full-scale output voltage shown in Table 2.
2. **Gain Adjustment.** Set the digital input code to 1111 1111 1111 (offset binary) or 0111 1111 1111 (two's complement) and adjust the GAIN ADJ. potentiometer to give the positive full-scale output voltage shown in Table 2.

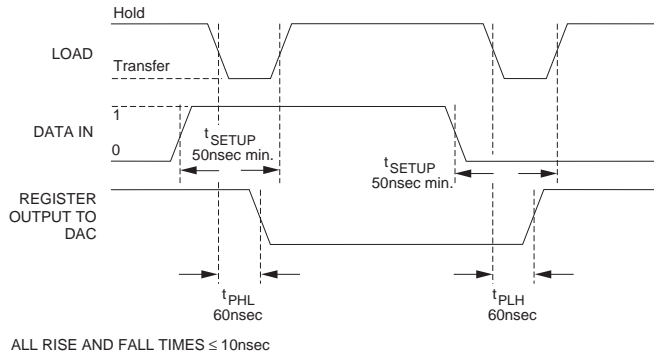


Figure 2. DAC-HK Timing

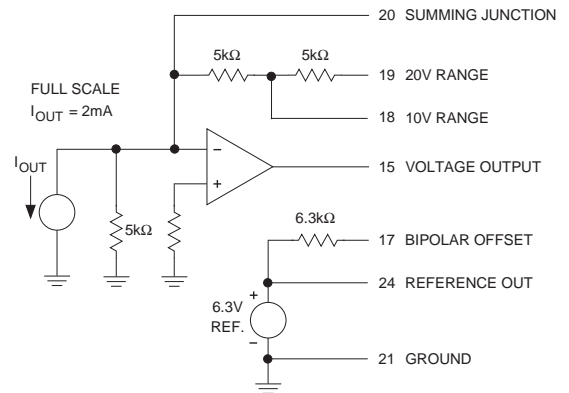


Figure 3. Output Circuit

CONNECTION DIAGRAMS

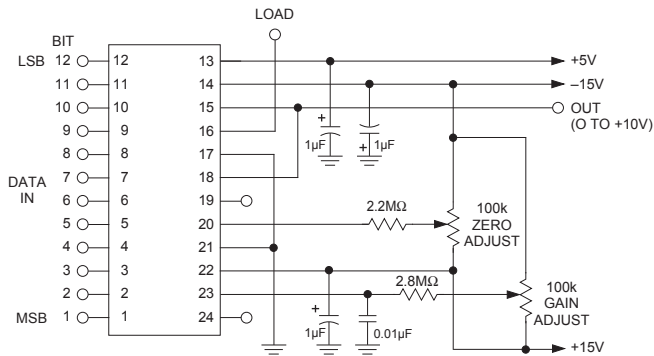


Figure 4. Unipolar Operation (0 to +10V)

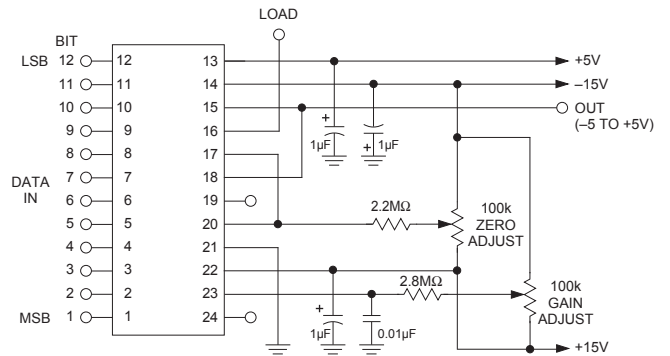


Figure 5. Bipolar Operation (±5V)

APPLICATIONS

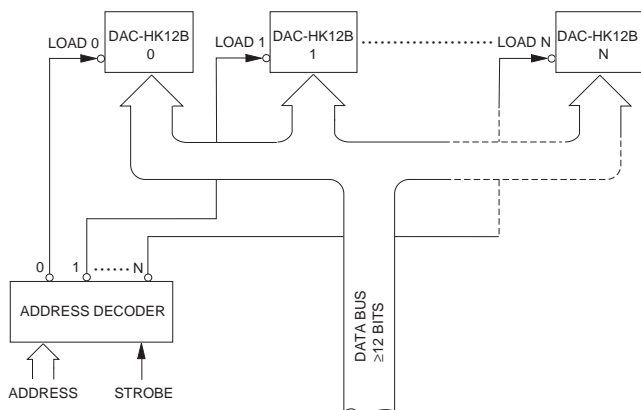


Figure 6. Interfacing to ≥12-Bit Data Bus

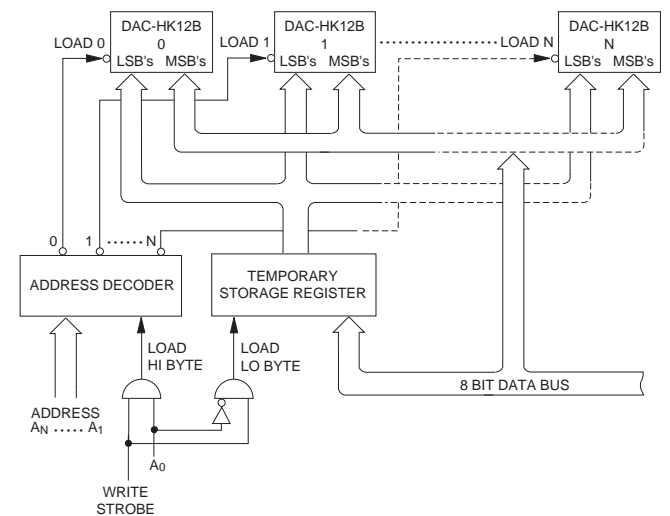


Figure 7. Interfacing to 8-Bit Data Bus

CODING TABLES

| STRAIGHT BINARY | | | OUTPUT RANGES | |
|-----------------|------|------|---------------|----------|
| MSB | | LSB | 0 to +10V | 0 to +5V |
| 1111 | 1111 | 1111 | +9.9976 | +4.9988 |
| 1100 | 0000 | 0000 | +7.5000 | +3.7500 |
| 1000 | 0000 | 0000 | +5.0000 | +2.5000 |
| 0100 | 0000 | 0000 | +2.5000 | +1.2500 |
| 0000 | 0000 | 0001 | +0.0024 | +0.0012 |
| 0000 | 0000 | 0000 | 0.0000 | 0.0000 |

Table 1. Unipolar Operation

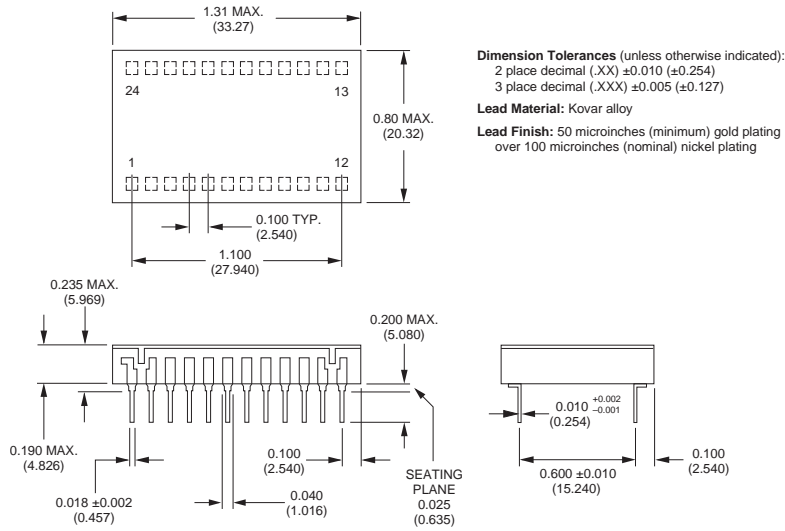
| OFFSET BINARY | | | TWO'S COMPLEMENT | | | OUTPUT RANGES | | |
|---------------|------|------|------------------|------|------|---------------|----------|------------|
| MSB | | LSB | MSB | | LSB | $\pm 10V$ | $\pm 5V$ | $\pm 2.5V$ |
| 1111 | 1111 | 1111 | 0111 | 1111 | 1111 | +9.9951 | +4.9976 | +2.4988 |
| 1100 | 0000 | 0000 | 0100 | 0000 | 0000 | +5.0000 | +2.5000 | +1.2500 |
| 1000 | 0000 | 0000 | 0000 | 0000 | 0000 | 0.0000 | 0.0000 | 0.0000 |
| 0100 | 0000 | 0000 | 1100 | 0000 | 0000 | -5.0000 | -2.5000 | -1.2500 |
| 0000 | 0000 | 0001 | 1000 | 0000 | 0001 | -9.9951 | -4.9976 | -2.4988 |
| 0000 | 0000 | 0000 | 1000 | 0000 | 0000 | -10.0000 | -5.0000 | -2.5000 |

Table 2. Bipolar Operation

| RANGE | CONNECT THESE PINS TOGETHER | | |
|------------|-----------------------------|---------|---------|
| $\pm 10V$ | 15 & 19 | 17 & 20 | |
| $\pm 5V$ | 15 & 18 | 17 & 20 | |
| $\pm 2.5V$ | 15 & 18 | 17 & 20 | 19 & 20 |
| +10V | 15 & 18 | 17 & 21 | |
| +5V | 15 & 18 | 17 & 21 | 19 & 20 |

Table 3. Output Range Selection

MECHANICAL DIMENSIONS (inches (mm))



ORDERING INFORMATION

| MODEL | OPERATING TEMPERATURE RANGE | RoHS RATING |
|--------------------------------|-----------------------------|-------------|
| Binary Coding | | |
| DAC-HK12BGC | 0 to +70°C | Non-RoHS |
| DAC-HK12BMC | 0 to +70°C | Non-RoHS |
| DAC-HK12BME | -40 to +85°C | Non-RoHS |
| DAC-HK12BMM | -55 to +125°C | Non-RoHS |
| DAC-HKB/883 | -55 to +125°C | Non-RoHS |
| DAC-HK12BGC-C | 0 to +70°C | RoHS |
| DAC-HK12BMC-C | 0 to +70°C | RoHS |
| DAC-HK12BME-C | -40 to +85°C | RoHS |
| DAC-HK12BMM-C | -55 to +125°C | RoHS |
| DAC-HKB-C/883 | -55 to +125°C | RoHS |
| Two's Complement Coding | | |
| DAC-HK12BGC-2 | 0 to +70°C | Non-RoHS |
| DAC-HK12BMC-2 | 0 to +70°C | Non-RoHS |
| DAC-HK12BME-2 | -40 to +85°C | Non-RoHS |
| DAC-HK12BMM-2 | -55 to +125°C | Non-RoHS |
| DAC-HKB-2/883 | -55 to +125°C | Non-RoHS |
| DAC-HK12BGC-2-C | 0 to +70°C | RoHS |
| DAC-HK12BMC-2-C | 0 to +70°C | RoHS |
| DAC-HK12BME-2-C | -40 to +85°C | RoHS |
| DAC-HK12BMM-2-C | -55 to +125°C | RoHS |
| DAC-HKB-2-C/883 | -55 to +125°C | RoHS |

The MIL-STD-883 units are available under DESC

Drawing Number 5962-89528. Contact DATEL for 883 product specifications.

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