

2559

PROTECTED QUAD POWER DRIVER

Providing improved output current limiting, the UDK, UDN, and UDQ2559B, EB, and LB quad power drivers combine AND logic gates and high-current bipolar outputs with complete output protection. Each of the four outputs will sink 700 mA in the on state. The outputs have a minimum breakdown voltage (load dump) of 60 V and a sustaining voltage of 40 V. The inputs are compatible with TTL and 5 V CMOS logic systems.

Over-current protection for each channel has been designed into these devices and is activated at approximately 1 A. It protects each output from short circuits with supply voltages up to 25 V. When an output current trip point is reached, that output stage is driven linearly resulting in a reduced output current level. If an over-current or short-circuit condition continues, the thermal-limiting circuits will first sense the rise in junction temperature and then the rise in chip temperature, further decreasing the output current. Under worst-case conditions, these devices will tolerate short circuits on all outputs, simultaneously.

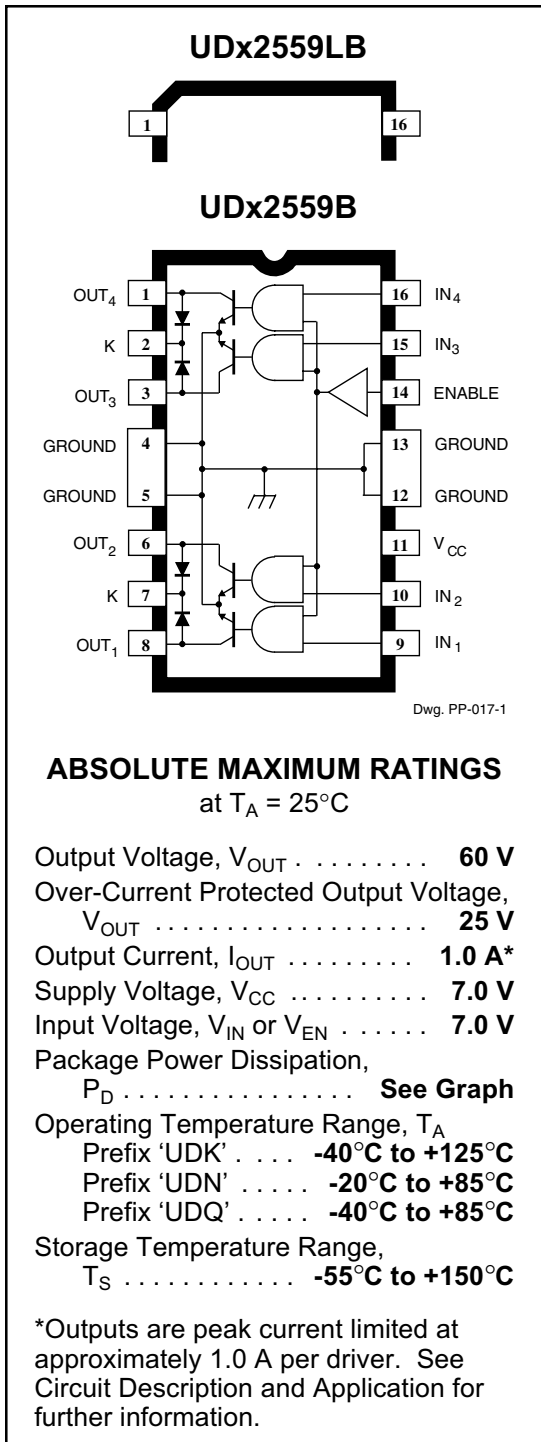
These devices can be used to drive various loads including incandescent lamps (without warming or limiting resistors) or inductive loads such as relays, solenoids, or dc stepping motors.

The suffix 'B' devices are 16-pin power DIPs, the suffix 'EB' devices are 28-lead power PLCCs and suffix 'LB' devices are 16-lead power SOICs for surface-mount applications. All three packages are of batwing construction to provide for maximum package power dissipation.

FEATURES

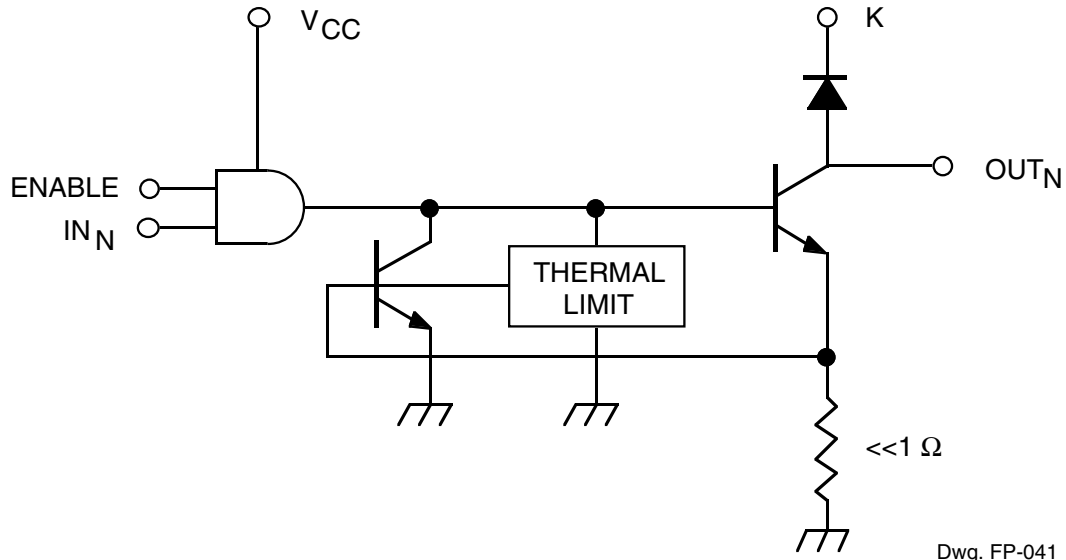
- 700 mA Output Current per Channel
- Independent Over-Current Protection for Each Driver
- Thermal Protection for Device and Each Driver
- Low Output-Saturation Voltage
- Integral Output Flyback Diodes
- TTL and 5 V CMOS Compatible Inputs
- Pin-Compatible With UDQ2543B/EB and UDK2549B/EB

Always order by complete part number: a prefix to indicate operating temperature range + the basic four-digit part number + a suffix to indicate package style, e.g., **UDK2559LB**.

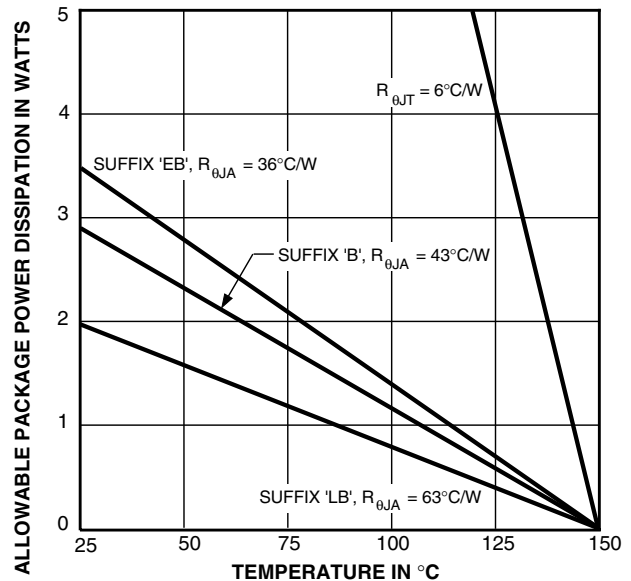
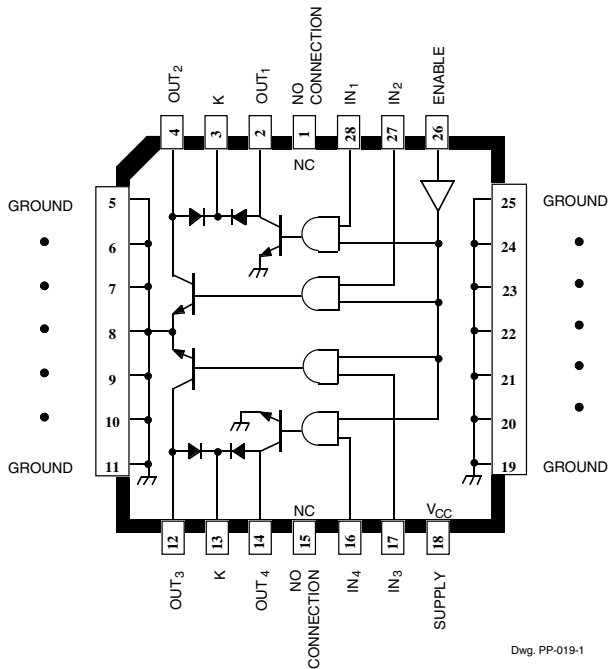


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FUNCTIONAL BLOCK DIAGRAM (1 of 4 Channels)



UDx2559EB



$$P_D = (V_{OUT1} \times I_{OUT1} \times dc) + \dots + (V_{OUTn} \times I_{OUTn} \times dc) + (V_{CC} \times I_{CC}) = (T_J - T_A) / R_{\theta JA}$$



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ELECTRICAL CHARACTERISTICS at $T_A = +25^\circ\text{C}$ (prefix 'UDN') or over operating temperature range (prefix 'UDK' or 'UDQ'), $V_{CC} = 4.75\text{ V to }5.25\text{ V}$

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Leakage Current	I_{CEX}	$V_{OUT} = 50\text{ V}, V_{IN} = 0.8\text{ V}, V_{EN} = 2.0\text{ V}$	—	<1.0	100	μA
		$V_{OUT} = 50\text{ V}, V_{IN} = 2.0\text{ V}, V_{EN} = 0.8\text{ V}$	—	<1.0	100	μA
Output Sustaining Voltage	$V_{OUT(SUS)}$	$I_{OUT} = 100\text{ mA}, V_{IN} = V_{EN} = 0.8\text{ V}$	40	—	—	V
Output Saturation Voltage	$V_{OUT(SAT)}$	All Devices, $I_{OUT} = 100\text{ mA}$	—	—	300	mV
		All Devices, $I_{OUT} = 400\text{ mA}$	—	—	500	mV
		'B' & 'EB' Packages Only, $I_{OUT} = 600\text{ mA}$	—	—	700	mV
Over-Current Trip	I_{TRIP}		—	1.0	—	A
Input Voltage	Logic 1	$V_{IN(1)}$ or $V_{EN(1)}$	2.0	—	—	V
	Logic 0	$V_{IN(0)}$ or $V_{EN(0)}$	—	—	0.8	V
Input Current	Logic 1	$V_{IN(1)}$ or $V_{EN(1)} = 2.0\text{ V}$	—	—	40	μA
	Logic 0	$V_{IN(0)}$ or $V_{EN(0)} = 0.8\text{ V}$	—	—	-10	μA
Total Supply Current	I_{CC}	All Outputs ON, $V_{IN}^* = V_{EN} = 2.0\text{ V}$	—	—	80	mA
		All Outputs OFF	—	—	5.0	mA
Clamp Diode Forward Voltage	V_F	$I_F = 1.0\text{ A}$	—	—	1.7	V
		$I_F = 1.5\text{ A}$	—	—	2.1	V
Clamp Diode Leakage Current	I_R	$V_R = 50\text{ V}, D_1 + D_2$ or $D_3 + D_4$	—	—	50	μA
Turn-On Delay	t_{PHL}	$I_{OUT} = 500\text{ mA}$	—	—	20	μs
	t_{PLH}	$I_{OUT} = 500\text{ mA}$	—	—	20	μs
Thermal Limit	T_J		—	165	—	$^\circ\text{C}$

Typical Data is for design information only.

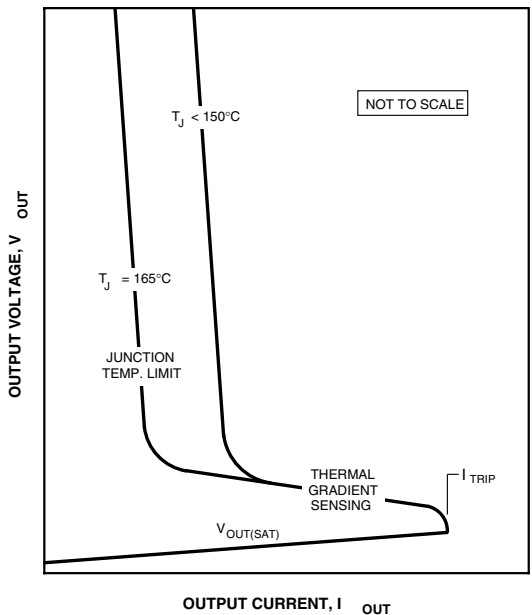
Negative current is defined as coming out of (sourcing) the specified terminal.

As used here, -100 is defined as greater than +10 (absolute magnitude convention) and the minimum is implicitly zero.

* All inputs simultaneously, all other tests are performed with each input tested separately.

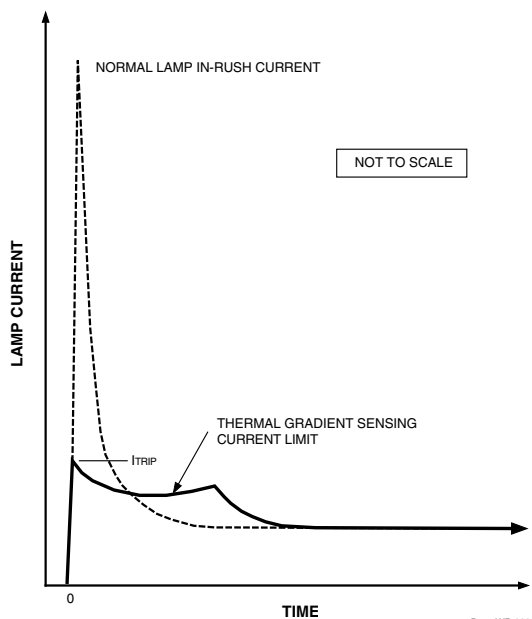
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TYPICAL OUTPUT CHARACTERISTIC



Dwg. GP-013

TYPICAL OUTPUT BEHAVIOR



Dwg. WP-008

CIRCUIT DESCRIPTION AND APPLICATION

INCANDESCENT LAMP DRIVER

High incandescent lamp turn-ON/in-rush currents can contribute to poor lamp reliability and destroy semiconductor lamp drivers. Warming or current-limiting resistors protect both driver and lamp but use significant power either when the lamp is OFF or when the lamp is ON, respectively. Lamps with steady-state current ratings up to 700 mA can be driven by these devices without the need for warming (parallel) or current-limiting (series) resistors.

When an incandescent lamp is initially turned ON, the cold filament is at minimum resistance and would normally allow a 10x to 12x in-rush current. With these drivers, during turn-ON, the high in-rush current is sensed by the internal low-value sense resistor. Drive current to the output stage is then diverted by the shunting transistor, and the load current is momentarily limited to approximately 1.0 A. During this short transition period, the output current is reduced to a value dependent on supply voltage and filament resistance. During lamp warmup, the filament resistance increases to its maximum value, the output stage goes into saturation and applies maximum rated voltage to the lamp.

INDUCTIVE LOAD DRIVER

Bifilar (unipolar) stepper motors, relays, or solenoids can be driven directly. The internal flyback diodes prevent damage to the output transistors by suppressing the high-voltage spikes that occur when turning OFF an inductive load.

For rapid current decay (fast turn-OFF speeds), the use of Zener diodes will raise the flyback voltage and improve performance. However, the peak voltage must not exceed the specified minimum sustaining voltage ($V_{SUPPLY} + V_Z + V_F \leq V_{OUT(SUS)}$).

FAULT CONDITIONS

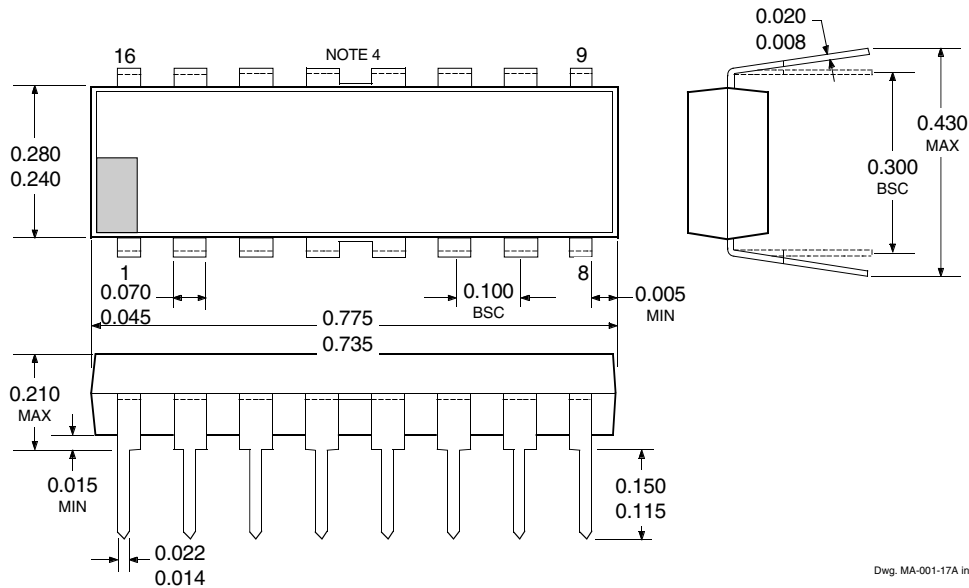
In the event of a shorted load, the load current will attempt to increase. As described above, the drive current to the affected output stage is reduced, causing the output stage to go linear, limiting the peak output current to approximately 1 A. As the power dissipation of that output stage increases, a thermal gradient sensing circuit will become operational, further decreasing the drive current to the affected output stage and reducing the output current to a value dependent on supply voltage and load resistance.

Continuous or multiple overload conditions causing the chip temperature to reach approximately 165°C will result in an additional reduction in output current to maintain a safe level.

If the fault condition is corrected, the output stage will return to its normal saturated condition.

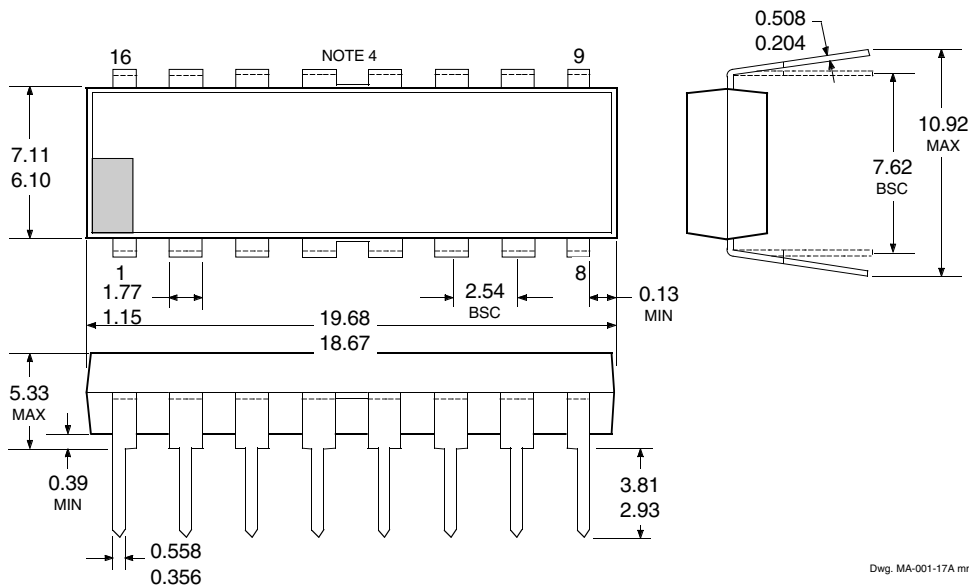
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UDx2559B Dimensions in Inches (controlling dimensions)



Dwg. MA-001-17A in

Dimensions in Millimeters (for reference only)



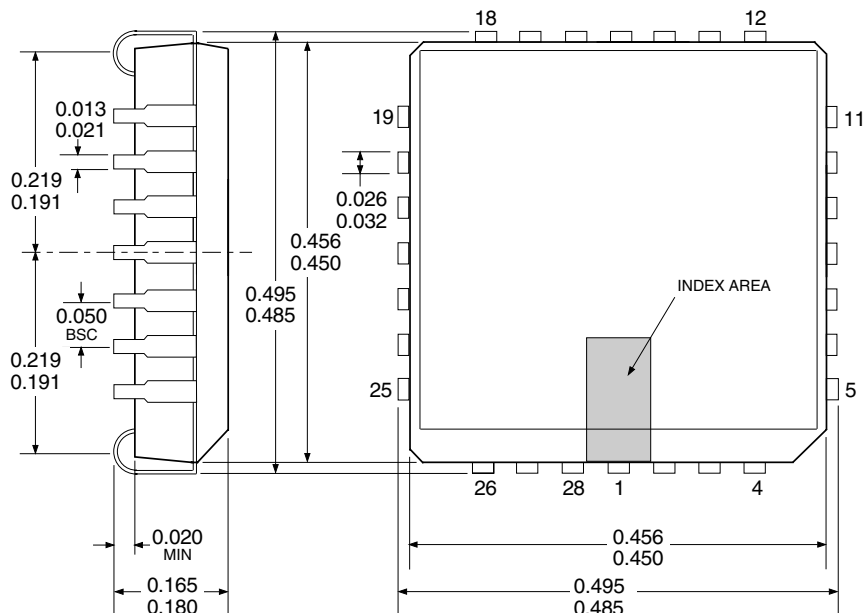
Dwg. MA-001-17A mm

- NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
 2. Lead spacing tolerance is non-cumulative
 3. Lead thickness is measured at seating plane or below.
 4. Webbed lead frame. Leads 4, 5, 12, and 13 are internally one piece.

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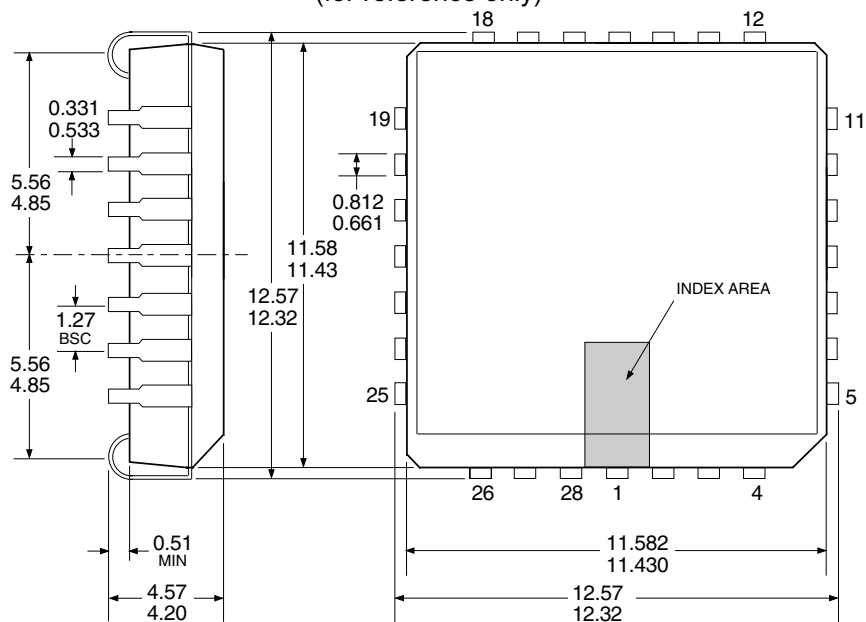
UDx2559EB

Dimensions in Inches
(controlling dimensions)



Dwg. MA-005-28A in

Dimensions in Millimeters
(for reference only)



Dwg. MA-005-28A mm

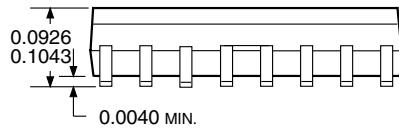
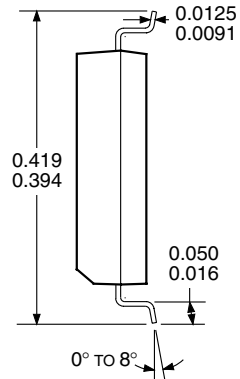
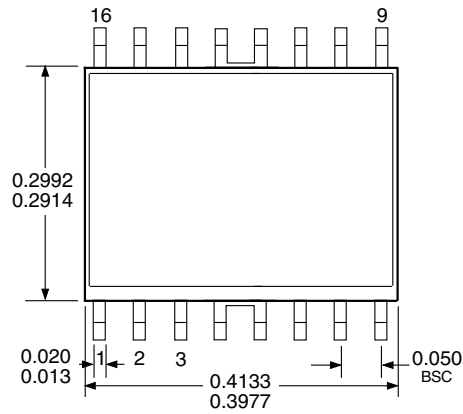
- NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
 2. Lead spacing tolerance is non-cumulative
 3. Webbed lead frame. Leads 5–11, and 19–25 are internally one piece.



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 Worcester, Massachusetts 01615-0036 (508) 853-5000

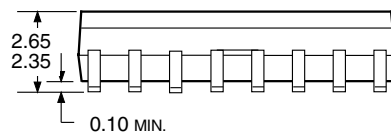
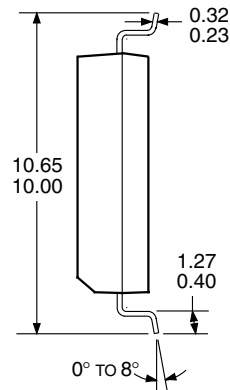
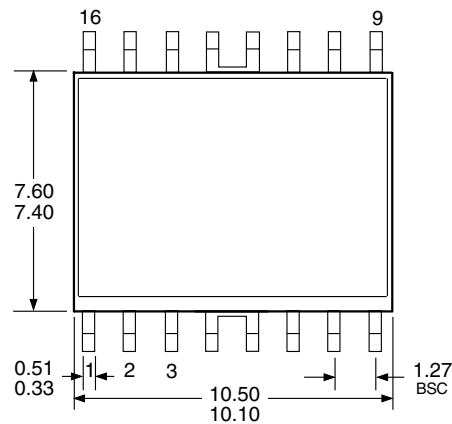
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UDx2559LB Dimensions in Inches (for reference only)



Dwg. MA-008-17A in

Dimensions in Millimeters (controlling dimensions)



Dwg. MA-008-17A mm

- NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
 2. Lead spacing tolerance is non-cumulative
 3. Webbed lead frame. Leads 4, 5, 12, and 13 are internally one piece.

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