International Rectifier

ADVANCE INFORMATION **Data Sheet No. PD60175-C**

IR2171

LINEAR CURRENT SENSING IC

Features

- Floating channel up to +600V
- Monolithic integration
- Linear current feedback through shunt resistor
- Direct digital PWM output for easy interface
- Low IQBS allows the boot strap power supply
- High Common Mode Noise Immunity
- Input overvoltage Protection for IGBT short circuit condition
- Open Drain output

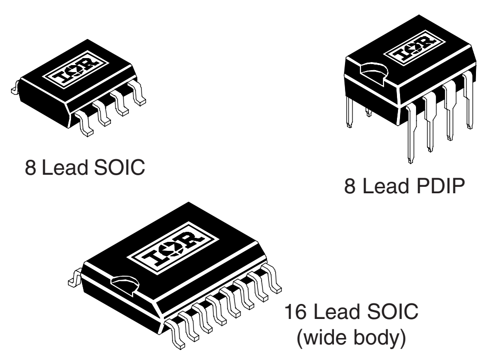
Product Summary

V_{OFFSET}	600V
I_{QBS}	1mA
V_{in}	+/-260mVmax
Gain temp. drift	20ppm/°C(typ.)
f_O	40kHz (typ.)

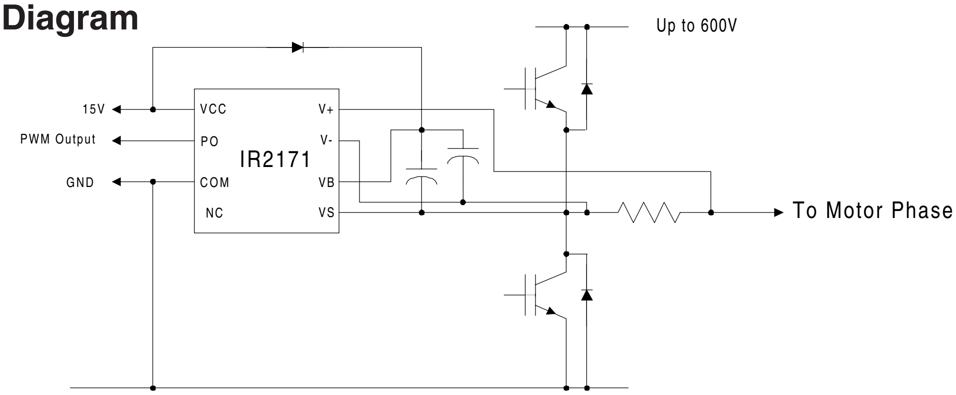
Descriptions

IR2171 is the linear current sensing IC designed for motor drive applications. It senses the motor phase current through an extenal shunt resistor, converts from analog to digital signal, and transfers the signal to the low side. IR's proprietary high voltage isolation technology is implemented to enable the high bandwidth signal processing. The output format is discrete PWM at 40kHz to eliminate need for the A/D input interface. It allows direct interface to uP via simple counter based measurement. The independently powered output enables easy interface to the opto coupler device for galvanic isolation if needed.

Packages



Block Diagram



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_S	High side offset voltage		-0.3	600	V
V_{BS}	High side floating supply voltage		V_S -0.3	25	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{IN}	Maximum input voltage between V_{IN+} and V_{IN-}		-5	5	
V_{PO}	Digital PWM output voltage		COM -0.3	V_{CC} +0.3	
V_{IN-}	V_{IN-} input voltage (note 1)		Vs -5	V_B+0.3	
dV/dt	Allowable offset voltage slew rate		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	8 lead SOIC	—	.625	W
		8 lead PDIP	—	1.0	
		16 lead SOIC	—	1.25	
Rth_{JA}	Thermal resistance, junction to ambient	8 lead SOIC	—	200	°C/W
		8 lead PDIP	—	125	
		16 lead SOIC	—	100	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Note 1: Capacitors are required between V_B and Vin-, and between V_B and Vs pins when bootstrap power is used. The external power supply, when used, is required between V_B and Vin-, and between V_B and Vs pins.

Recommended Operating Conditions

The output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply voltage	V_S +13.0	V_S +20	V
V_S	High side floating supply offset voltage	note 2	600	
V_{PO}	Digital PWM output voltage	COM	V_{CC}	
V_{CC}	Low side and logic fixed supply voltage	9.5	20	
V_{IN}	Input voltage between V_{IN+} and V_{IN-}	-260	+260	mV
T_A	Ambient temperature	-40	125	°C

Note 2: Logic operation for Vs of -5 to +600V. Logic state held for Vs of -5V to $-V_{BS}$.

DC Electrical Characteristics

V_{CC} = V_{BS} = 15V, unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IN}	Nominal input voltage range before saturation $\lvert V_{IN+} - V_{IN-}\rvert$	-260	—	260	mV	
V_{OS}	Input offset voltage	-10	0	10	mV	V_{IN} = 0V (Note 1)
$\Delta V_{OS}/\Delta TA$	Input offset voltage temperature drift	—	25	—	µV/°C	
G	Gain (duty cycle % per V_{IN})	157	162	167	%/V	max gain error=5% (Note 2)
$\Delta G/\Delta TA$	Gain temperature drift	—	20	—	ppm/°C	
I_{LK}	Offset supply leakage current	—	—	50	µA	$V_B = V_S$ = 600V
I_{QBS}	Quiescent V_{BS} supply current	—	1	2	mA	V_S = 0V
I_{QCC}	Quiescent V_{CC} supply current	—	—	1	mA	
LIN	Linearity (duty cycle deviation from ideal linearity curve)	—	0.5	1	%	
$\Delta LIN/\Delta TA$	Linearity temperature drift	—	.005	—	%/°C	
I_{O-}	Output sink current	20	—	—	mA	V_O = 1V
		2	—	—		V_O = 0.1V

Note 1: ±10mV offset represents ±1.5% duty cycle fluctuation
Note 2: Gain = (full range of duty cycle in %) / (full input voltage range).

AC Electrical Characteristics

V_{CC} = V_{BS} = 15V, unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
Propagation delay characteristics						
fo	Carrier frequency output	—	40	—	kHz	figure 1
$\Delta f/\Delta TA$	Temperature drift of carrier frequency	—	500	—	ppm/°C	V_{IN} = 0V & 5V
Dmin	Minimum duty	—	7	—	%	V_{IN+}=-260mV, V_{IN-}=0
Dmax	Maximum duty	—	93	—	%	V_{IN+}=+260mV, V_{IN-}=0
BW	fo bandwidth		15		kHz	V_{IN+}=100mV pk-pk sine wave, -3dB
PHS	Phase shift at 1kHz		-10		°	V_{IN+}=100mVpkpk sine wave

Timing Waveforms

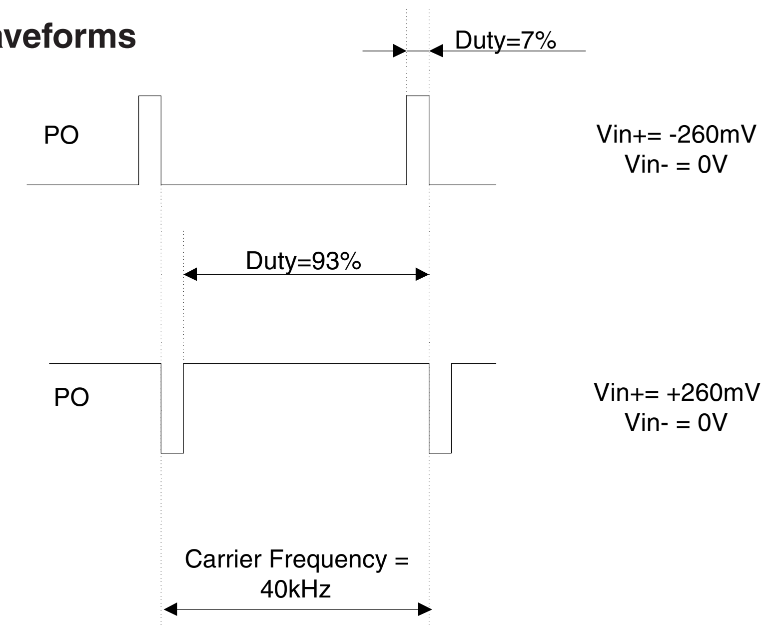


Figure 1 Output waveform

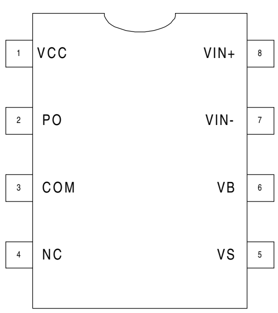
Application Hint:

Temperature drift of the output carrier frequency can be cancelled by measuring both a PWM period and the on-time of PWM (Duty) at a same time. Since both periods vary in the same direction, computing the ratio between these values at each PWM periods gives consistent measurement of the current feedback over the temperature drift.

Lead Definitions

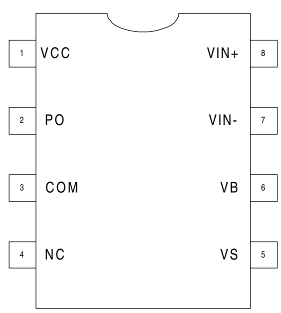
Symbol	Description
V_{CC}	Low side and logic supply voltage
COM	Low side logic ground
VIN+	Positive sense input
VIN-	Negative sense input
VB	High side supply
VS	High side return
PO	Digital PWM output
N.C.	No connection

Lead Assignment



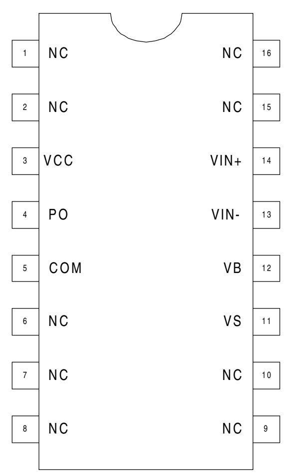
8 lead SOIC

IR2171S



8 lead PDIP

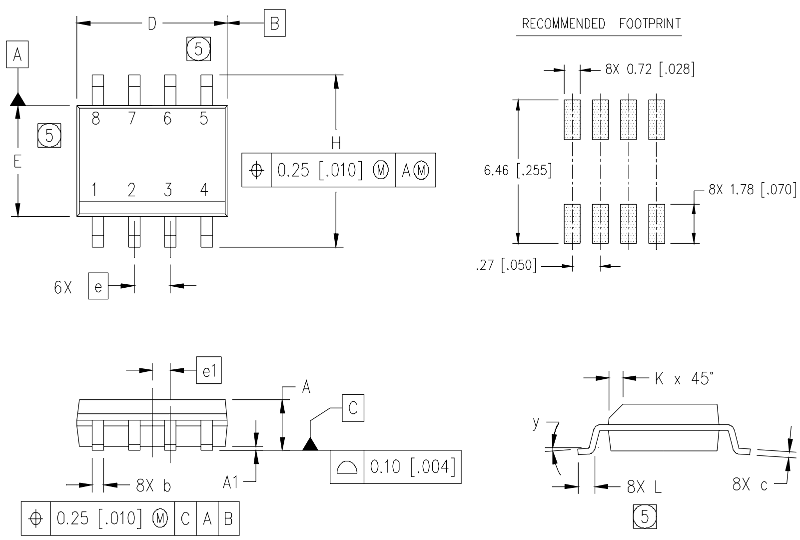
IR2171



16 lead SOIC

IR21716S

Case Outline



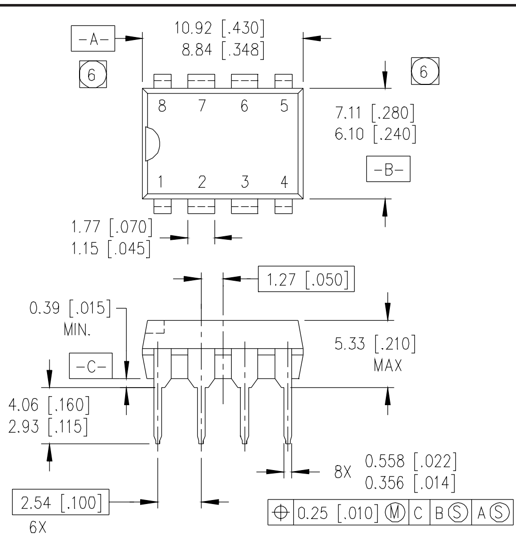
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.014	.018	0.36	0.46
c	.0075	.0098	0.19	0.25
D	.189	.196	4.80	4.98
E	.150	.157	3.81	3.99
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.011	.019	0.28	0.48
L	.016	.050	0.41	1.27
y	0°	8°	0°	8°

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.006].
6. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

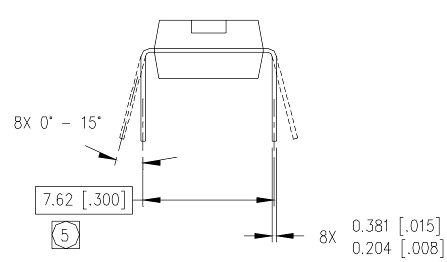
8 Lead SOIC

(MS-012AA) 01-0021 09



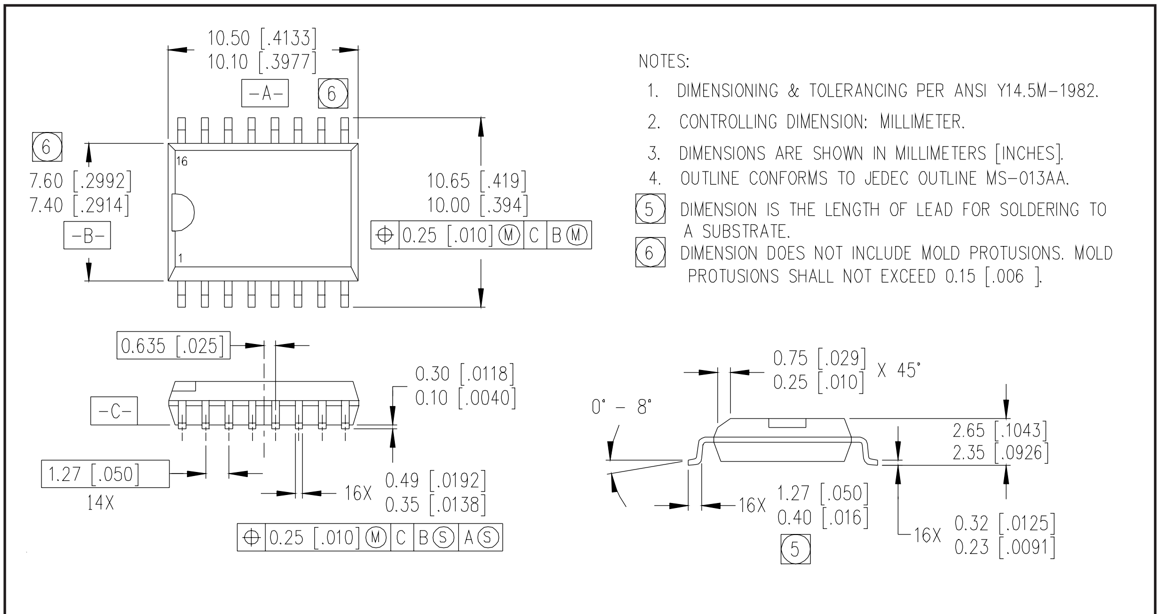
NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.

5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



8 Lead PDIP

01-3003 01



16 Lead SOIC (wide body)

01-3014 03

International IOR Rectifier

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Data and specifications subject to change without notice. 6/29/2000