



Improved, 16-Channel/Dual 8-Channel, CMOS Analog Multiplexers

DG406/DG407

General Description

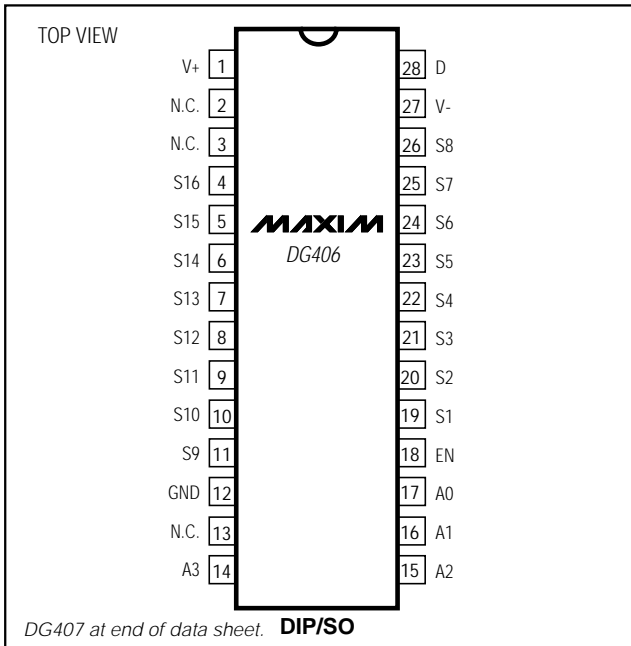
Maxim's redesigned DG406 and DG407 CMOS analog multiplexers now feature guaranteed matching between channels (8Ω max) and flatness over the specified signal range (9Ω max). These low on-resistance muxes (100Ω max) conduct equally well in either direction and feature guaranteed low charge injection (15pC max). In addition, these new muxes offer low input off-leakage current over temperature—less than 5nA at +85°C.

The DG406 is a 1 of 16 multiplexer/demultiplexer and the DG407 is a dual 8-channel multiplexer/demultiplexer. Both muxes operate with a +4.5V to +30V single supply and with ±4.5V to ±20V dual supplies. ESD protection is guaranteed to be greater than 2000V per Method 3015.7 of MIL-STD 883. These improved muxes are pin-compatible plug-in upgrades for the industry standard DG406 and DG407.

Applications

- Sample-and-Hold Circuits
- Test Equipment
- Guidance and Control Systems
- Communications Systems
- Data-Acquisition Systems
- Audio Signal Routing

Pin Configurations



Features

- ◆ Pin-Compatible Plug-In Upgrade for Industry Standard DG406/DG407
- ◆ Guaranteed Matching Between Channels, 8Ω Max
- ◆ Guaranteed On-Resistance Flatness, 9Ω Max
- ◆ Guaranteed Low Charge Injection, 15pC Max
- ◆ Low On-Resistance 100Ω Max
- ◆ Input Leakage, 5nA Max at +85°C
- ◆ Low Power Consumption, 1.25mW Max
- ◆ Rail-to-Rail Signal Handling
- ◆ Digital Input Controls TTL/CMOS Compatible
- ◆ ESD Protection >2000V per Method 3015.7

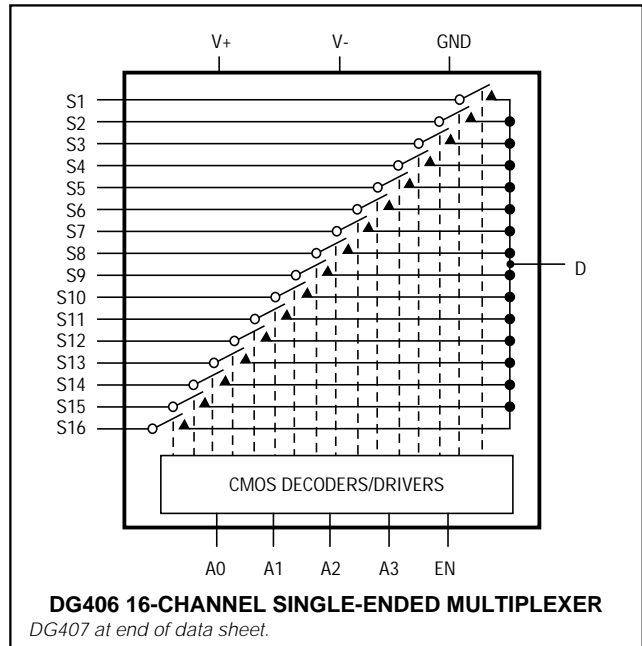
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
DG406CJ	0°C to +70°C	28 Plastic DIP
DG406CWI	0°C to +70°C	28 Wide SO
DG406C/D	0°C to +70°C	Dice*
DG406DJ	-40°C to +85°C	28 Plastic DIP
DG406DWI	-40°C to +85°C	28 Wide SO
DG406DN	-40°C to +85°C	28 PLCC
DG406AK	-55°C to +125°C	28 CERDIP

Ordering Information continued at end of data sheet.

* Contact factory for dice specifications.

Functional Diagrams



Maxim Integrated Products 1

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Improved, 16-Channel/Dual 8-Channel, CMOS Analog Multiplexers

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-

V+-0.3V, 44V
GND-0.3V, 25V
Digital Inputs, S, D (Note 1)(V- - 2V) to (V+ + 2V) or 30mA (whichever occurs first)
Continuous Current (any terminal)30mA
Peak Current, S or D (pulsed at 1ms, 10% duty cycle max)100mA
Continuous Power Dissipation (T _A = +70°C)	
Plastic DIP (derate 9.09mW/°C above +70°C)727mW

Wide SO (derate 12.50mW/°C above +70°C)1000mW
PLCC (derate 10.53mW/°C above +70°C)842mW
CERDIP (derate 16.67mW/°C above +70°C)1333mW
Operating Temperature Ranges	
DG406/DG407C_0°C to +70°C
DG406/DG407D_-40°C to +85°C
DG406/DG407AK-55°C to +125°C
Storage Temperature Range-65°C to +150°C
Lead Temperature (soldering, 10sec)+300°C

Note 1: Signals on S₋, D₋, A0, A1, A2, A3, or EN exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current ratings.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = 15V, V- = -15V, GND = 0V, V_{AH} = +2.4V, V_{AL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS	
SWITCH								
Analog Signal Range	V _{ANALOG}	(Note 3)		-15		15	V	
Drain-Source On-Resistance	r _{DS(ON)}	I _S = -1.0mA, V _D = ±10V	T _A = +25°C	60		100	Ω	
			T _A = T _{MIN} to T _{MAX}			125		
On-Resistance Matching Between Channels	Δr _{DS(ON)}	I _S = -1.0mA, V _D = ±10V (Note 4)	T _A = +25°C	1.5		8	Ω	
			T _A = T _{MIN} to T _{MAX}			10		
On-Resistance Flatness	r _{FLAT}	I _S = -1.0mA, V _D = ±5V or 0V	T _A = +25°C	1.8		9	Ω	
			T _A = T _{MIN} to T _{MAX}			12		
Source-Off Leakage Current (Note 5)	I _{S(OFF)}	V _D = ∓10V, V _S = ±10V, V _{EN} = 0V	T _A = +25°C	-0.5	0.01	0.5	nA	
			T _A = T _{MIN} to T _{MAX}	C, D	-5			5
				A	-50			50
Drain-Off Leakage Current (Note 5)	I _{D(OFF)}	V _D = ±10V, V _S = ∓10V, V _{EN} = 0V	DG406	T _A = +25°C	-1	0.02	1	nA
				T _A = T _{MIN} to T _{MAX}	C, D	-40		
		A	-200			200		
		V _D = ∓10V, V _S = ±10V, V _{EN} = 0V	DG407	T _A = +25°C	-1	0.02	1	
				T _A = T _{MIN} to T _{MAX}	C, D	-20		
		A	-100			100		
Drain-On Leakage Current (Note 5)	I _{D(ON)} + I _{S(ON)}	V _D = ±10V, V _S = ±10V, sequence each switch on	DG406	T _A = +25°C	-1	0.02	1	nA
				T _A = T _{MIN} to T _{MAX}	C, D	-40		
		A	-200			200		
		V _D = ±10V, V _S = ±10V, sequence each switch on	DG407	T _A = +25°C	-1	0.02	1	
				T _A = T _{MIN} to T _{MAX}	C, D	-20		
		A	-100			100		

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ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V₊ = 15V, V₋ = -15V, GND = 0V, V_{AH} = +2.4V, V_{AL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS	
INPUT								
Input Current with Input Voltage High	I _{AH}	V _A = 2.4V or 15V		-1.0		1.0	μA	
Input Current with Input Voltage Low	I _{AL}	V _{EN} = 0V or 2.4V, V _A = 0V		-1.0		1.0	μA	
SUPPLY								
Power-Supply Range				±4.5		±20	V	
Positive Supply Current	I ₊	V _{EN} = V _A = 0V or 4.5V	T _A = +25°C		16	30	μA	
			T _A = T _{MIN} to T _{MAX}			75		
		V _{EN} = 2.4V, V _{A(ALL)} = 0V or 2.4V	T _A = +25°C		0.075	0.5	mA	
			T _A = T _{MIN} to T _{MAX}			1		
Negative Supply Current	I ₋	V _{EN} = 2.4V, V _{A(ALL)} = 0V or 2.4V	T _A = +25°C		-1	1	μA	
			T _A = T _{MIN} to T _{MAX}			-10		10
DYNAMIC								
Transition Time	t _{TRANS}	Figure 2	T _A = +25°C		110	300	ns	
			T _A = T _{MIN} to T _{MAX}			400		
Break-Before-Make Interval	t _{OPEN}	Figure 4	T _A = +25°C		10	40	ns	
Enable Turn-On Time	t _{ON(EN)}	Figure 3	T _A = +25°C			130	200	ns
			T _A = T _{MIN} to T _{MAX}				400	
Enable Turn-Off Time	t _{OFF(EN)}	Figure 3	T _A = +25°C			55	150	ns
			T _A = T _{MIN} to T _{MAX}				300	
Charge Injection (Note 3)	Q	C _L = 1.0nF, V _S = 0V, R _S = 0Ω, Figure 5	T _A = +25°C		2	15	pC	
Off Isolation (Note 6)	V _{ISO}	V _{EN} = 0V, R _L = 1kΩ, f = 100kHz, Figure 6	T _A = +25°C		-69		dB	
Crosstalk Between Channels	V _{CT}	V _{EN} = 2.4V, f = 100kHz, V _{GEN} = 1V _{P-P} , R _L = 1kΩ, Figure 7	T _A = +25°C		-92		dB	
Logic Input Capacitance	C _{IN}	f = 1MHz	T _A = +25°C		8		pF	
Source-Off Capacitance	C _{S(OFF)}	f = 1MHz, V _{EN} = V _S = 0V, Figure 8	T _A = +25°C		8		pF	
Drain-Off Capacitance	C _{D(OFF)}	f = 1MHz, V _{EN} = 0.8V, V _D = 0V, Figure 8	DG406	T _A = +25°C		130	pF	
			DG407			65		
Drain-Source On Capacitance	C _{D(ON)} + C _{S(ON)}	f = 1MHz, V _{EN} = 2.4V, V _D = 0V, Figure 8	DG406	T _A = +25°C		140	pF	
			DG407			70		

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ELECTRICAL CHARACTERISTICS—Single Supply

(V+ = 12V, V- = 0V, GND = 0V, VAH = +2.4V, VAL = +0.8V, TA = TMIN to TMAX, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
SWITCH						
Analog Signal Range	VANALOG	(Note 3)	0		12	V
Drain-Source On-Resistance	r _{DS(ON)}	I _S = -1.0mA V _D = 3V or 10V T _A = +25°C		120	175	Ω
DYNAMIC						
Transition Time (Note 3)	t _{TRANS}	V _{S1} = 8V, V _{S16} = 0V, V _A = 0V, Figure 2 T _A = +25°C		130	450	ns
Enable Turn-On Time (Note 3)	t _{ON(EN)}	V _{AL} = 0V, V _{S1} = 5V, Figure 3 T _A = +25°C		105	600	ns
Enable Turn-Off Time (Note 3)	t _{OFF(EN)}	V _{AL} = 0V, V _{S1} = 5V, Figure 3 T _A = +25°C		80	300	ns
Charge Injection (Note 3)	Q	C _L = 1.0nF, V _{S1} = 0V, R _S = 0Ω T _A = +25°C		2	10	pC

Note 2: The algebraic convention where the most negative value is a minimum and the most positive value a maximum is used in this data sheet.

Note 3: Guaranteed by design.

Note 4: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$. On-resistance match between channels and flatness are guaranteed only with specified voltages. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured at the extremes of the specified analog signal range.

Note 5: Leakage parameters are 100% tested at the maximum rated hot temperature and guaranteed by correlation at +25°C.

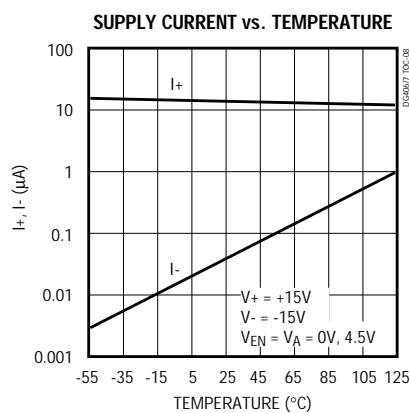
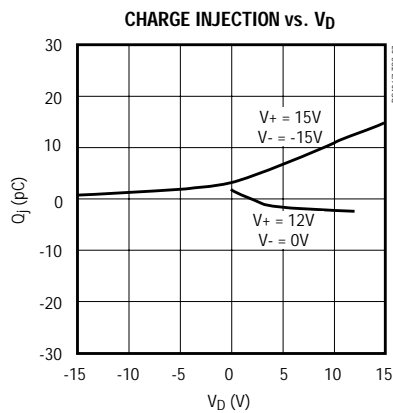
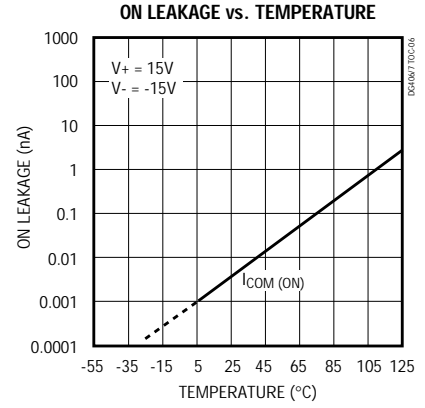
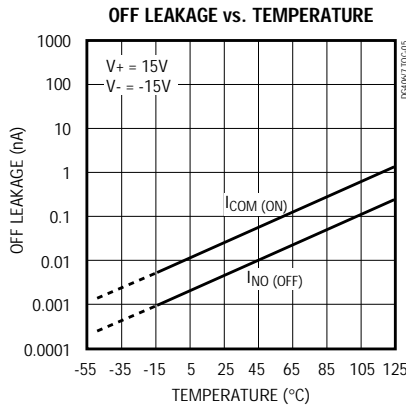
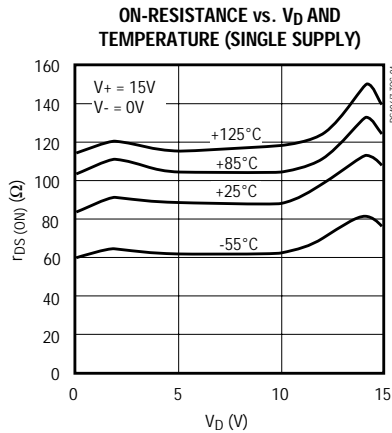
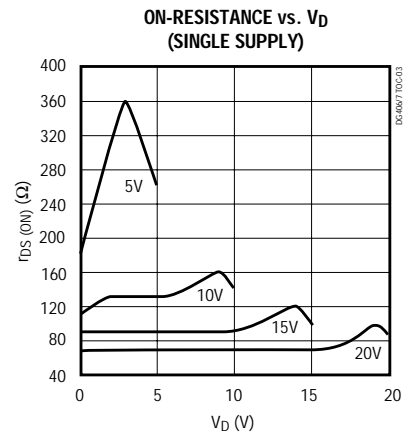
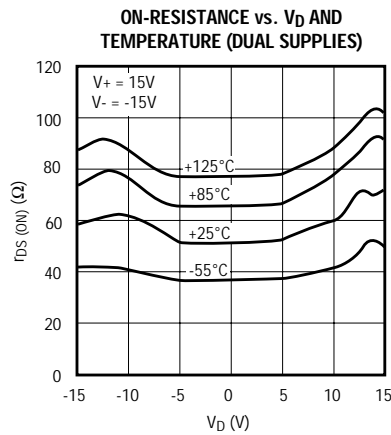
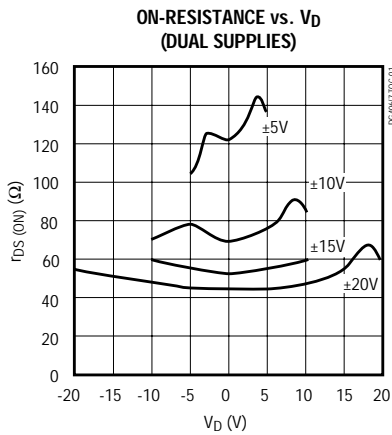
Note 6: Off isolation = $20 \log V_D/V_S$, where V_D = output and V_S = input to off switch.

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Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)

DG406/DG407



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Pin Descriptions

DG406 PIN	NAME	FUNCTION
1	V+	Positive Supply Voltage Input
2, 3, 13	N.C.	No Internal Connections
4-11	S16-S9	Bidirectional Analog Inputs
12	GND	Ground
14-17	A3-A0	Address Inputs
18	EN	Enable Inputs
19-26	S1-S8	Bidirectional Analog Inputs
27	V-	Negative Supply Voltage Input
28	D	Bidirectional Output

DG407 PIN	NAME	FUNCTION
1	V+	Positive Supply Voltage Input
2	DB	Bidirectional Output B
3, 13, 14	N.C.	No Internal Connection
4-11	S8B-S1B	Bidirectional Analog Inputs
12	GND	Ground
15, 16, 17	A2, A1, A0	Address Inputs
18	EN	Enable Input
19-26	S1A-S8A	Bidirectional Analog Inputs
27	V-	Negative Supply Voltage Input
28	DA	Bidirectional Output A

Applications Information

Operation with Supply Voltages Other than $\pm 15V$

Using supply voltages other than $\pm 15V$ reduces the analog signal range. The DG406/DG407 switches operate with $\pm 4.5V$ to $\pm 20V$ bipolar supplies or with a $+4.5V$ to $+30V$ single supply; connect V- to GND when operating with a single supply. Also, both device types can operate with unbalanced supplies such as $+24V$ and $-5V$. The *Typical Operating Characteristics* graphs show typical on-resistance with 20V, 15V, 10V, and 5V supplies. (Switching times increase by a factor of two or more for operation at 5V.)

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V+ on first, then V-, followed by the logic inputs and analog signals. If power-supply sequencing is not possible, add two small signal diodes in series with supply pins for overvoltage protection (Figure 1). Adding diodes reduces the analog

signal range to 1V above V+ and 1V below V-, but low switch resistance and low leakage characteristics are unaffected. Device operation is unchanged, and the difference between V+ and V- should not exceed +44V.

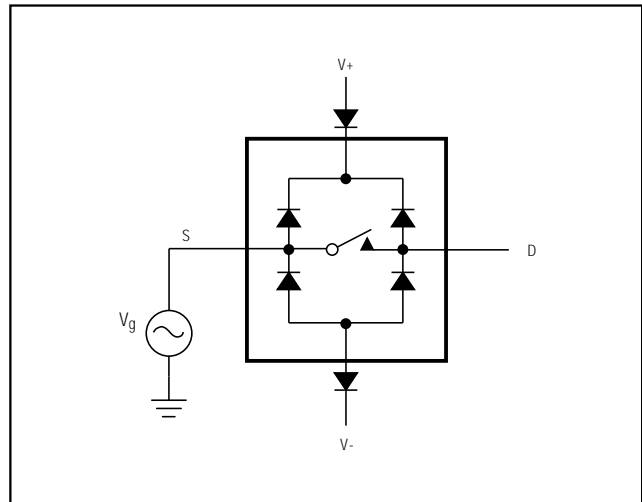


Figure 1. Overvoltage Protection Using External Blocking Diodes

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Test Circuits/Timing Diagrams

DG406/DG407

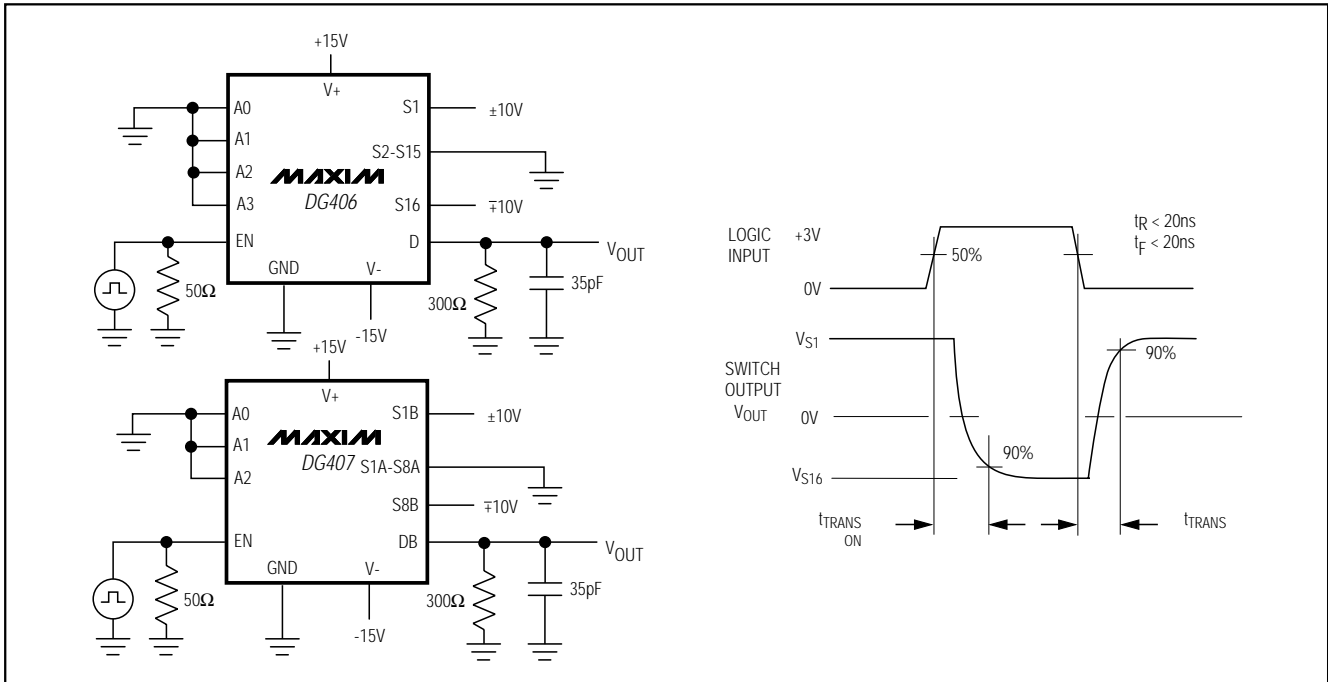


Figure 2. Transition Time

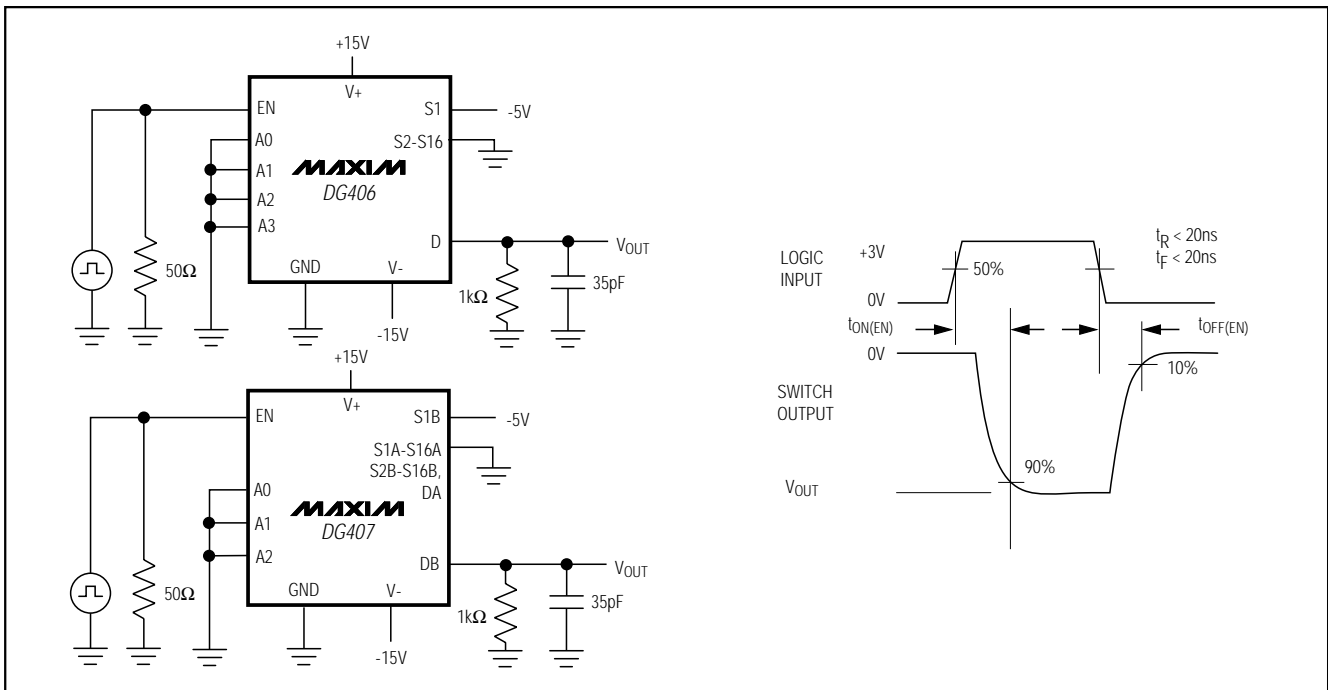


Figure 3. Enable Switching Time

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Test Circuits/Timing Diagrams (continued)

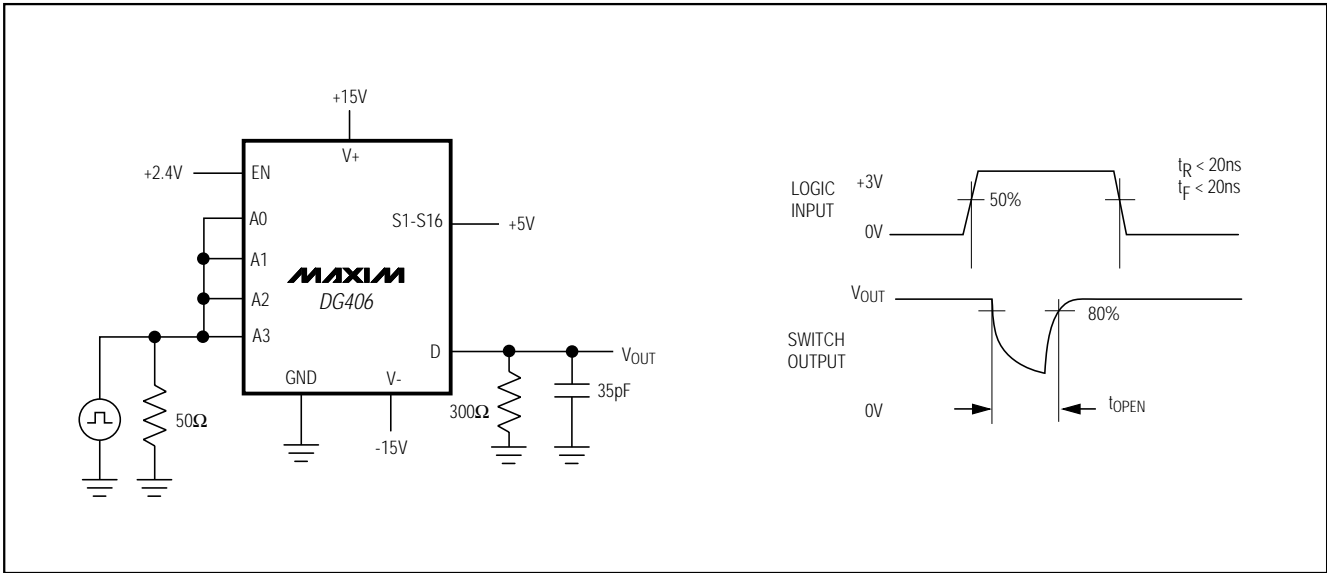


Figure 4. Break-Before-Make Interval

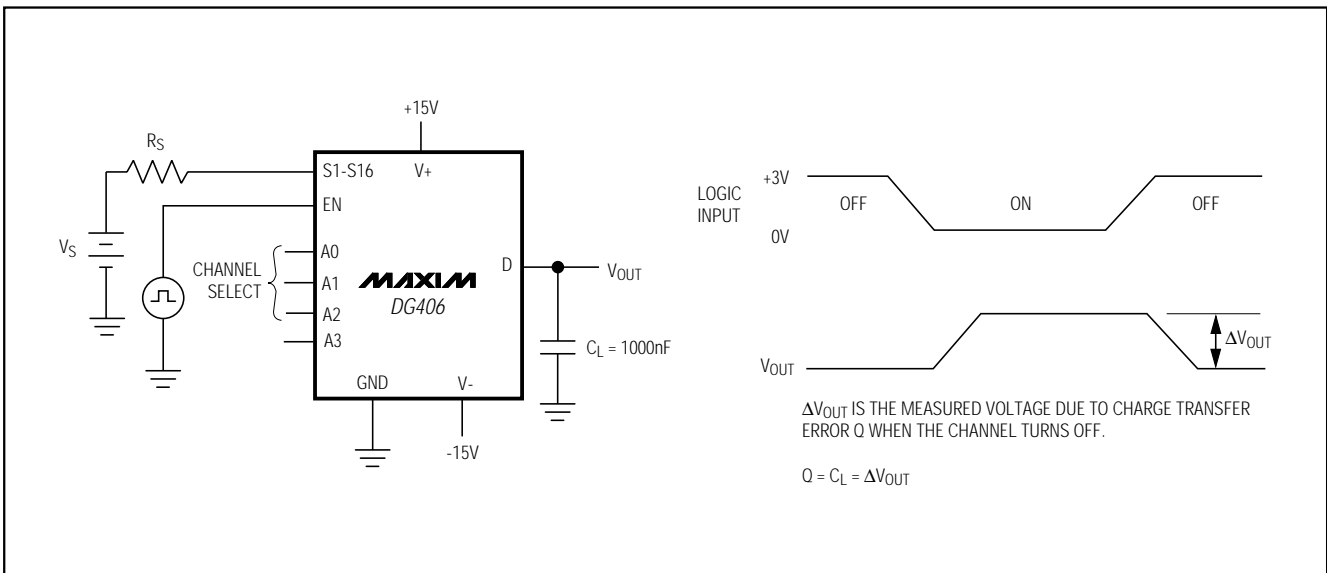


Figure 5. Charge Injection

Improved, 16-Channel/Dual 8-Channel, CMOS Analog Multiplexers

Test Circuits/Timing Diagrams (continued)

DG406/DG407

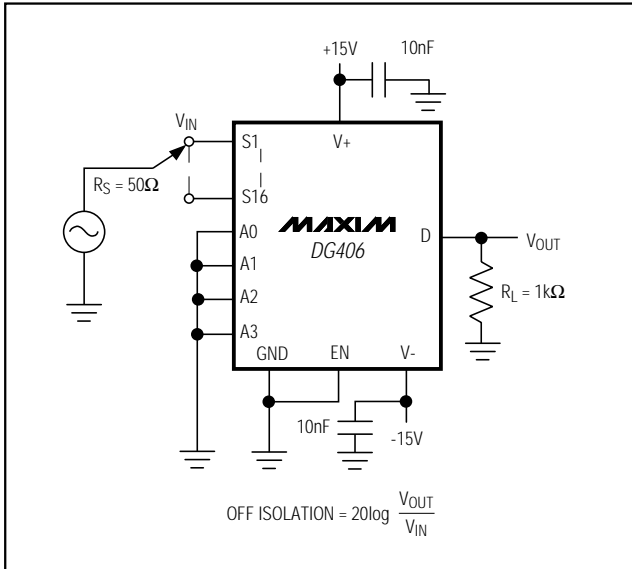


Figure 6. Off Isolation

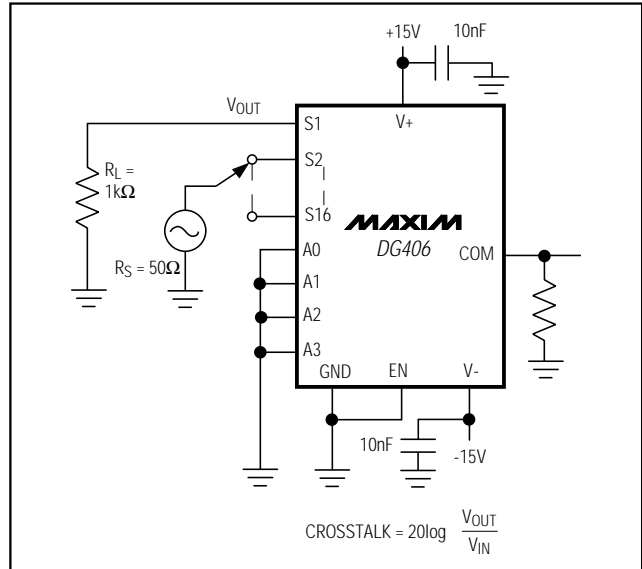


Figure 7. Crosstalk

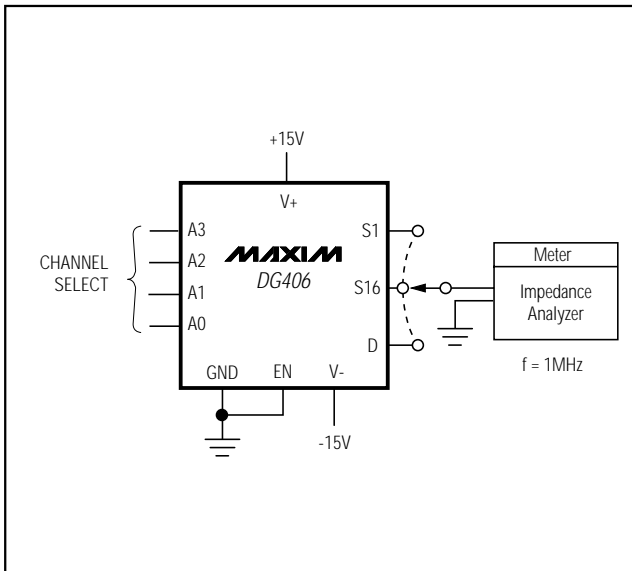
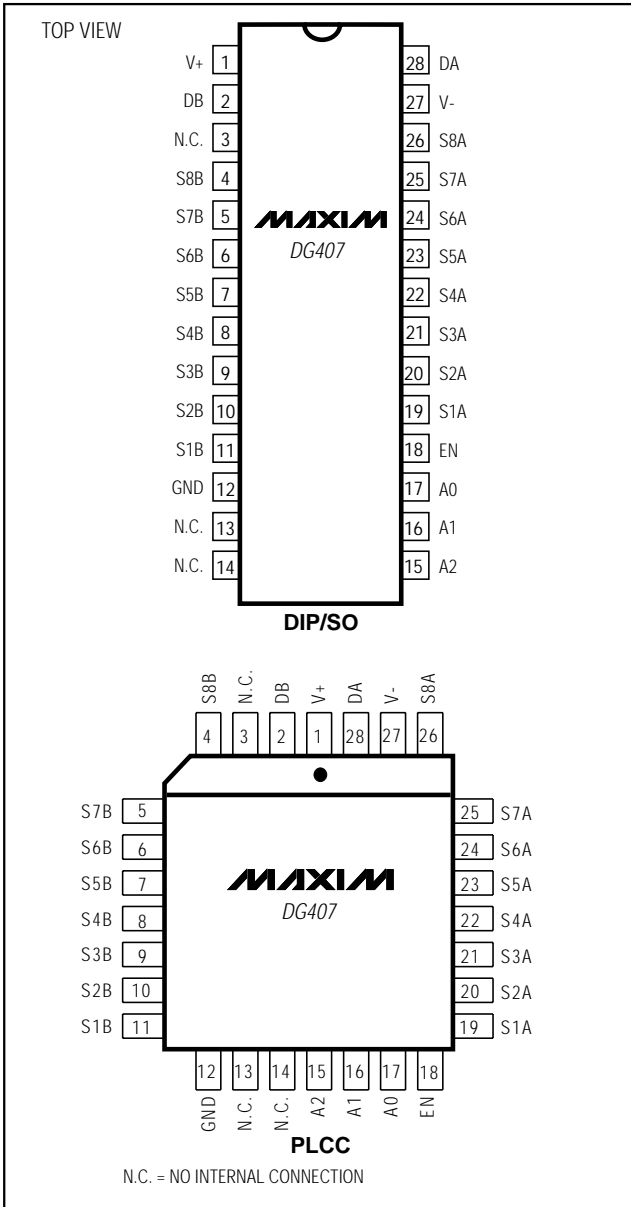


Figure 8. Source/Drain Capacitance

Improved, 16-Channel/Dual 8-Channel, CMOS Analog Multiplexers

Pin Configurations/Functional Diagrams/Truth Tables (continued)



A3	A2	A1	A0	EN	ON Switch
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

DG406

LOGIC "0" $V_{AL} \leq 0.8V$, LOGIC "1" = $V_{AH} \geq 2.4V$

A2	A1	A0	EN	ON Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

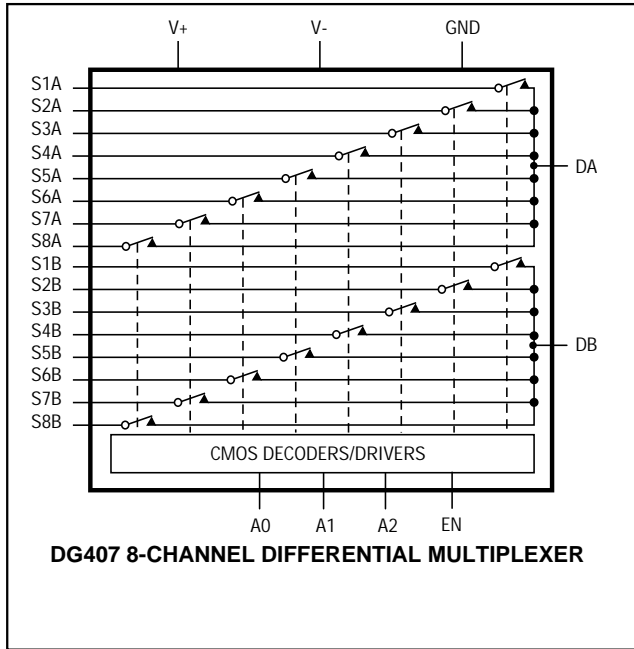
DG407

LOGIC "0" $V_{AL} \leq 0.8V$, LOGIC "1" = $V_{AH} \geq 2.4V$

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DG406/DG407

_Functional Diagrams (continued)



_Ordering Information (continued)

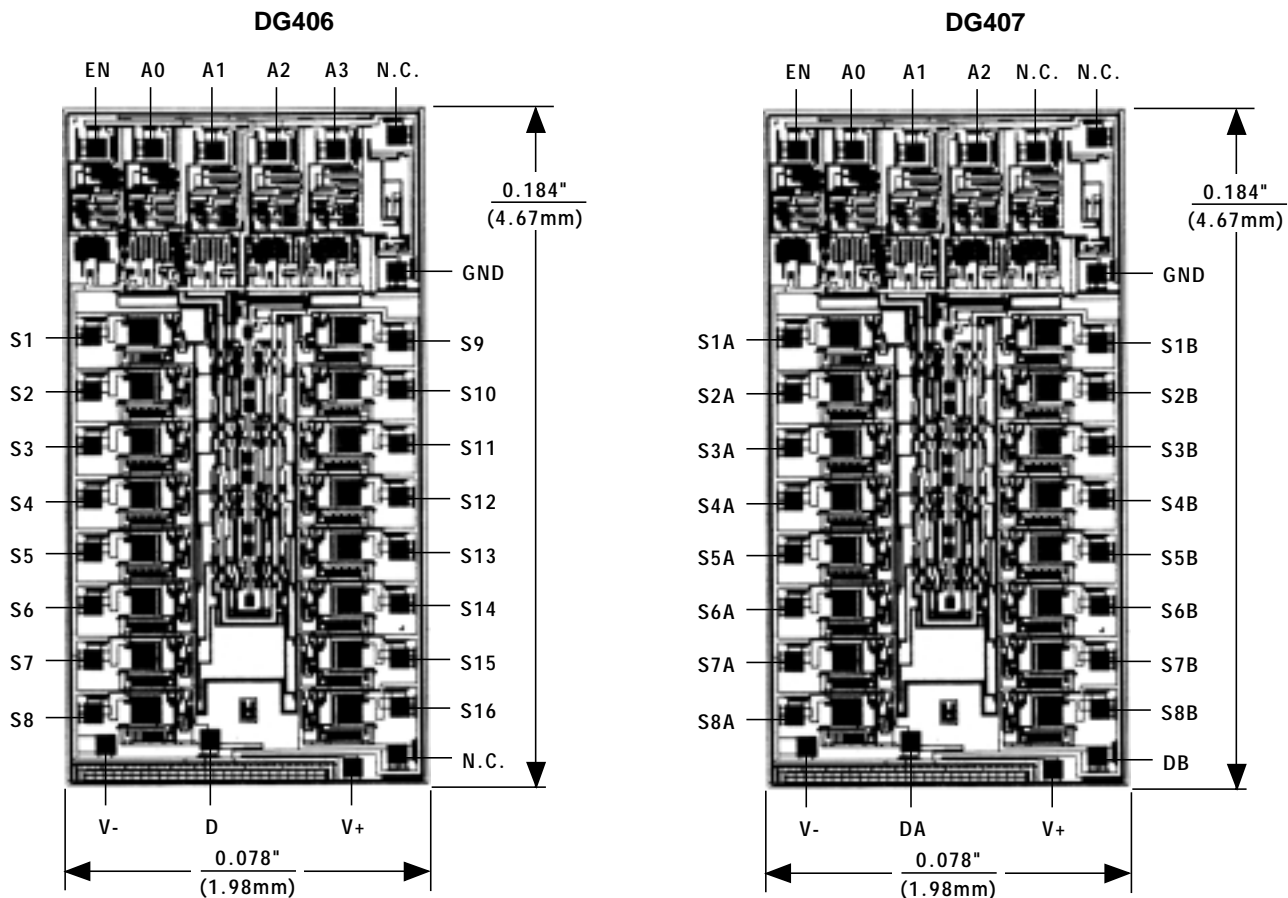
PART	TEMP. RANGE	PIN-PACKAGE
DG407CJ	0°C to +70°C	28 Plastic DIP
DG407CWI	0°C to +70°C	28 Wide SO
DG407C/D	0°C to +70°C	Dice*
DG407DJ	-40°C to +85°C	28 Plastic DIP
DG407DWI	-40°C to +85°C	28 Wide SO
DG407DN	-40°C to +85°C	28 PLCC
DG407AK	-55°C to +125°C	28 CERDIP

* Contact factory for dice specifications.

Improved, 16-Channel/Dual 8-Channel, CMOS Analog Multiplexers

Chip Topographies

DG406/DG407



N.C. = NO INTERNAL CONNECTION

TRANSISTOR COUNT: 269
SUBSTRATE IS INTERNALLY CONNECTED TO V+

TRANSISTOR COUNT: 269
SUBSTRATE IS INTERNALLY CONNECTED TO V+

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