

# CXK5B18120TM -12

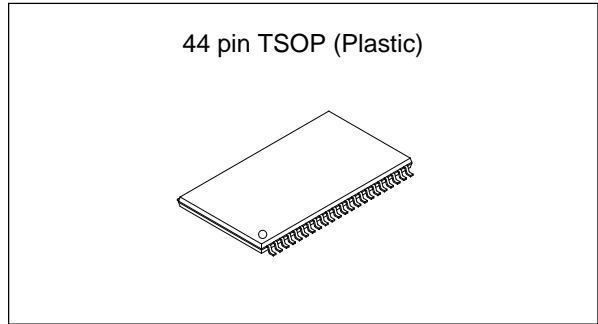
## 65536-word × 18-bit High Speed Bi-CMOS Static RAM

**Description**

CXK5B18120TM is a high speed 1M bit Bi-CMOS static RAM organized as 65536 words by 18 bits. Operating on a single 3.3V supply this asynchronous IC is suitable for use in high speed and low power applications.

**Features**

- Single 3.3V Supply     3.3V±0.3V
- Fast access time        12ns (Max.)
- Low stand-by current:    10mA (Max.)
- Low power operation    1116mW (Max.)
- Package line-up  
     Dual Vcc/Vss  
     CXK5B18120TM    400mil 44pin TSOP Package



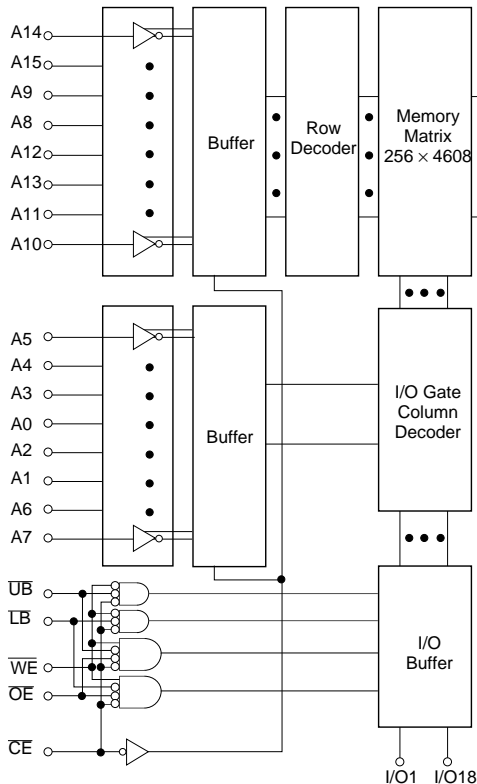
**Function**

65536-word × 18-bit static RAM

**Structure**

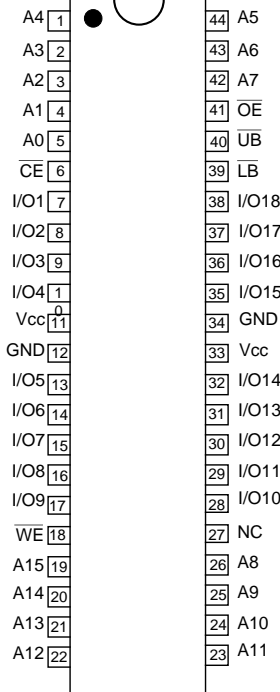
Silicon gate Bi-CMOS IC

**Block Diagram**



**Pin configuration**

(Top View)



**Pin Description**

Symbol	Description
A0 to A15	Address input
I/O1 to I/O9	Data input output (lower byte I/O)
I/O10 to I/O18	Data input output (upper byte I/O)
CE	Chip enable input
WE	Write enable input
OE	Output enable input
LB	Lower byte select input
UB	Upper byte select input
Vcc	+3.3V Power supply
GND	Ground
NC	No connection

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**Absolute Maximum Ratings**

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub>	-0.5* <sup>1</sup> to +4.6	V
Input voltage	V <sub>IN</sub>	-0.5* <sup>1</sup> to V <sub>CC</sub> + 0.5	V
Input and output voltage	V <sub>I/O</sub>	-0.5* <sup>1</sup> to V <sub>CC</sub> + 0.5	V
Allowable power dissipation	P <sub>D</sub>	1.5* <sup>2</sup>	W
Operating temperature	T <sub>opr</sub>	0 to +70	°C
Storage temperature	T <sub>stg</sub>	-55 to +150	°C
Soldering temperature • time	T <sub>solder</sub>	235 • 10	°C • sec

\*<sup>1</sup> V<sub>CC</sub>, V<sub>IN</sub>, V<sub>I/O</sub> = -2.0V Min. for pulse width less than 5ns\*<sup>2</sup> Air Flow ≥ 1m/s**Truth Table**

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O1 to I/O9	I/O10 to I/O18	Current
H	×	×	×	×	Not selected	High Z	High Z	I <sub>SB1</sub> , I <sub>SB2</sub>
L	L	H	L	L	Read	Data Out	Data out	I <sub>CC</sub>
			L	H	Read	Data Out	High Z	I <sub>CC</sub>
			H	L	Read	High Z	Data out	I <sub>CC</sub>
			H	H	Not selected	High Z	High Z	I <sub>CC</sub>
L	×	L	L	L	Write	Data in	Data in	I <sub>CC</sub>
			L	H	Write	Data in	High Z	I <sub>CC</sub>
			H	L	Write	High Z	Data in	I <sub>CC</sub>
L	H	H	×	×	Output disable	High Z	High Z	I <sub>CC</sub>
L	×	×	H	H	Not selected	High Z	High Z	I <sub>CC</sub>

×: "H" or "L"

**Recommended Operating Conditions**

(Ta = 0 to +70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V <sub>CC</sub>	3.0	3.3	3.6	V
Input high voltage	V <sub>IH</sub>	2.0	—	V <sub>CC</sub> + 0.3	V
Input low voltage	V <sub>IL</sub>	-0.3*	—	0.8	V

\* V<sub>IL</sub> = -2.0V Min. for pulse width less than 5ns

Electrical Characteristics

DC Characteristics

(Vcc = 3.3V±0.3V, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Conditions	Min.	Typ.*	Max.	Unit
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> = GND to V <sub>CC</sub>	-10	—	+10	μA
Output leakage current	I <sub>LO</sub>	$\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{UB} = V_{IH}$ or $\overline{LB} = V_{IH}$ V <sub>I/O</sub> = GND to V <sub>CC</sub>	-10	—	+10	μA
Average operating current	I <sub>CC</sub>	Min. Cycle Duty = 100% I <sub>OUT</sub> = 0mA, $\overline{CE} = V_{IL}$ , V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	—	—	310	mA
Standby current	I <sub>SB1</sub>	$\overline{CE} \geq V_{CC} - 0.2V$ V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V	—	—	10	mA
	I <sub>SB2</sub>	Min. Cycle Duty = 100% $\overline{CE} = V_{IH}$ , V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	—	—	100	mA
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -2.0mA	2.4	—	—	V
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2.0mA	—	—	0.4	V

\* Vcc = 3.3V, Ta = 25°C

I/O Capacitance

(Ta = 25°C, f = 1MHz)

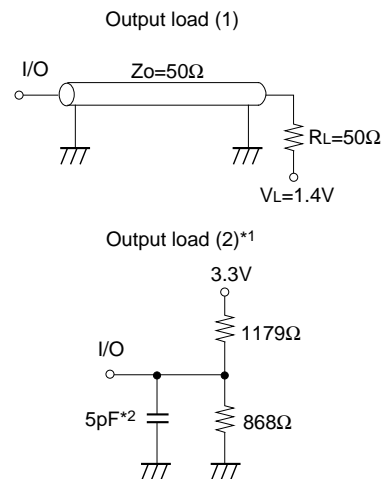
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0V	—	—	5	pF
I/O capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0V	—	—	7	pF

Note) This parameter is sampled and is not 100% tested.

AC Characteristics

• AC test condition (Vcc = 3.3V±0.3V, Ta = 0 to +70°C)

Item	Condition
Input pulse high level	V <sub>IH</sub> = 3.0V
Input pulse low level	V <sub>IL</sub> = 0.0V
Input rise time	t <sub>r</sub> = 2ns
Input fall time	t <sub>f</sub> = 2ns
Input and output reference level	1.4V
Output load conditions	Fig. 1



\*1. For tLZ, tOLZ, tLBLZ, tUBLZ, tHZ, tOHZ, tLBHZ, tUBHZ, tOW, tWHZ

\*2. Including scope and jig capacitances.

Fig. 1

• Read cycle

Item	Symbol	-12		Unit
		Min.	Max.	
Read cycle time	t <sub>RC</sub>	12	—	ns
Address access time	t <sub>AA</sub>	—	12	ns
Chip enable access time	t <sub>CO</sub>	—	12	ns
Output enable to output valid	t <sub>OE</sub>	—	6	ns
Byte select to output valid	t <sub>LB</sub> , t <sub>UB</sub>	—	6	ns
Output data hold time	t <sub>OH</sub>	3	—	ns
Chip enable to output in low Z ( $\overline{CE}$ )	t <sub>LZ</sub> *	3	—	ns
Output enable to output in low Z ( $\overline{OE}$ )	t <sub>OLZ</sub> *	0	—	ns
Byte select to output in low Z ( $\overline{LB}$ , $\overline{UB}$ )	t <sub>LBLZ</sub> , t <sub>UBLZ</sub> *	0	—	ns
Chip disable to output in high Z ( $\overline{CE}$ )	t <sub>HZ</sub> *	0	6	ns
Output disable to output in high Z ( $\overline{OE}$ )	t <sub>OHZ</sub> *	0	6	ns
Byte select to output in high Z ( $\overline{LB}$ , $\overline{UB}$ )	t <sub>LBHZ</sub> , t <sub>UBHZ</sub> *	0	6	ns

\* Transition is measured ±200mV from steady voltage with specified loading in Fig. 1-(2).  
This parameter is sampled and is not 100% tested.

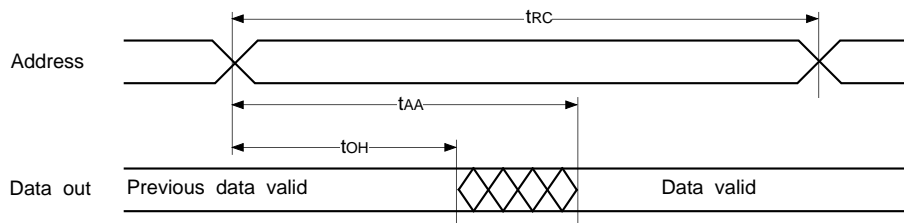
• Write cycle

Item	Symbol	-12		Unit
		Min.	Max.	
Write cycle time	t <sub>WC</sub>	12	—	ns
Address valid to end of write	t <sub>AW</sub>	10	—	ns
Chip enable to end of write	t <sub>CW</sub>	10	—	ns
Byte select to end of write	t <sub>LBW</sub> , t <sub>UBW</sub>	10	—	ns
Data valid to end to write	t <sub>DW</sub>	8	—	ns
Data hold from end of write	t <sub>DH</sub>	0	—	ns
Write pulse width	t <sub>WP</sub>	10	—	ns
Address set up time	t <sub>AS</sub>	0	—	ns
Write recovery time	t <sub>WR</sub>	0	—	ns
Output active from end of write	t <sub>OW</sub> *	4	—	ns
Write to output in high Z	t <sub>WHZ</sub> *	0	6	ns

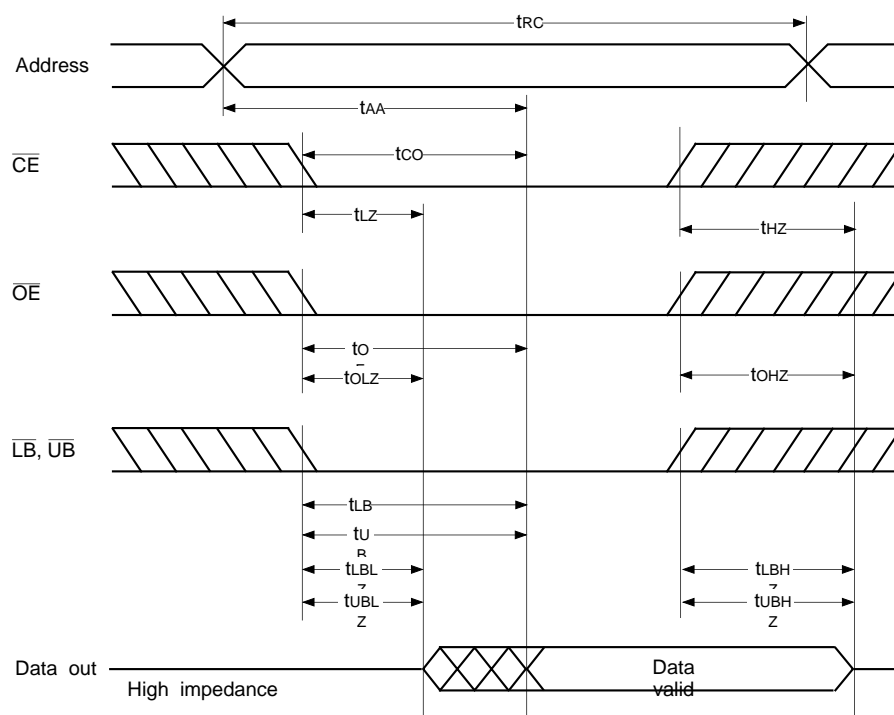
\* Transition is measured ±200mV from steady voltage with specified loading in Fig. 1-(2).  
This parameter is sampled and is not 100% tested.

Timing Waveform

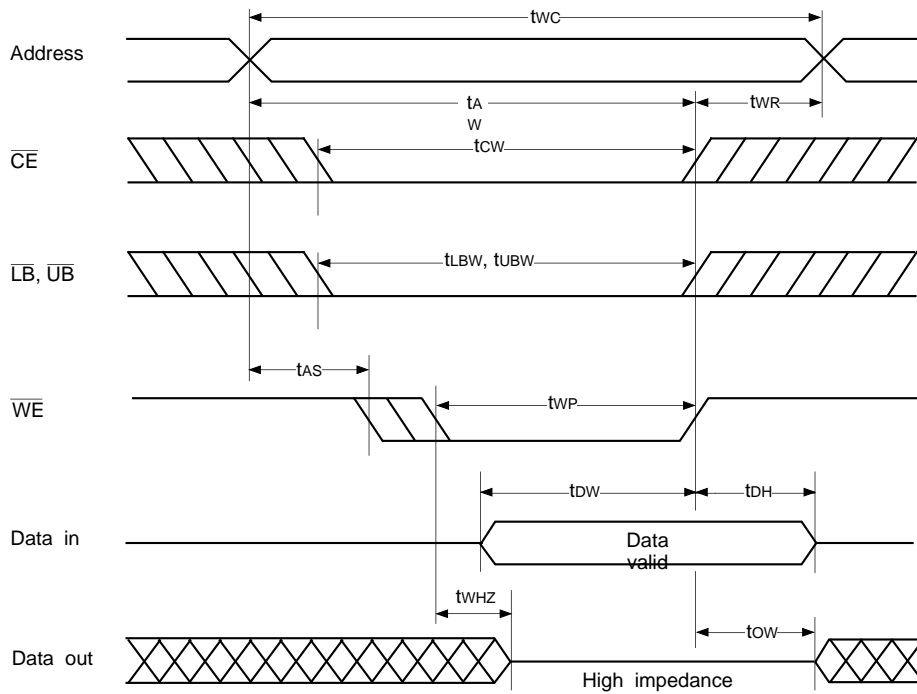
- Read cycle (1) :  $\overline{CE} = \overline{OE} = V_{IL}$ ,  $\overline{WE} = V_{IH}$



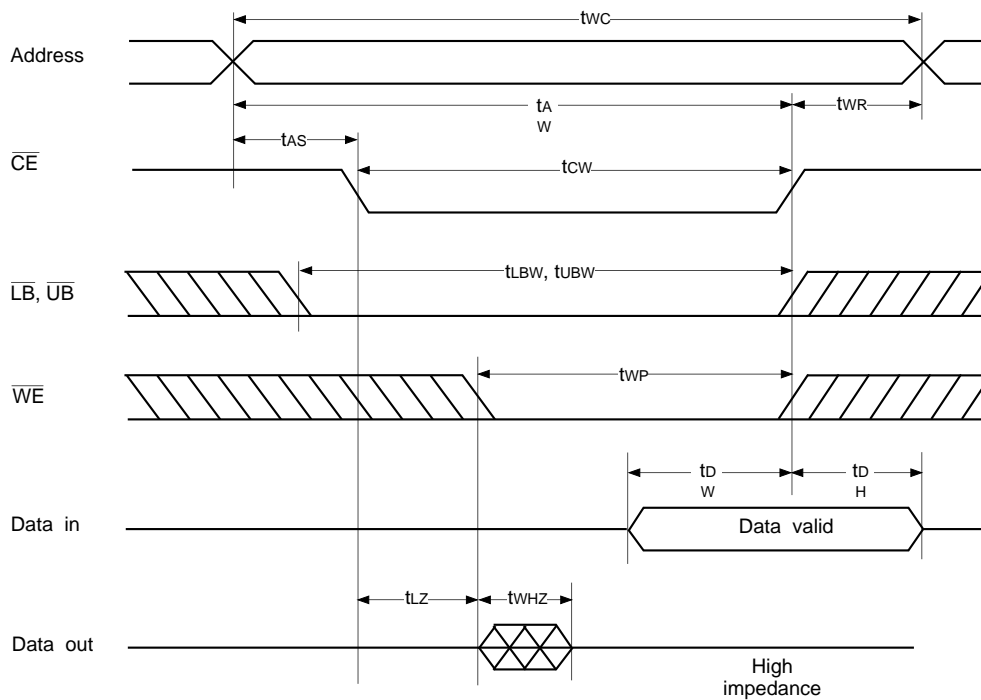
- Read cycle (2) :  $\overline{WE} = V_{IH}$



• Write cycle (1) : WE control

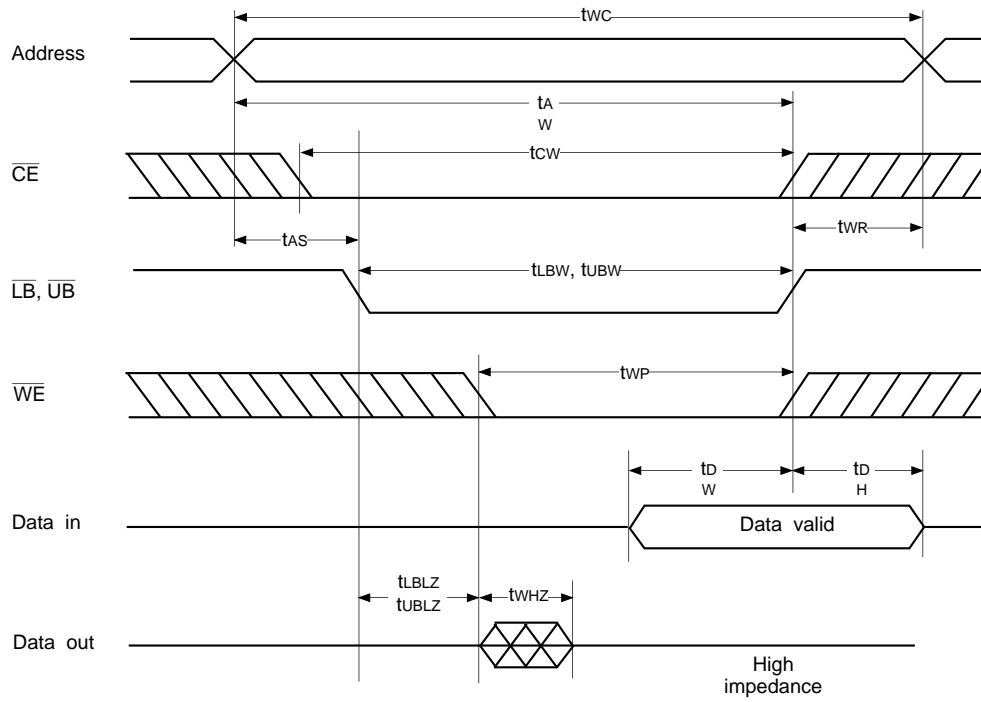


• Write cycle (2) :  $\overline{CE}$  control



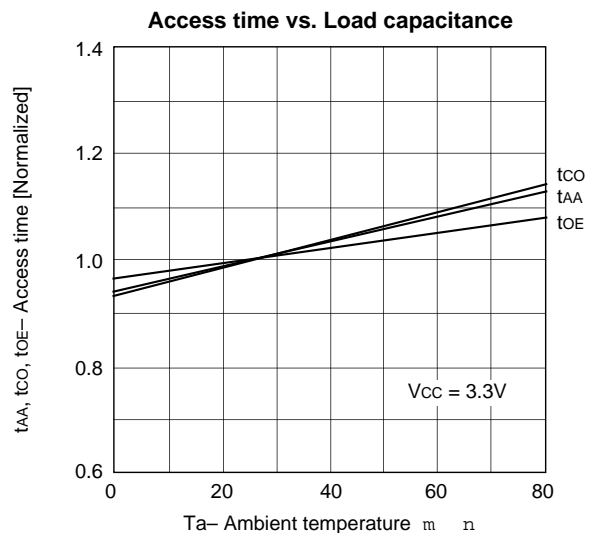
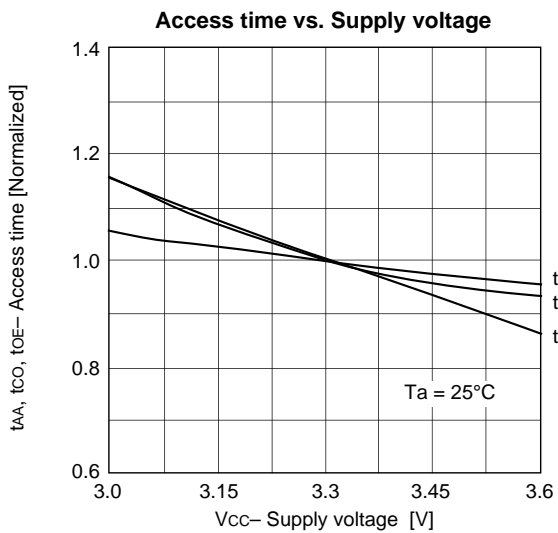
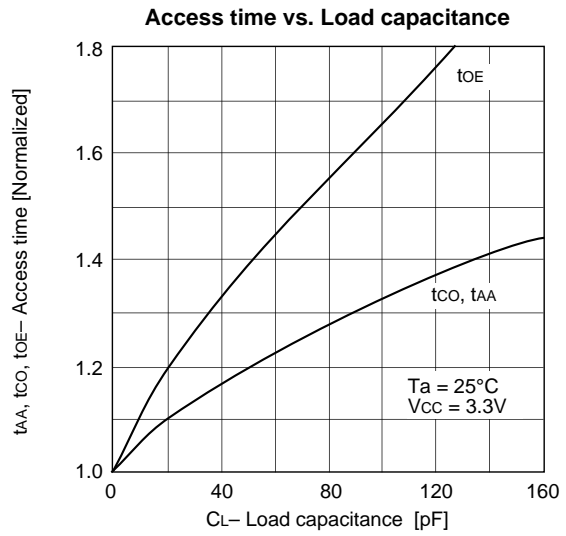
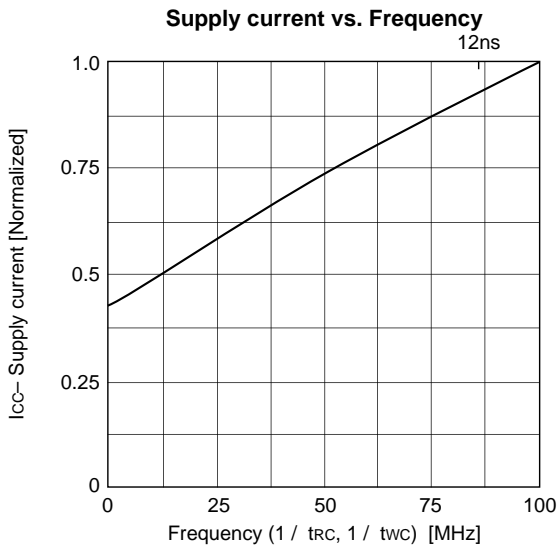
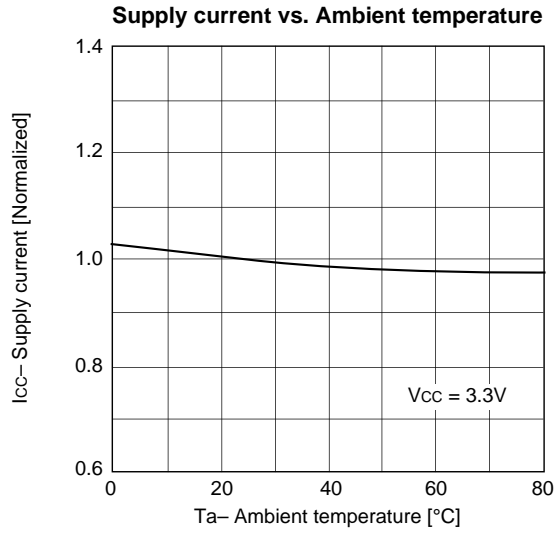
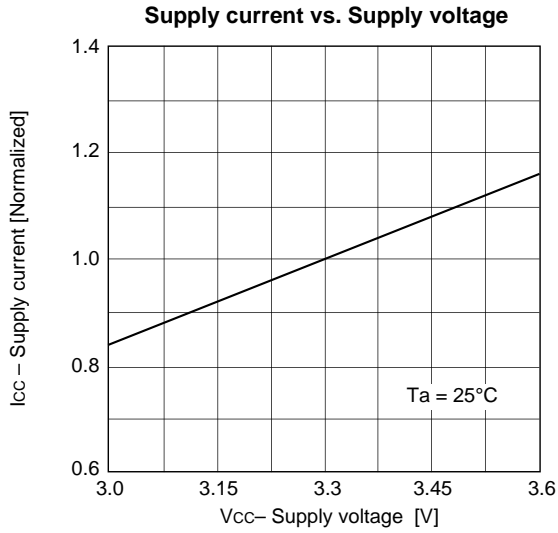
\* Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.

• Write cycle (3) : LB, UB control

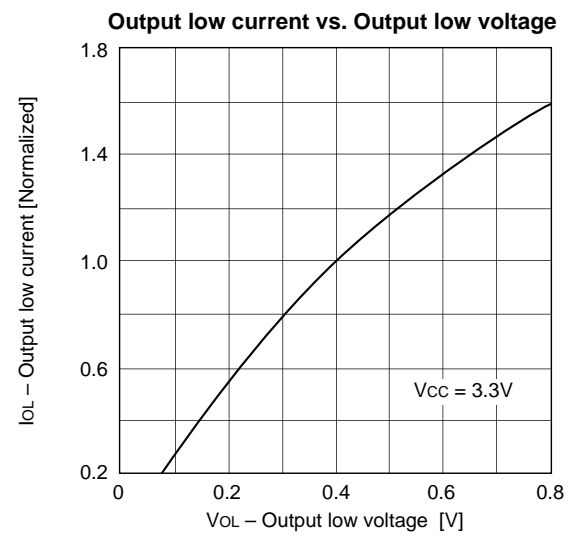
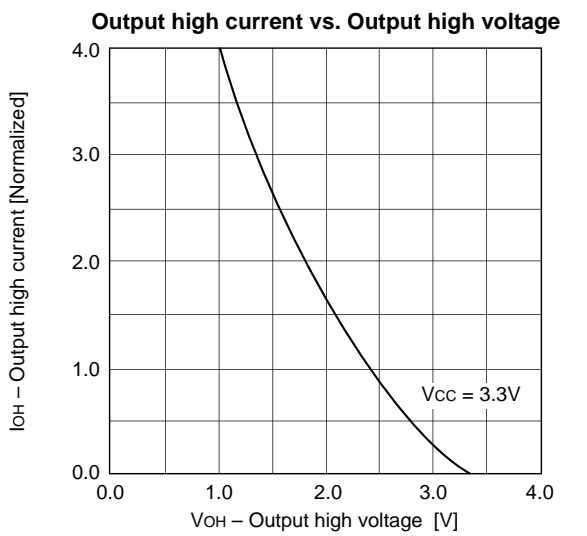
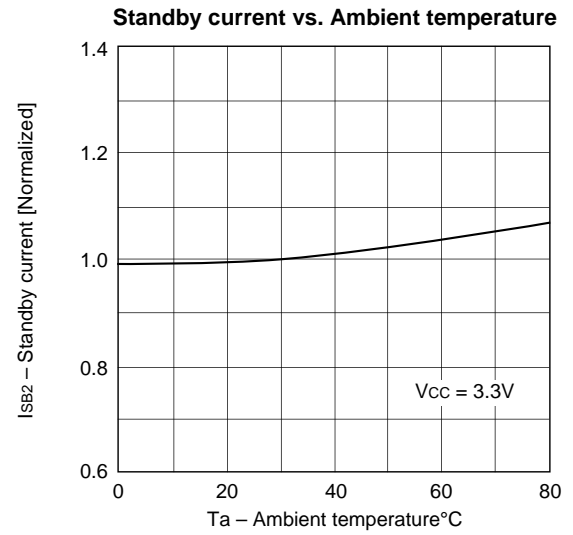
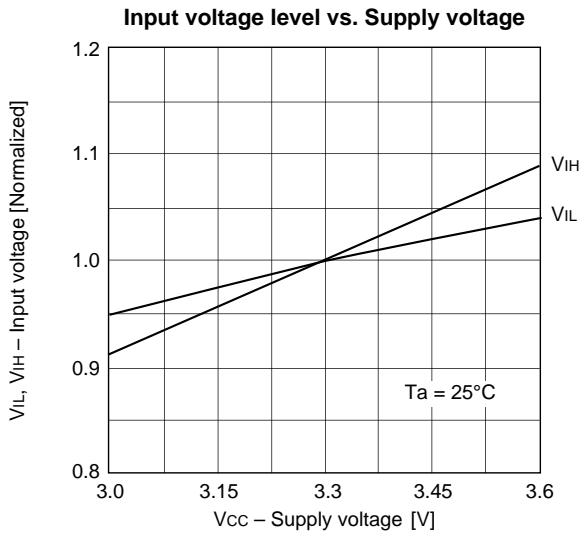
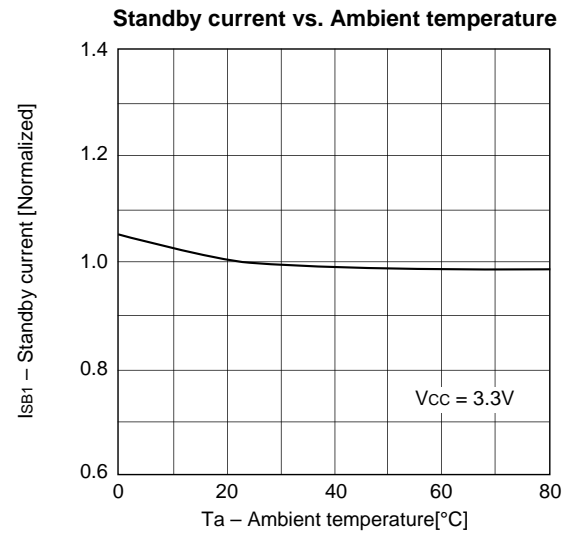
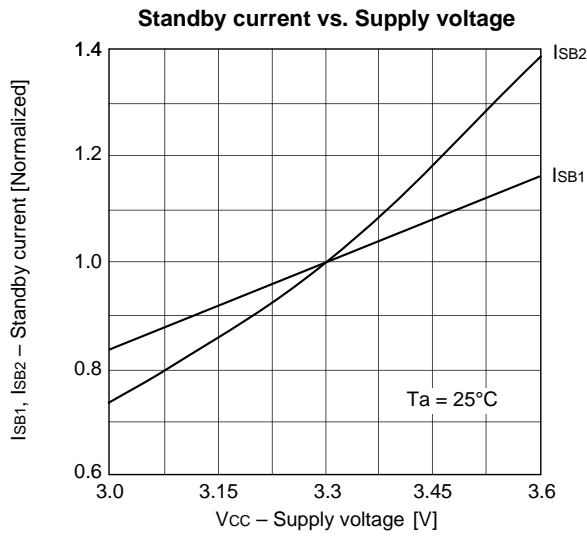


\* Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.

Example of Representative Characteristics

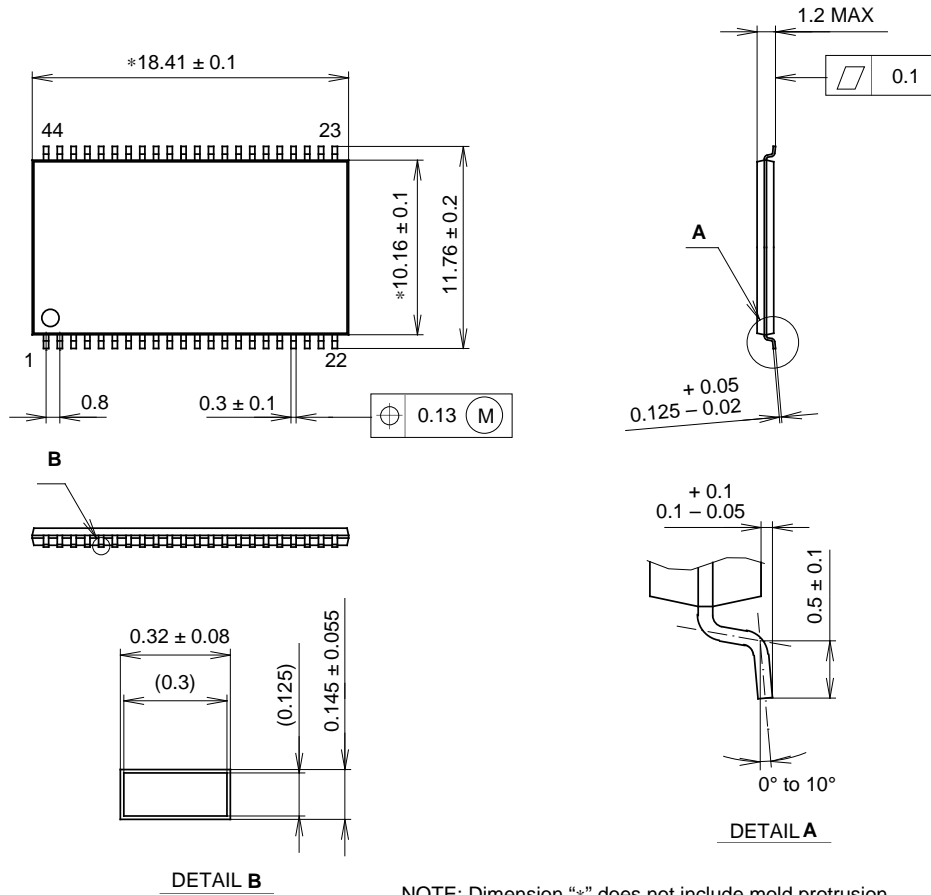






Package Outline Unit: mm

44PIN TSOP (II) (PLASTIC) 400mil



NOTE: Dimension "\*" does not include mold protrusion.

PACKAGE STRUCTURE

SONY CODE	TSOP (II) -44P-L01
EIAJ CODE	TSOP (II) 044-P-0400-A
JEDEC CODE	—

MOLDING COMPOUND	EPOXY / PHENOL RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.5g