SONY

CXD1172AM/AP

6-bit 20MSPS Video A/D Converter (CMOS)

Description

CXD1172AM/AP is a 6-bit CMOS A/D converter for video use. The adoption of a 2-step parallel system achieves low consumption at a maximum conversion speed of 20MSPS minimum, 35MSPS typical.

Features

- Resolution: 6-bit ± 1/2LSB
- Max. sampling frequency: 20MSPS
- Low power consumption: 40mW (at 20MSPS typ.)
  (Reference current excluded)
- Built-in sampling and hold circuit.
- 3-state TTL compatible output.
- Power supply: 5V single
- Low input capacitance: 4pF
- Reference impedance: 250Ω (typ.)

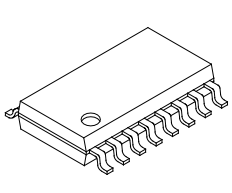
Applications

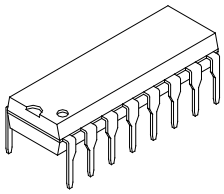
TV, VCR digital systems and a wide range of fields where high speed A/D conversion is required.

Structure

Silicon gate CMOS monolithic IC

CXD1172AM	CXD1172AP
16 pin SOP (Plastic)	16 pin DIP (Plastic)





Absolute Maximum Ratings (Ta = 25°C)

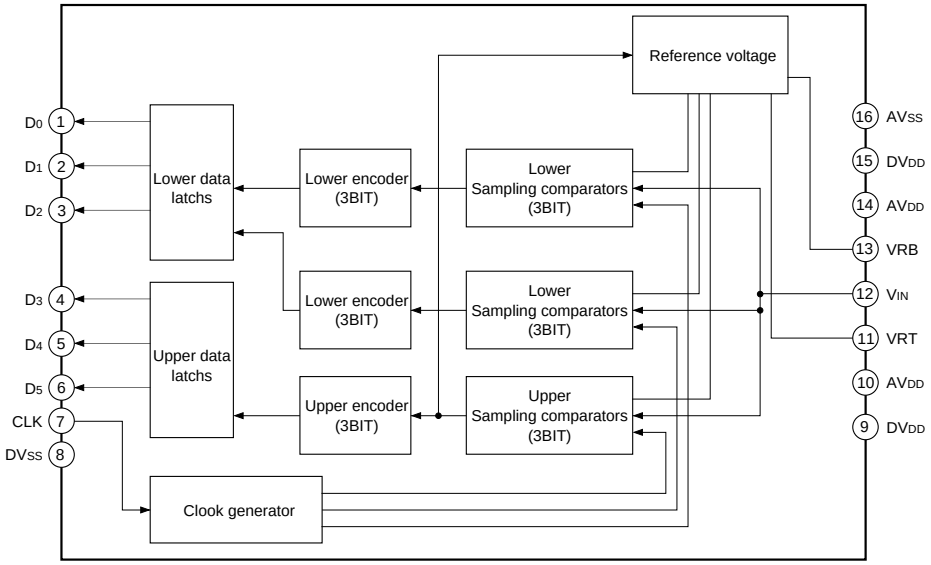
• Supply voltage	V_{DD}	7	V
• Reference voltage	V_{RT}, V_{RB}	V_{DD} + 0.5 to V_{SS} – 0.5	V
• Input voltage (Analog)	V_{IN}	V_{DD} + 0.5 to V_{SS} – 0.5	V
• Input voltage (Digital)	V_{CLK}	V_{DD} + 0.5 to V_{SS} – 0.5	V
• Output voltage (Digital)	V_{OH}, V_{OL}	V_{DD} + 0.5 to V_{SS} – 0.5	V
• Storage temperature	Tstg	–55 to +150	°C

Recommended Operating Conditions

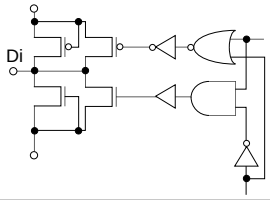
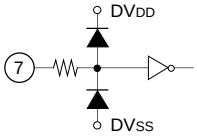
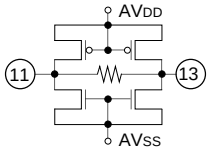
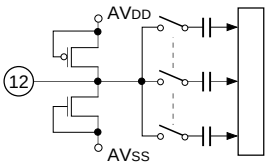
• Supply voltage	AV_{DD}, AV_{SS}	4.75 to 5.25	V
	DV_{DD}, DV_{SS}	4.75 to 5.25	V
• Reference input voltage	V_{RB}	0 to 4.1	V
	V_{RT}	0.9 to 5.0	V
	V_{RT} – V_{RB}	0.9 to AV_{DD}	V
• Analog input voltage	V_{IN}	V_{RB} to V_{RT}	V
• Clock pulse width	T_{PW1}, T_{PW0}	23ns (min.) to 1.1µs (max.)	
• Operating temperature	Topr	–20 to +75	°C

E89320C78-PS

Block Diagram and Pin Configuration



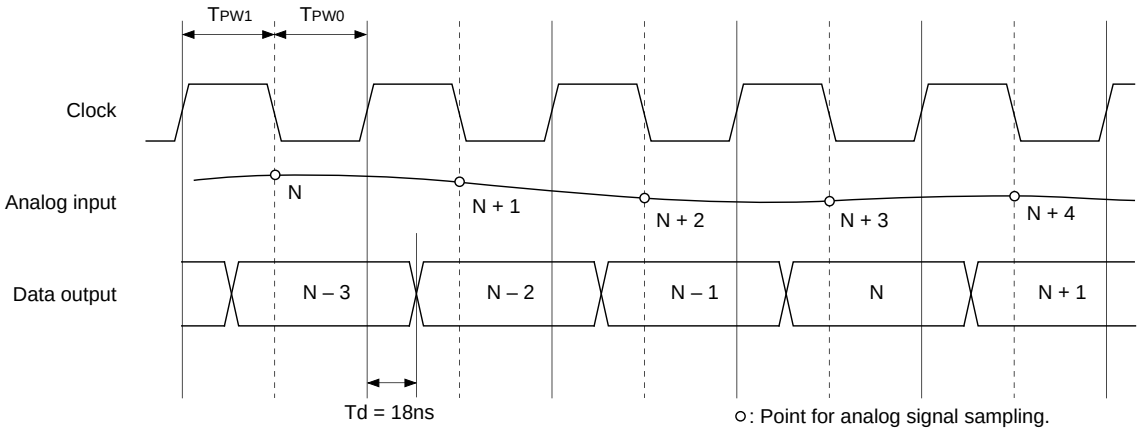
PIn Description and Equivalent Circuits

No.	Symbol	Equivalent Circuit	Description
1 to 6	D_0 to D_5		D_0 (LSB) to D_5 (MSB) output
7	CLK		Clock input
8	DV_{SS}		Digital GND
9, 15	DV_{DD}		Digital +5V
10, 14	AV_{DD}		Analog +5V
11	VRT		Reference voltage (Top)
13	VRB		Reference voltage (Bottom)
12	V_{IN}		Analog input
16	AV_{SS}		Analog GND

Digital Output

Compatibility between Analog input voltage and the digital output code is indicated in the chart below.

Input signal voltage	Step	Digital output code MSB LSB
V_{RT}	0	1 1 1 1 1 1
⋮	⋮	⋮
	31	1 0 0 0 0 0
	32	0 1 1 1 1 1
⋮	⋮	⋮
V_{RB}	63	0 0 0 0 0 0



Timing Chart 1

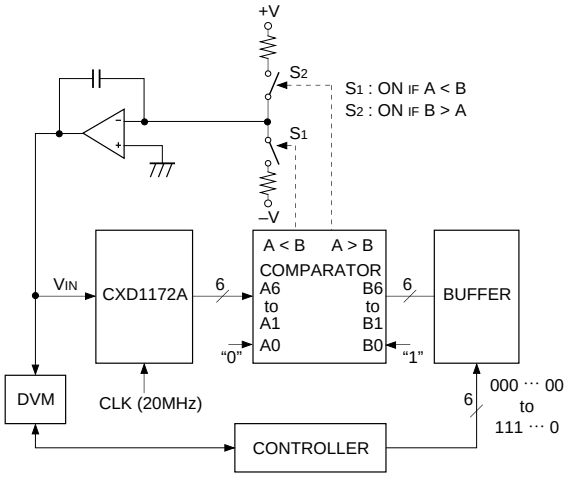
Electrical Characteristics (V_{DD} = 5V, V_{RB} = 1.0V, V_{RT} = 2.0V, Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Conversion speed	Fc	V_{DD} = 4.75 to 5.25V Ta = –20 to +75°C V_{IN} = 1.0 to 2.0V f_{IN} = 1kHz ramp	0.5		20	MSPS
Supply current	I_{DD}	Fc = 20MSPS NTSC ramp wave input		7	12	mA
Reference pin current	I_{REF}		3	4	5.7	
Analog input band width (–1dB)	BW	Envelope		18		MHz
Analog input capacitance	C_{IN}	V_{IN} = 1.5V + 0.07Vrms		4		pF
Reference resistance (V_{RT} to V_{RB})	R_{REF}		175	250	325	Ω
Offset voltage*1	E_{OT}	Potential difference to VRT	0	–20	–40	mV
	E_{OB}	Potential difference to VRB	15	35	55	
Digital input voltage	V_{IH}	V_{DD} = 4.75 to 5.25V Ta = –20 to +75°C	4.0			V
	V_{IL}				1.0	
Digital input current	I_{IH}	V_{DD} = max. V_{IH} = V_{DD}			5	μA
	I_{IL}	V_{IL} = 0V			5	
Digital output current	I_{OH}	V_{DD} = min. V_{OH} = V_{DD} + 0.5V	–1.1			mA
	I_{OL}	V_{OL} = 0.4V	3.7			
Output data delay	T_{DL}	With TTL 1 gate and 10pF load Ta = –20 to +75°C V_{DD} = 4.75 to 5.25V		18	30	ns
Integral non-linearity error	E_L	End point		±0.3	±0.5	LSB
Differential non-linearity error	E_D			±0.3	±0.5	
Differential gain error	DG	NTSC 40 IRE mod ramp Fc = 14.3MSPS		1.0		%
Differential phase error	DP			1.0		deg
Aperture jitter	Taj			40		ps
Sampling delay	Tsd			4		ns

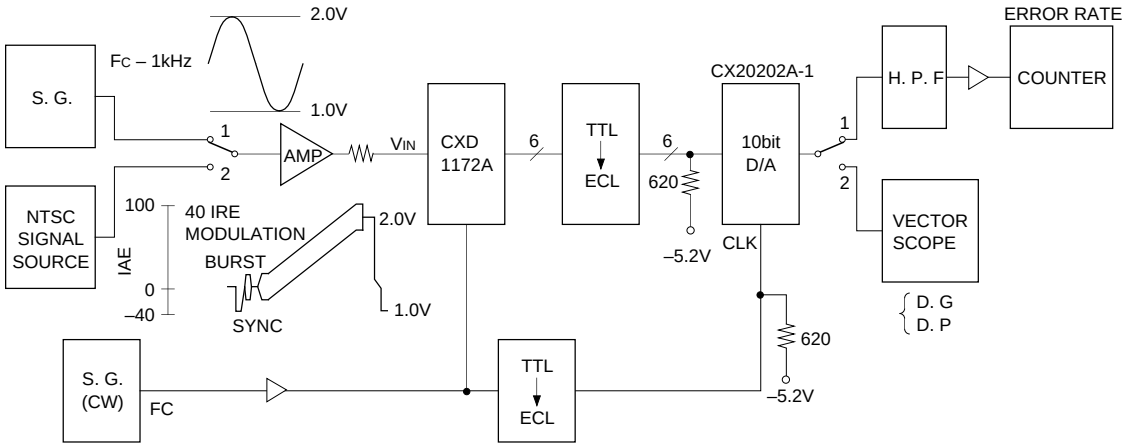
*1 The offset voltage EOB is a potential difference between VRB and a point of position where the voltage drops equivalent to 1/2 LSB of the voltage when the output data changes from "00000000" to "00000001". EOT is a potential difference between VRT and a potential of point where the voltage rises equivalent to 1/2 LSB of the voltage when the output data changes from "11111111" to "11111110".

Electrical Characteristics Test Circuit

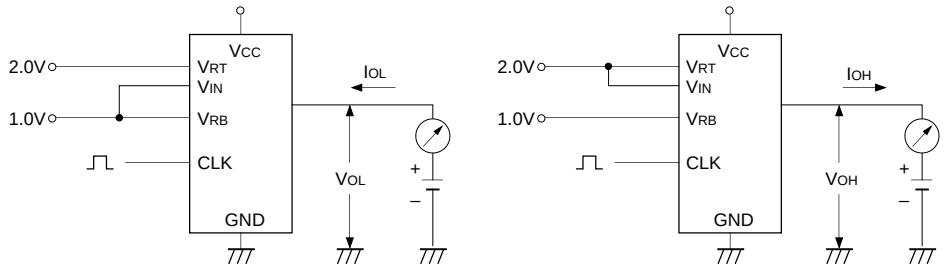
Integral non-linearity error
Differential non-linearity } **Test Circuit**
Offset voltage



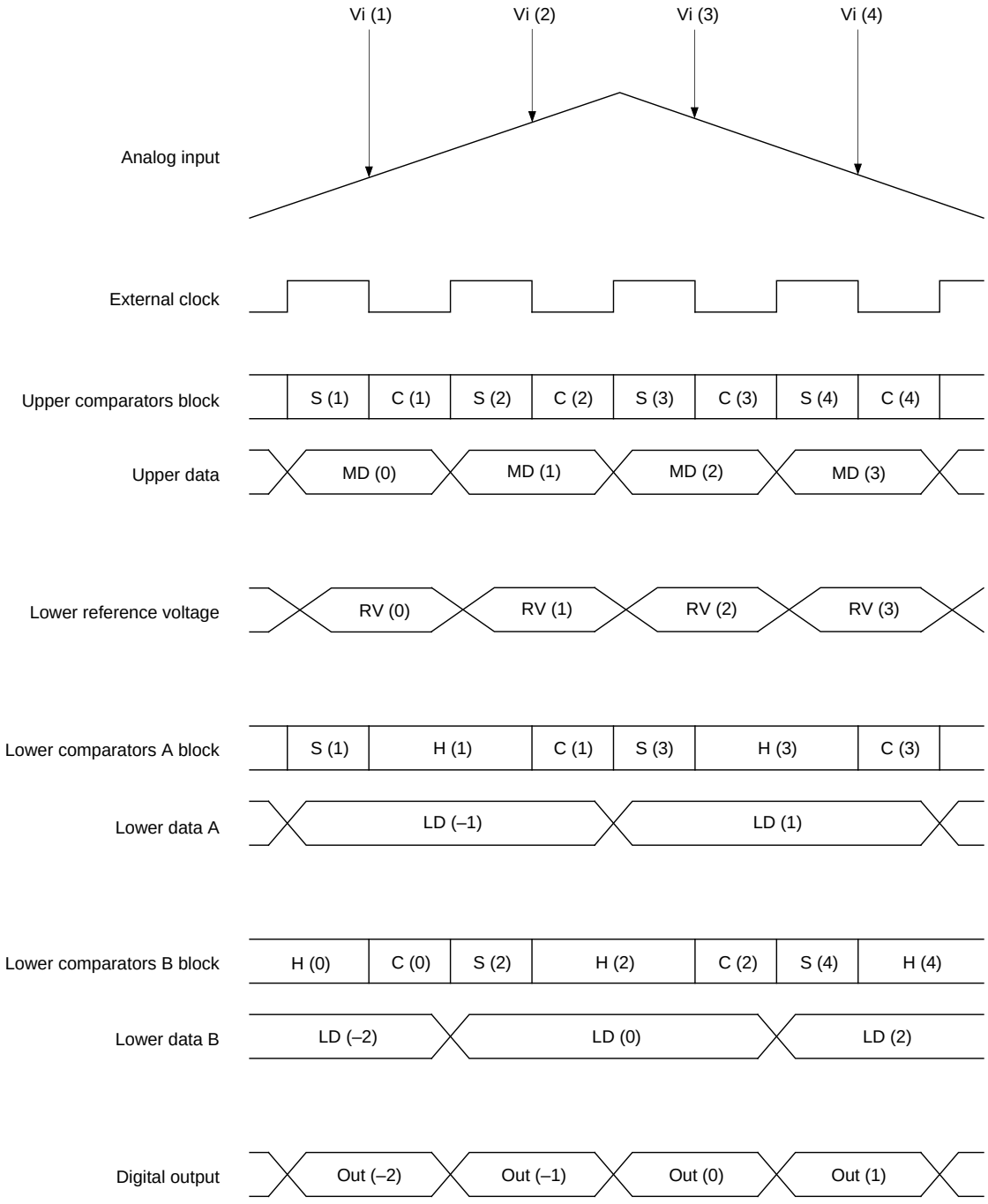
Maximum operational speed
Differential gain error } **Test Circuit**
Differential phase error



Digital output current test circuit



Timing Chart 2



Operation (See Block Diagram and Timing Chart)

1. CXD1172AM/AP is a 2-step parallel system A/D converter featuring a 3-bit upper comparators group and 2 lower comparators groups of 3-bit each. The reference voltage that is equal to the voltage between VRT-VRB/8 is constantly applied to the upper 3-bit comparator block. Voltage that corresponded to the upper data is fed through the reference supply to the lower data.

2. This IC uses an offset cancel type comparator and operates synchronously with an external clock. It features the following operating modes which are respectively indicated on the timing chart with S, H, C symbols. That is input sampling (auto zero) mode, input hold mode and comparison mode.

3. The operation of respective parts is as indicated in the chart. For instance input voltage Vi (1) is sampled with the falling edge of the first clock by means of the upper comparator block and the lower comparator A block.
   The upper comparators block finalizes comparison data MD (1) with the rising edge of the first clock. Simultaneously the reference supply generates the lower reference voltage RV (1) that corresponded to the upper results. The lower comparator block finalizes comparison data LD (1) with the rising edge of the second clock. MD (1) and LD (1) are combined and output as Out (1) with the rising edge of the 3rd clock. Accordingly there is a 2.5 clock delay from the analog input sampling point to the digital data output.

Operation Notes

1. V_{DD}, Vss
   To reduce noise effects, separate the analog and digital systems close to the device. For both the digital and analog V_{DD} pins, use a ceramic capacitor of about 0.1µF set as close as possible to the pin to bypass to the respective GND's.

2. Analog input
   Compared with the flash type A/D converter, the input capacitance of the analog input is rather small. However it is necessary to conduct the drive with an amplifier featuring sufficient band and drive capability. When driving with an amplifier of low output impedance, parasite oscillation may occur. That may be prevented by inserting a resistance of about 100Ω in series between the amplifier output and A/D input.

3. Clock input
   The clock line wiring should be as short as possible also, to avoid any interference with other signals, separate it from other circuits.

4. Reference input
   Voltage between VRT to VRB is compatible with the dynamic range of the analog input. Bypassing VRT and VRB pins to GND, by means of a capacitor about 0.1µF, stable characteristics are obtained.

5. Timing
   Analog input is sampled with the falling edge of CLK and output as digital data with a delay of 2.5 clocks and with the following rising edge. The delay from the clock rising edge to the data output is about 18ns.

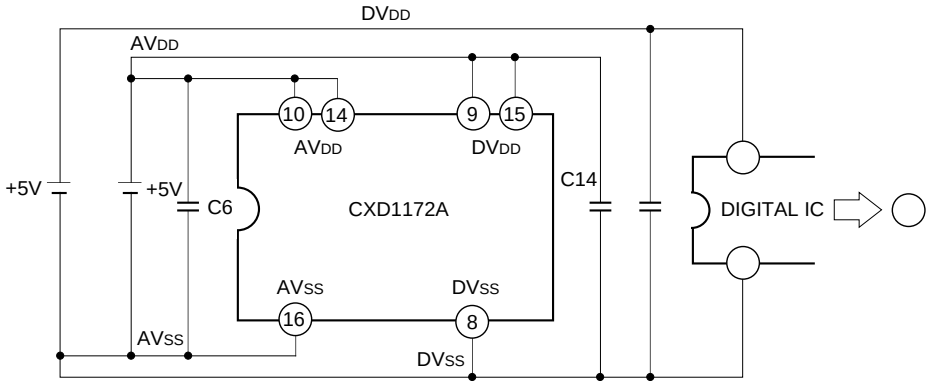
6. About latch up
   It is necessary that AV_{DD} and DV_{DD} pins be the common source of power supply.
   This is to avoid latch up due to the voltage difference between AV_{DD} and DV_{DD} pins when power is ON.
   See "For latch up prevention" of CXD1172P/CXA1106P PCB description. (Page 6, 7)

Latch Up Prevention

The CXD1172A is a CMOS IC which requires latch up precautions. Latch up is mainly generated by the lag in the voltage rising time of AV_{DD} (Pins 10 and 14) and DV_{DD} (Pins 9 and 15), when power supply is ON.

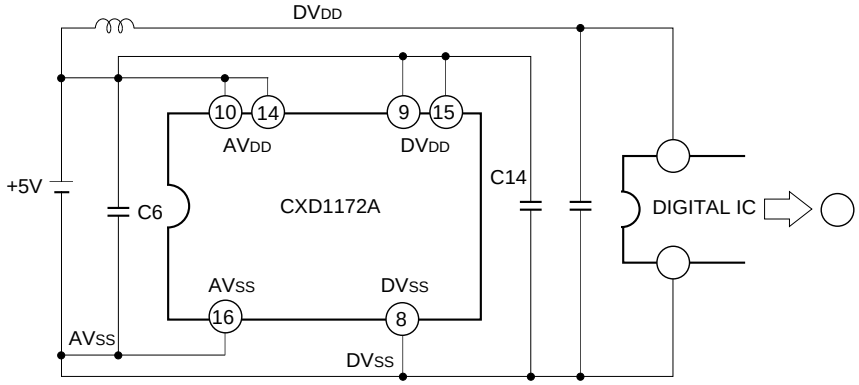
1. Correct usage

a. When analog and digital supplies are from different sources

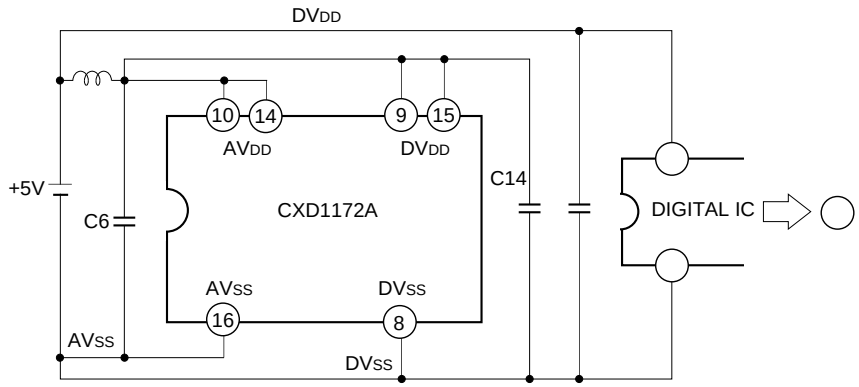


b. When analog and digital supplies are from a common source

(i)

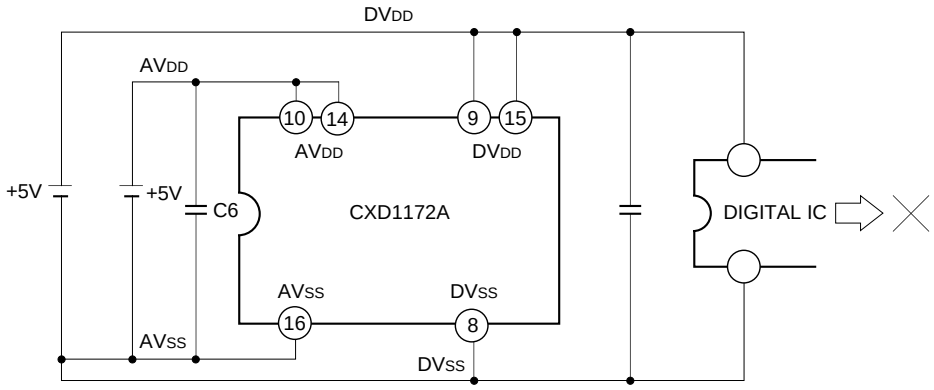


(ii)



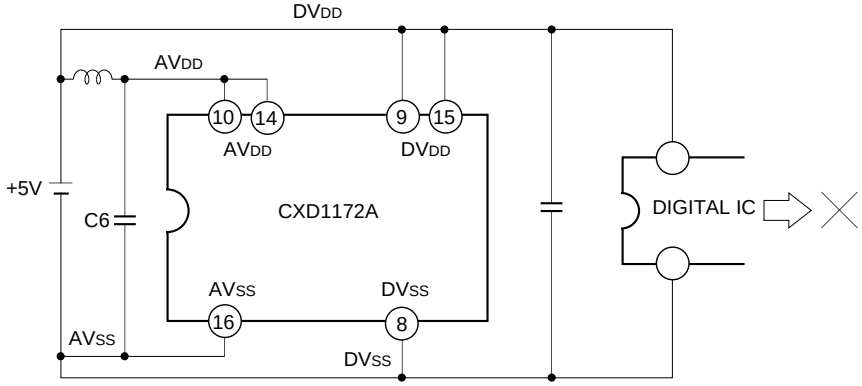
2. Example when latch up easily occurs

a. When analog and digital supplies are from different sources

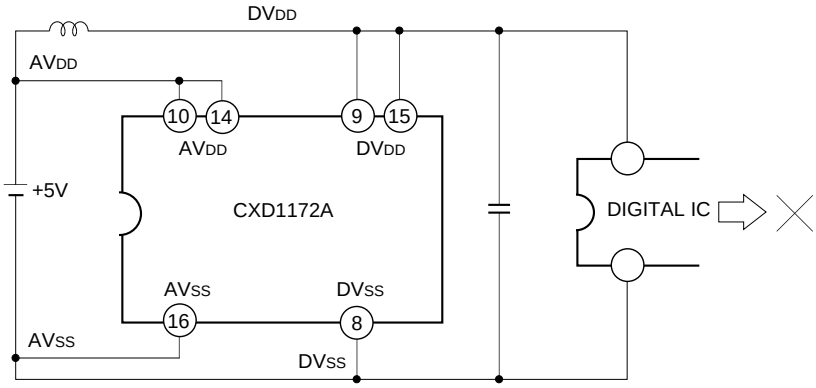


b. When analog and digital supplies are from common source

(i)

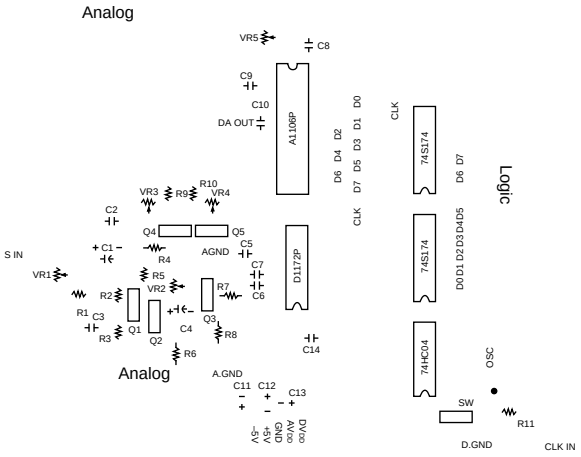


(ii)

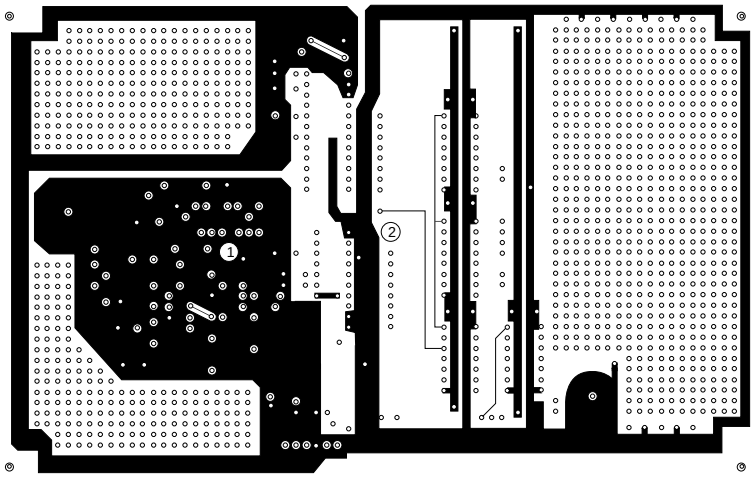


6-bit, 20MSPS ADC and DAC Evaluation Board

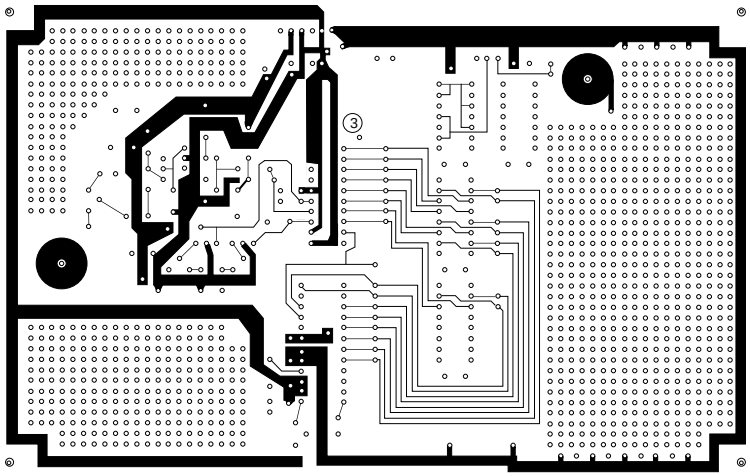
Silk Side



Component Side



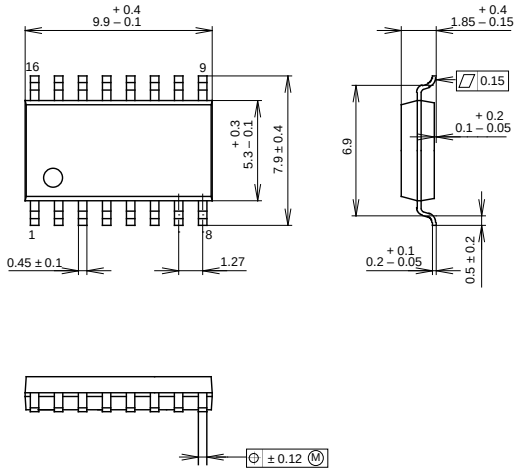
Soldering Side



Package Outline Unit: mm

CXD1172AM

16PIN SOP (PLASTIC) 300mil



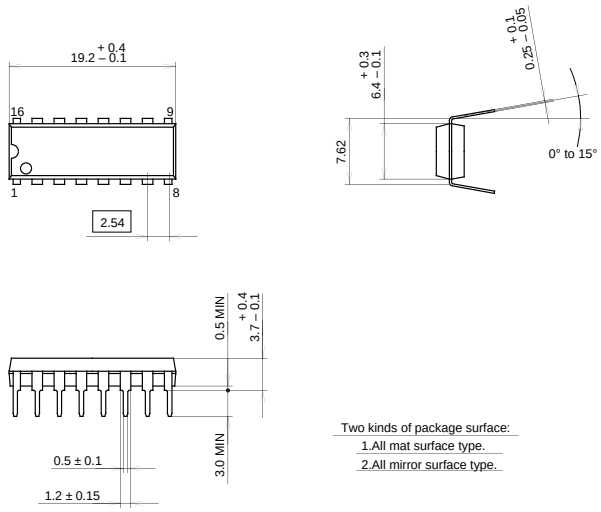
PACKAGE STRUCTURE

SONY CODE	SOP-16P-L01
EIAJ CODE	*SOP016-P-0300-A
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE WEIGHT	0.2g

CXD1172AP

16PIN DIP (PLASTIC)



Two kinds of package surface:
1.All mat surface type.
2.All mirror surface type.

PACKAGE STRUCTURE

SONY CODE	DIP-16P-01
EIAJ CODE	DIP016-P-0300
JEDEC CODE	Similar to MO-001-AE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	1.0 g