

# Addressable relay driver

# NE/SA5090

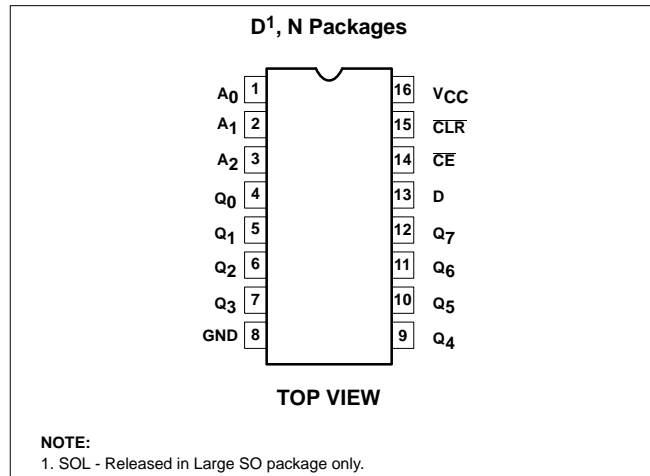
## DESCRIPTION

The NE/SA5090 addressable relay driver is a high-current latched driver, similar in function to the 9934 address decoder. The device has 8 open-collector Darlington power outputs, each capable of 150mA load current. The outputs are turned on or off by respectively loading a logic "1" or logic "0" into the device data input. The required output is defined by a 3-bit address. The device must be enabled by a  $\overline{CE}$  input line which also serves the function of further address decoding. A common clear input, CLR, turns all outputs off when a logic "0" is applied. The device is packaged in a 16-pin plastic or Cerdip package.

## FEATURES

- 8 high-current outputs
- Low-loading bus-compatible inputs
- Power-on clear ensures safe operation
- Will operate in addressable or demultiplex mode
- Allows random (addressed) data entry
- Easily expandable
- Pin-compatible with 9334 (Siliconix or Fairchild)

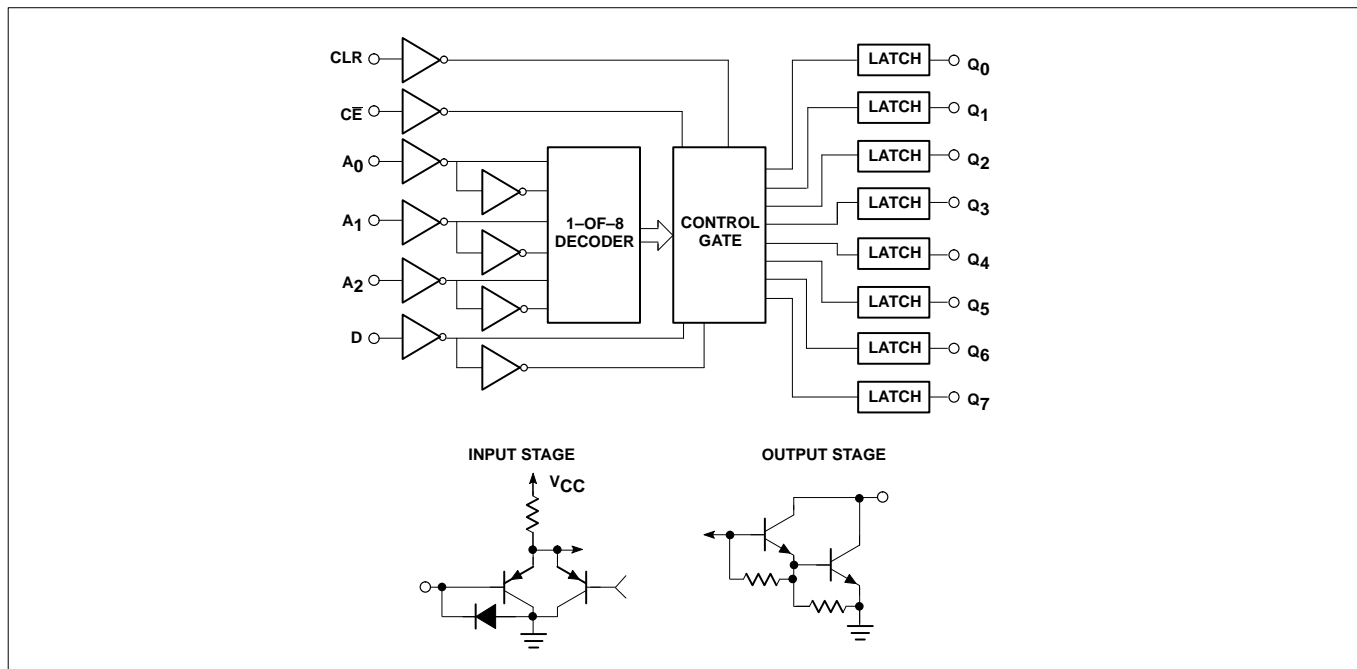
## PIN CONFIGURATION



## APPLICATIONS

- Relay driver
- Indicator lamp driver
- Triac trigger
- LED display digit driver
- Stepper motor driver

## BLOCK DIAGRAM



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## PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION
1-3	A <sub>0</sub> -A <sub>2</sub>	A 3-bit binary address on these pins defines which of the 8 output latches is to receive the data.
4-7, 9-12	Q <sub>0</sub> -Q <sub>7</sub>	The 8 device outputs.
13	D	The data input. When the chip is enabled, this data bit is transferred to the defined output such that: "1" turns output switch "ON" "0" turns output switch "OFF"
14	CE	The chip enable. When this input is low, the output latches will accept data. When CE goes high, all outputs will retain their existing state, regardless of address of data input condition.
15	CLR	The clear input. When CLR goes low all output switches are turned "OFF". The high data input will override the clear function on the addressed latch.

## ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Small Outline Large (SOL) Package	0 to +70°C	NE5090D	0171B
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5090N	0406C
16-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA5090N	0406C
16-Pin Plastic Small Outline Large (SOL) Package	-40 to +85°C	SA5090D	0171B

## TRUTH TABLE

INPUTS						OUTPUTS								MODE	
CL	C	D	A	A	A	Q	Q	Q	Q	Q	Q	Q	Q	Q	
R	E	0	1	2		0	1	2	3	4	5	6	7		
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	Clear
L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	Demultiplex
L	L	H	L	L	L	L	H	H	H	H	H	H	H		
L	L	L	H	L	L	H	H	H	H	H	H	H	H		
L	L	H	H	L	L	H	L	H	H	H	H	H	H		
L	L	L	H	H	H	H	H	H	H	H	H	H	H		
L	L	H	H	H	H	H	H	H	H	H	H	H	L		
H	H	X	X	X	X	Q <sub>N-1</sub>	—————>							Memory	
H	L	L	L	L	L	H	Q <sub>N-1</sub>	—————>							Addressable Latch
H	L	H	L	L	L	L	Q <sub>N-1</sub>	—————>							
H	L	L	H	L	L	Q <sub>N-1</sub>	H	Q <sub>N-1</sub>	—————>						
H	L	H	H	L	L	Q <sub>N-1</sub>	L	Q <sub>N-1</sub>	—————>						
H	L	L	H	H	H	Q <sub>N-1</sub>	—————>							H	
H	L	H	H	H	H	Q <sub>N-1</sub>	—————>							L	

### NOTES:

X=Don't care condition

Q<sub>N-1</sub>=Previous output state

L=Low voltage level/"ON" output state

H=High voltage level/"OFF" output state

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**ABSOLUTE MAXIMUM RATINGS** $T_A=25^{\circ}\text{C}$ , unless otherwise specified.

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}$	Supply voltage	-0.5 to +7	V
$V_{IN}$	Input voltage	-0.5 to +15	V
$V_{OUT}$	Output voltage	0 to +30	V
$I_{GND}$	Ground current	500	mA
$I_{OUT}$	Output current Each output	200	mA
$P_D$	Maximum power dissipation, $T_A=25^{\circ}\text{C}$ (still-air) <sup>1</sup> N package D package	1712 1315	mW mW
$T_A$	Ambient temperature range	0 to +70	$^{\circ}\text{C}$
$T_J$	Junction temperature	150	$^{\circ}\text{C}$
$T_{STG}$	Storage temperature range	-65 to +150	$^{\circ}\text{C}$
$T_{SOLD}$	Lead soldering temperature (10sec. max)	300	$^{\circ}\text{C}$

**NOTES:**

- Derate above  $25^{\circ}\text{C}$  at the following rates:  
F package at  $11.1\text{mW}/^{\circ}\text{C}$   
N package at  $13.7\text{mW}/^{\circ}\text{C}$   
D package at  $10.5\text{mW}/^{\circ}\text{C}$

**DC ELECTRICAL CHARACTERISTICS** $V_{CC} = 4.75\text{V}$  to  $5.25\text{V}$ ,  $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ , unless otherwise specified.<sup>1</sup>

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
$V_{IH}$ $V_{IL}$	Input voltage High Low		2.0		0.8	V
$V_{OL}$	Output voltage Low	$I_{OL}=150\text{mA}$ , $T_A=25^{\circ}\text{C}$ Over temperature		1.05	1.30 1.50	V
$I_{IH}$ $I_{IL}$	Input current High Low	$V_{IN}=V_{CC}$ $V_{IN}=0\text{V}$		<1.0 -3.0	10 -250	$\mu\text{A}$
$I_{OH}$	Leakage current	$V_{OUT}=28\text{V}$ ,		5	250	$\mu\text{A}$
$I_{CCL}$ $I_{CCH}$	Supply current All outputs low All outputs high	$V_{CC}=5.25\text{V}$		35 22	60 50	mA
$P_D$	Power dissipation	No output load			315	mW

**NOTES:**

- All typical values are at  $V_{CC}=5\text{V}$  and  $T_A=25^{\circ}\text{C}$

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## SWITCHING CHARACTERISTICS

 $V_{CC}=5V$ ,  $T_A=25^{\circ}C$ ,  $V_{OUT}=5V$ ,  $I_{OUT}=100mA$ ,  $V_{IL}=0.8V$ ,  $V_{IH}=2.0V$ .

SYMBOL	PARAMETER	TO	FROM	MIN	TYP	MAX	UNIT
$t_{PLH}$	Propagation delay time Low-to-high <sup>1</sup>	Output	$\overline{CE}$		900	1800	ns
$t_{PHL}$	High-to-low <sup>1</sup>				130	260	
$t_{PLH}$	Low-to-high <sup>2</sup>	Output	Data		920	1850	ns
$t_{PHL}$	High-to-low <sup>2</sup>				130	260	
$t_{PLH}$	Low-to-high <sup>3</sup>	Output	Address		900	1800	ns
$t_{PHL}$	High-to-low <sup>3</sup>				130	260	
$t_{PLH}$	Low-to-high <sup>4</sup>	Output	$\overline{CLR}$		920	1850	ns
$t_{PHL}$	High-to-low <sup>4</sup>						
<b>Switching setup requirements</b>							
$t_{S(H)}$	Setup time high Setup time low	Chip enable Chip enable	High data Low data	40 50			ns
$t_{S(A)}$	Address setup time	Chip enable	Address	40			ns
$t_{H(H)}$	Hold time high Hold time low	Chip enable Chip enable	High data Low data	10 10			ns
$t_{PW(E)}$	Chip enable pulse width <sup>1</sup>			40			ns

## NOTES:

1. See Turn-On and Turn-Off Delays, Enable-to-Output and Enable Pulse Width timing diagram.
2. See Turn-On and Turn-Off Delays, Data-to-Output timing diagram.
3. See Turn-On and Turn-Off Delays, Address-to-Output timing diagram.
4. See Turn-Off Delay, Clear-to-Output timing diagram.
5. See Setup and Hold Time, Data-to-Enable timing diagram.
6. See Setup Time, Address-to-Enable timing diagram.

## FUNCTIONAL DESCRIPTION

This peripheral driver has latched outputs which hold the input data until cleared. The NE5090 has active-Low, open-collector outputs, all of which are cleared when power is first applied. This device is identical to the NE590, except the outputs can withstand 28V.

## Addressable Latch Function

Any given output can be turned on or off by presenting the address of the output to be set or cleared to the three address pins, by holding the "D" input High to turn on the selected output, or by holding it Low to turn off, holding the  $\overline{CLR}$  input High, and bringing the  $\overline{CE}$  input Low. Once an output is turned on or off, it will remain so until addressed again, or until all outputs are cleared by bringing the  $\overline{CLR}$  input Low while holding the  $\overline{CE}$  input High.

## Demultiplexer Operation

By holding the  $\overline{CLR}$  and  $\overline{CE}$  inputs Low and the "D" input High, the addressed output will remain on and all other outputs will be off.

## High Current Outputs

The obvious advantage of this device over other drivers such as the 9334 and N74LS259 is the fact that the outputs of the NE5090 are each capable of 200mA and 28V. It must be noted, however, that the total power dissipation would be over 2.5W if all 8 outputs were on together and carrying 200mA each. Since the total power dissipation is limited by the package to 1W, and since power dissipation due to supply current is 0.25W, the total load power dissipation by the device is limited to 0.75W at room temperature, and decreases as ambient temperature rises.

The maximum die junction temperature must be limited to 165°C, and the temperature rise above ambient and the junction temperature are defined as:

$$T_R = \theta_{JA} \times P_D$$

$$T_J = T_A + T_R$$

where

For example, if we are using the NE5090 in a plastic package in an application where the ambient temperature is never expected to rise above 50°C, and the output current at the 8 outputs, when on, are 100, 40, 50, 200, 15, 30, 80, and 10mA, we find from the graph of output voltage vs load current that the output voltages are expected to be about 0.92, 0.75, 0.78, 1.04, 0.5, 0.7, 0.9, and 0.4V, respectively. Total device power due to these loads is found to be 473.5mW. Adding the 200mW due to the power supply brings total device power dissipation to 723.5mW. The thermal resistances are 83°C per W for plastic packages and 100°C per W for Cerdips. Using the equations above we find:

$$\text{Plastic } T_R = 83 \times 0.7235 = 60^{\circ}C$$

$$\text{Plastic } T_J = 50 + 60 = 110^{\circ}C$$

$$\text{Cerdip } T_R = 100 \times 0.7235 = 72.4^{\circ}C$$

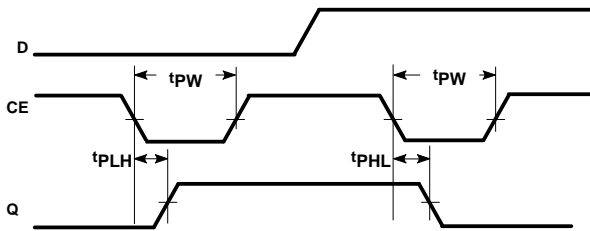
$$\text{Cerdip } T_J = 50 + 72.4 = 122.4^{\circ}C$$

Thus we find that  $T_J$  for either package is below the 165°C maximum and either package could be used in this application. The graphs of total load power vs ambient temperature would also give us this same information, although interpreting the graphs would not yield the same accuracy.

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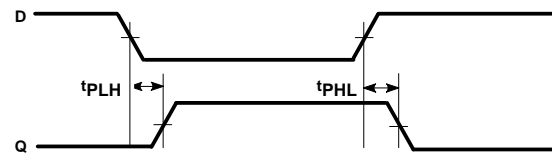
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## TIMING DIAGRAMS



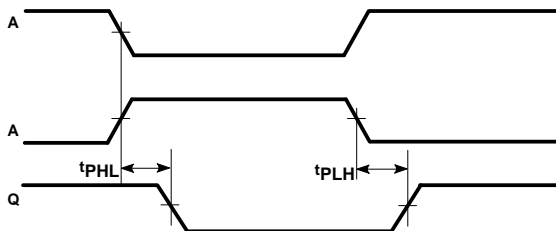
**NOTE:**  
Other Inputs:  $\overline{\text{CLR}} = \text{H}$ , A = Stable

**Turn-On and Turn-Off Delays, Enable-to-Output and Enable Pulse Width**



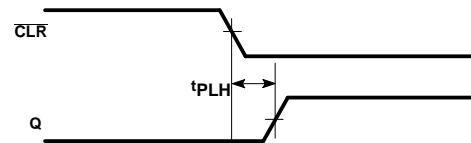
**NOTE:**  
Other Inputs:  $\overline{\text{CE}} = \text{L}$ ,  $\overline{\text{CLR}} = \text{H}$ , A = Stable

**Turn-On and Turn-Off Delays, Data-to-Output**

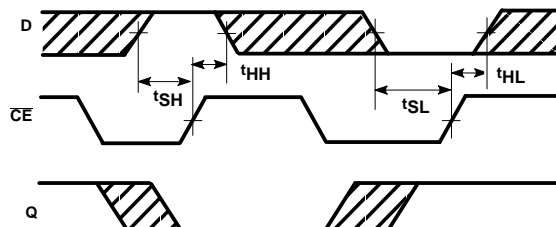


**NOTE:**  
Other Inputs:  $\overline{\text{CE}} = \text{L}$ ,  $\overline{\text{CLR}} = \text{L}$ , D = H

**Turn-On and Turn-Off Delays, Address-to-Output**

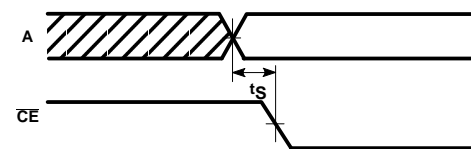


**Turn-Off Delays, Clear-to-Output**



**NOTE:**  
Other Inputs:  $\overline{\text{CLR}} = \text{H}$ , A = Stable

**Setup and Hold Time, Data-to-Enable**



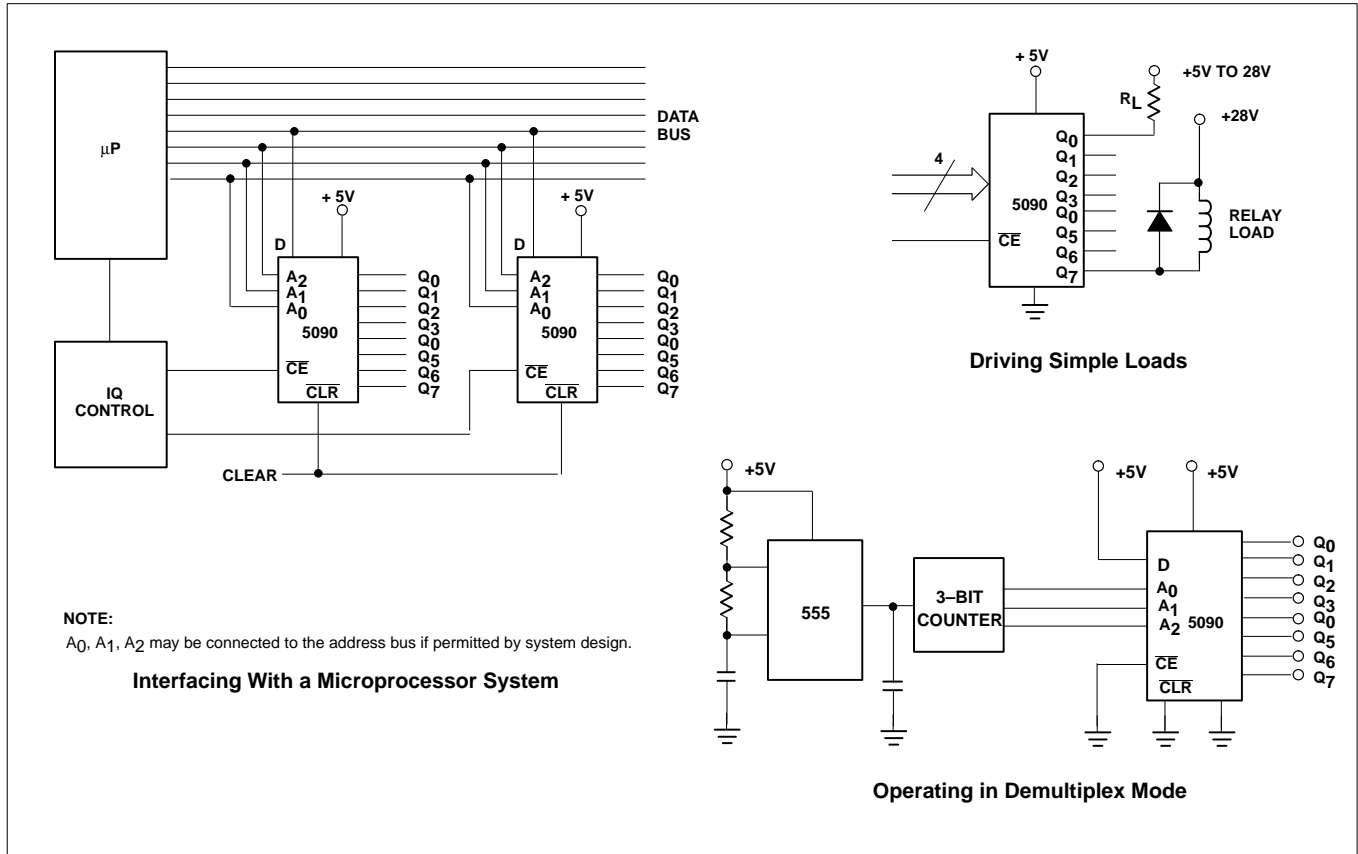
**NOTE:**  
Other Inputs:  $\overline{\text{CLR}} = \text{H}$

**Setup Time, Address-to-Enable**

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## TYPICAL APPLICATIONS



## TYPICAL PERFORMANCE CHARACTERISTICS

