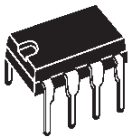
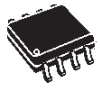
LF155-LF255-LF355
LF156-LF256-LF356
LF157-LF257-LF357

WIDE BANDWIDTH SINGLE J-FET OPERATIONAL AMPLIFIERS

- HIGH INPUT IMPEDANCE J-FET INPUT STAGE
- HIGH SPEED J-FET OP-AMPs : up to 20MHz, 50V/µs
- OFFSET VOLTAGE ADJUSTMENT DOES NOT DEGRADE DRIFT OR COMMON-MODE REJECTION AS IN MOST OF MONOLITHIC AMPLIFIERS
- INTERNAL COMPENSATION AND LARGE DIFFERENTIAL INPUT VOLTAGE CAPABILITY (UP TO V_{CC}^+)



N
DIP8
(Plastic Package)



D
SO8
(Plastic Micropackage)

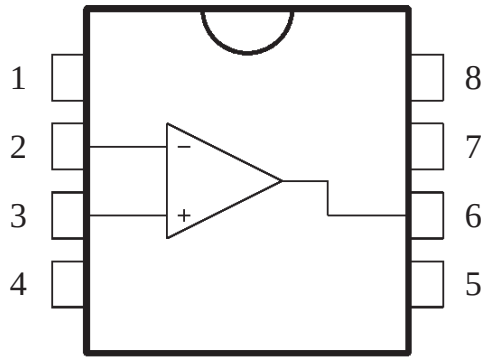
TYPICAL APPLICATIONS

- PRECISION HIGH SPEED INTEGRATORS
- FAST D/A AND CONVERTERS
- HIGH IMPEDANCE BUFFERS
- WIDEBAND, LOW NOISE, LOW DRIFT AMPLIFIERS
- LOGARITHIMIC AMPLIFIERS
- PHOTOCELL AMPLIFIERS
- SAMPLE AND HOLD CIRCUITS

ORDER CODES

Part Number	Temperature Range	Package	
		N	D
LF355, LF356, LF357	0°C, +70°C	•	•
LF255, LF256, LF257	–40°C, +105°C	•	•
LF155, LF156, LF157	–55°C, +125°C	•	•
Example : LF355N			

PIN CONNECTIONS (top view)



1 - Offset Null 1
2 - Inverting input
3 - Non-inverting input
4 - V_{CC}^-
5 - Offset Null 2
6 - Output
7 - V_{CC}^+
8 - N.C.

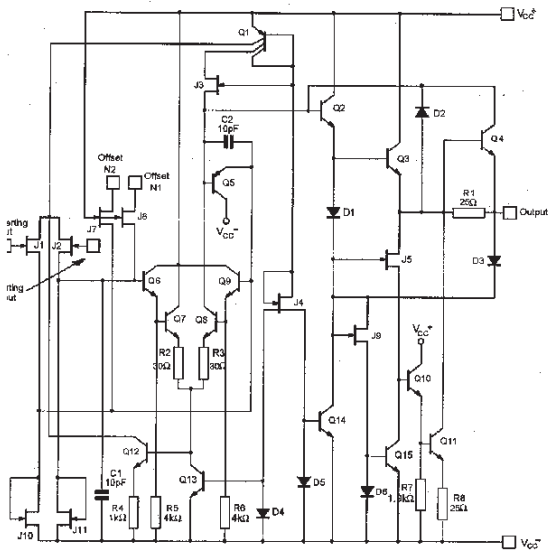
DESCRIPTION

These circuits are monolithic J-FET input operational amplifiers incorporating well matched, high voltage J-FET on the same chip with standard bipolar transistors.

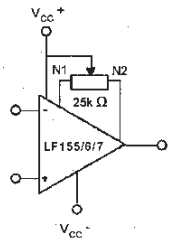
This amplifiers feature low input bias and offset currents, low input offset voltage and input offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection.

The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise level.

SCHEMATIC DIAGRAM



V_{io} ADJUSTMENT



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		±22	V
V_i	Input Voltage - (note 1)		±20	V
V_{id}	Differential Input Voltage		±40	V
P_{tot}	Power Dissipation		570	mW
	Output Short-circuit Duration		Infinite	
T_{oper}	Operating Free Air Temperature Range	LF155-LF156-LF157 LF255-LF256-LF257 LF355-LF356-LF357	-55 to +125 –40 to +105 0 to 70	^{o}C
T_{stg}	Storage Temperature Range		–65 to 150	^{o}C

ELECTRICAL CHARACTERISTICS

LF155, LF156, LF157 $-55^oC \le T_{amb} \le +125^oC$ $\pm5V \le V_{CC} \le \pm20V$
LF255, LF256, LF257 $-40^oC \le T_{amb} \le +105^oC$ $\pm5V \le V_{CC} \le \pm20V$
(unless otherwise specified)

Symbol	Parameter		LF155 - LF156 - LF157 LF255 - LF256 - LF257 Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage (R_S = 50Ω) T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$	 LF155, LF156, LF157 LF255, LF256, LF257		3	 5 7 6.2	mV
I_{io}	Input Offset Current - (note 3) T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$	 LF155, LF156, LF157 LF255, LF256, LF257		3	20 20 1	pA nA nA
I_{ib}	Input Bias Current - (note 3) T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$	 LF155, LF156, LF157 LF255, LF256, LF257		20	100 50 5	pA nA nA
A_{vd}	Large Signal Voltage Gain (R_L = 2kΩ, V_O = ±10V, V_{CC} = ±15V) T_{amb} = 25°C $T_{min.} \le T_{amb} \le T_{max.}$		50 25	200		V/mV
SVR	Supply Voltage Rejection Ratio - (note 4)		85	100		dB
I_{CC}	Supply Current (V_{CC} = ±15V, no load) T_{amb} = 25°C	 LF155, LF255 LF156, LF256 LF157, LF257		 2 5 5	 4 7 7	mA
DV_{io}	Input Offset Voltage Drift (R_S = 50Ω)			5		µV/°C
DV_{io}/V_{io}	Change in Average Temperature Coefficient with V_{io} adjust (R_S = 50Ω) - (note 2)			0.5		µV/°C
V_{icm}	Input Common Mode Voltage Range (V_{CC} = ±15V, T_{amb} = 25°C)		±11	+15.1 -12		V
CMR	Common Mode Rejection Ratio		85	100		dB
$\pm V_{OPP}$	Output Voltage Swing (V_{CC} = ±15V) R_L = 10kΩ R_L = 2kΩ		 ±12 ±10	 ±13 ±12		V
GBP	Gain Bandwidth Product (V_{CC} = ±15V, T_{amb} = 25°C)	 LF155, LF255 LF156, LF256 LF157, LF257		 2.5 5 20		MHz
SR	Slew Rate (V_{CC} = ±15V, T_{amb} = 25°C) A_V = 1 A_V = 5	 LF155, LF255 LF156, LF256 LF157, LF257	 7.5 30	 5 12 50		V/µs
R_i	Input Resistance (T_{amb} = 25°C)			10^{12}		Ω
C_i	Input Capacitance (V_{CC} = ±15V, T_{amb} = 25°C)			3		pF
e_n	Equivalent Input Noise Voltage (V_{CC} = ±15V, T_{amb} = 25°C, R_S = 100Ω) f = 1000Hz f = 100Hz	 LF155, LF255 LF156, LF256 LF157, LF257 LF155, LF255 LF156, LF256 LF157, LF257		 20 12 12 25 15 15		$\frac{nV}{\sqrt{Hz}}$
i_n	Equivalent Input Noise Current (V_{CC} = ±15V, T_{amb} = 25°C, f = 100Hz or f = 1000Hz)			0.01		$\frac{pA}{\sqrt{Hz}}$
t_s	Settling Time (V_{CC} = ±15V, T_{amb} = 25°C) - (note 5)	 LF155, LF255 LF156, LF256 LF157, LF257		 4 1.5 1.5		µs

ELECTRICAL CHARACTERISTICS

LF355, LF356, LF357 $0^oC \leq T_{amb} \leq +70^oC$ $V_{CC} = \pm 15V$, (unless otherwise specified)

Symbol	Parameter		LF355 - LF356 - LF357			Unit
			Min.	Typ.	Max.	
V_{io}	Input Offset Voltage ($R_S = 50\Omega$) $T_{amb} = 25^oC$ $T_{min.} \leq T_{amb} \leq T_{max.}$			3	10 13	mV
I_{io}	Input Offset Current - (note 3) $T_{amb} = 25^oC$ $T_{min.} \leq T_{amb} \leq T_{max.}$			3	50 2	pA nA
I_{ib}	Input Bias Current - (note 3) $T_{amb} = 25^oC$ $T_{min.} \leq T_{amb} \leq T_{max.}$			20	200 8	pA nA
A_{vd}	Large Signal Voltage Gain ($R_L = 2k\Omega$, $V_O = \pm 10V$) $T_{amb} = 25^oC$ $T_{min.} \leq T_{amb} \leq T_{max.}$		25 15	200		V/mV
SVR	Supply Voltage Rejection Ratio - (note 4)		80	100		dB
I_{CC}	Supply Current (no load) $T_{amb} = 25^oC$	LF355 LF356, LF357		2 5	4 10	mA
DV_{io}	Input Offset Voltage Drift ($R_S = 50\Omega$) - (note 2)			5		$\mu V/^oC$
DV_{io}/V_{io}	Change in Average Temperature Coefficient with V_{io} adjust ($R_S = 50\Omega$)			0.5		$\mu V/^oC$ per mV
V_{icm}	Input Common Mode Voltage Range ($T_{amb} = 25^oC$)		±10	+15.1 -12		V
CMR	Common Mode Rejection Ratio		80	100		dB
$\pm V_{OPP}$	Output Voltage Swing	$R_L = 10k\Omega$ $R_L = 2k\Omega$	±12 ±10	±13 ±12		V
GBP	Gain Bandwidth Product $T_{amb} = 25^oC$)	LF355 LF356 LF357		2.5 5 20		MHz
SR	Slew Rate ($T_{amb} = 25^oC$) $A_V = 1$ $A_V = 5$	LF355 LF356 LF357		5 12 50		V/µs
R_i	Input Resistance ($T_{amb} = 25^oC$)			10^{12}		Ω
C_i	Input Capacitance (Tamb = 25^oC)			3		pF
e_n	Equivalent Input Noise Voltage ($T_{amb} = 25^oC$, $R_S = 100\Omega$) f = 1000Hz f = 100Hz	LF355 LF356, LF357 LF355 LF356, LF357		20 12 25 15		$\frac{nV}{\sqrt{Hz}}$
i_n	Equivalent Input Noise Current ($T_{amb} = 25^oC$, f = 100Hz or f = 1000Hz)			0.01		$\frac{pA}{\sqrt{Hz}}$
t_s	Settling Time ($T_{amb} = 25^oC$) - (note 5)	LF355 LF356, LF357		4 1.5		µs

Notes :
1. Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
2. The temperature coefficient of the adjusted input offset voltage changes only a small amount ($0.5\mu V/^oC$ typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are alsounaffected by offset adjustment.
3. The input bias currents are junction leakage currents which approximately double for every 10^oC increase in the junction temperature T_{amb}. Due to limited production test time, the input bias current measured is correlated to junction temperature. In a normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_{tot}-T_{amb} =T_{amb} +$R_{th(j-a)}$xP_{tot} where $Rt_{h(j-a)}$ is the thermal resistance from junction to ambient. Use of a heatsink is recommended f input currents are to be kept to a minimum.
4. Supply voltage rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practise.
5. Settling time is defined here, for a unity gain inverter connection using 2kΩ resistors for the LF155, LF156 series. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF157 series A_V = -5, the feedback resistor from output to input is 2kΩ and the output step is 10V.

APPLICATION HINTS

The LF155, LF156, LF157 series are op amps with JFET input transistors. These JFETs have large reverse breakdown voltages from gate to source or drain eliminating the need of clamps across the inputs. Therefore large differential input voltages can easily be accommodated without a large increase of input currents. The maximum differential input voltage is independent of the supply voltage. However, neither of the negative input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit. Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode. Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state. These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply volt-age and over the full operating temperature range. The positive suplly can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter. Precautions should be taken to ensure that the power supply for the integrated circuit never becomes re-versed in polarity or that the unit is not inadvertently in-stalled backwards in a socket as an unilimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

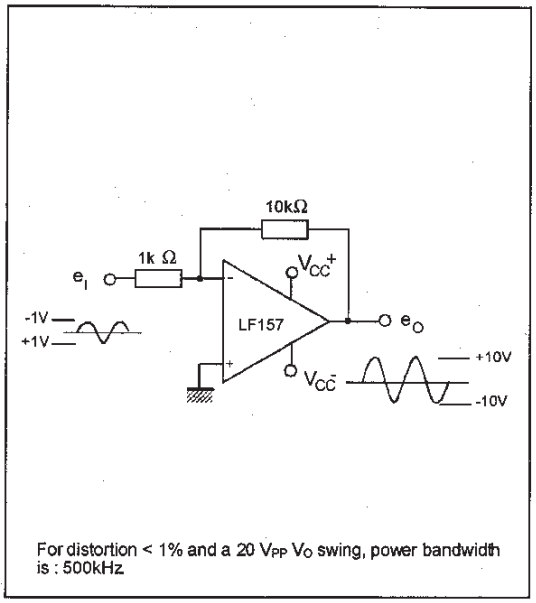
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltages.

As with most amplifiers, care should be taken with lead dress, components placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimiz "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six time the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of that added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

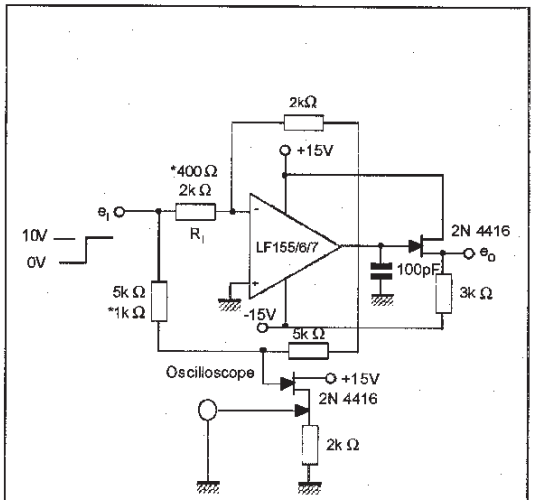
TYPICAL CIRCUITS

LARGE POWER BW AMPLIFIER

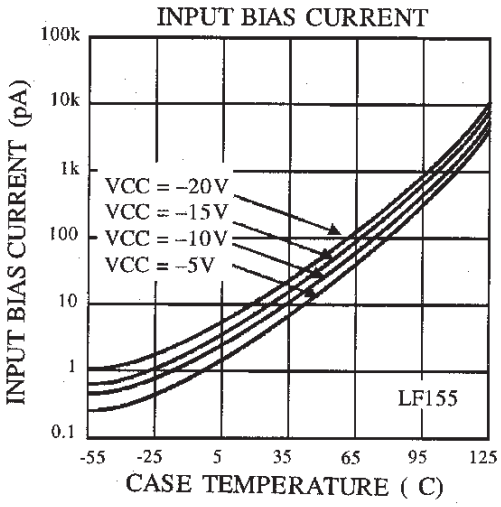


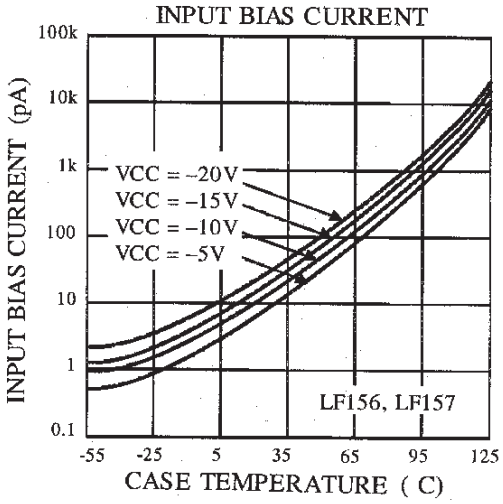
For distortion < 1% and a 20 V_{PP} V_O swing, power bandwidth is : 500kHz.

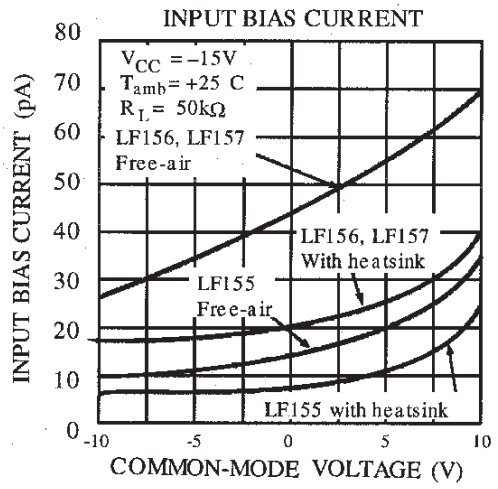
SETTLING TIME TEST CIRCUIT

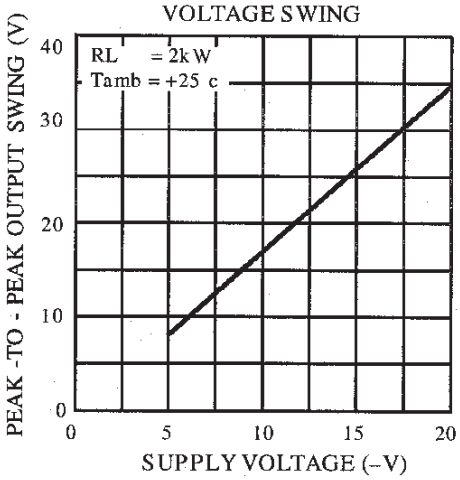


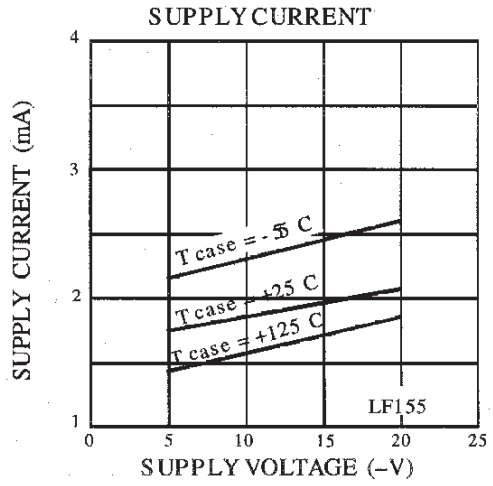
Settling time is tested with the LF155, LF156 connected as unity gain converter R_I = 2kΩ and LF157 connected for A_V = -5, R_I = 0.4kΩ

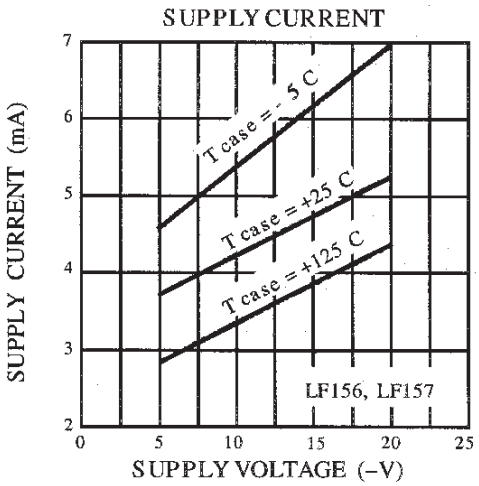




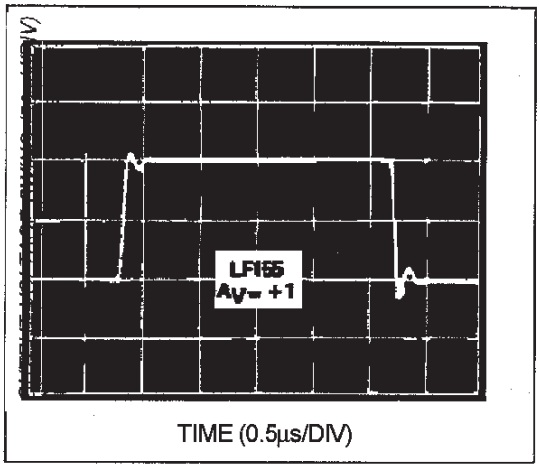




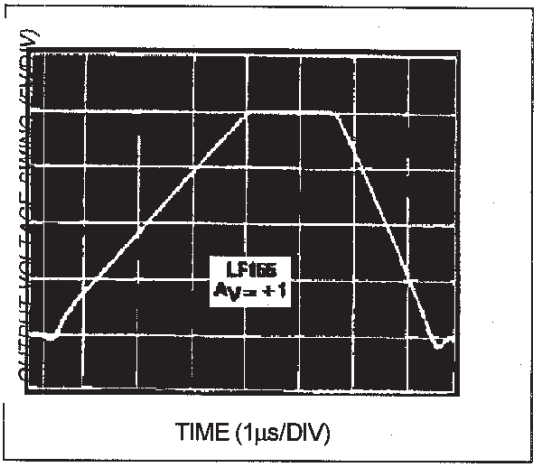




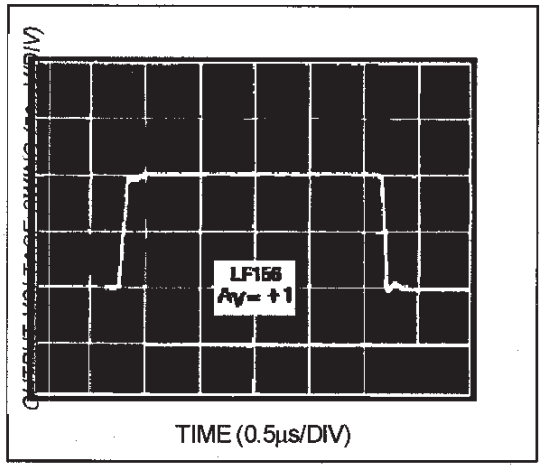
SMALL SIGNAL PULSE RESPONSE



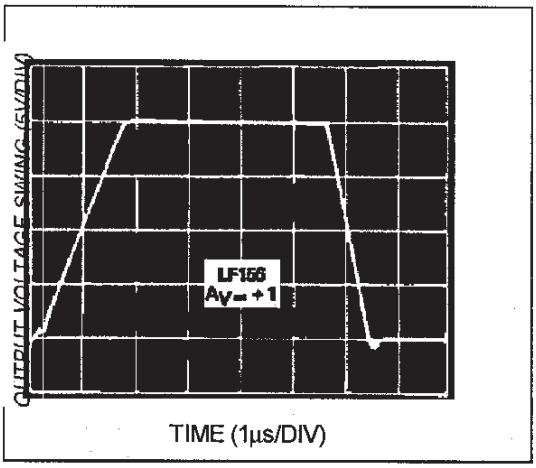
SMALL SIGNAL PULSE RESPONSE



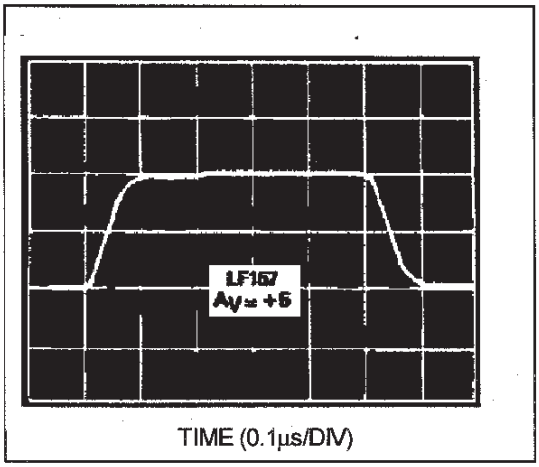
SMALL SIGNAL PULSE RESPONSE



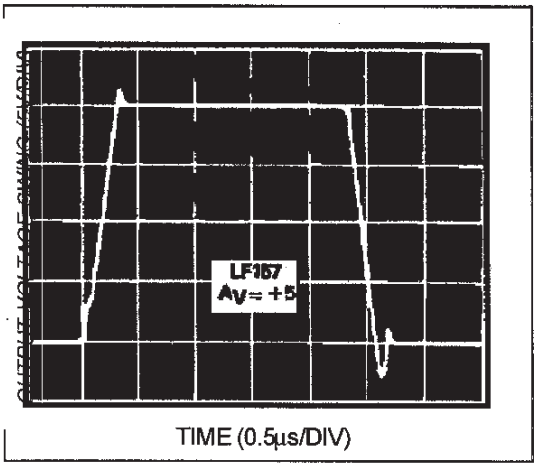
SMALL SIGNAL PULSE RESPONSE



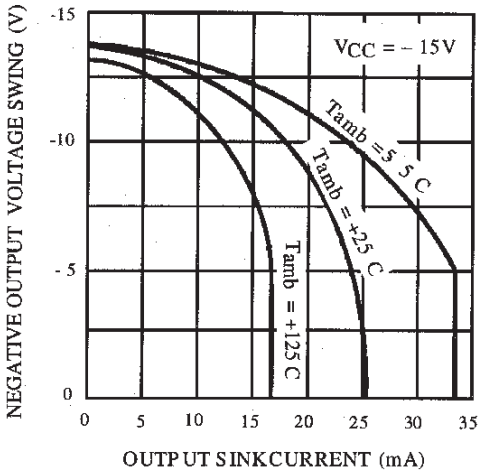
SMALL SIGNAL PULSE RESPONSE



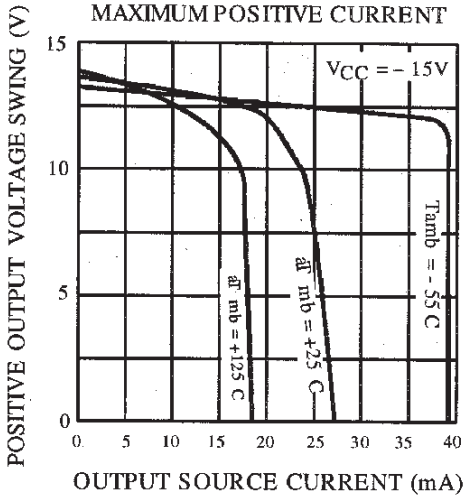
SMALL SIGNAL PULSE RESPONSE



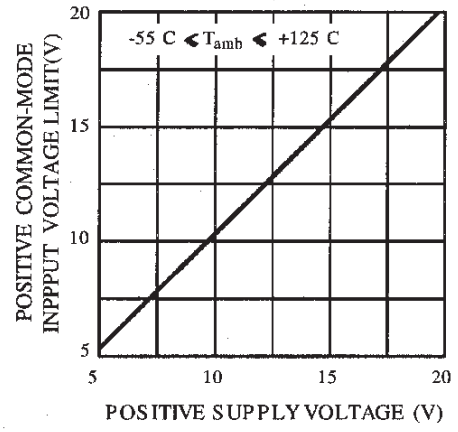
MAXIMUM NEGATIVE CURRENT



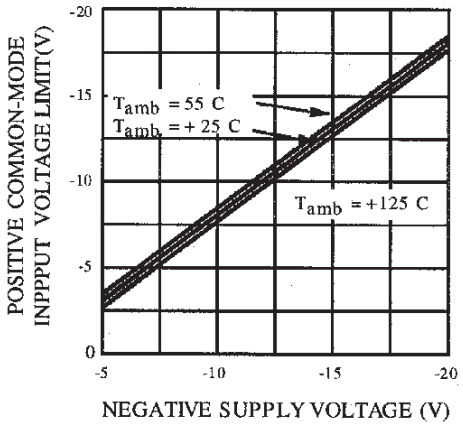
MAXIMUM POSITIVE CURRENT



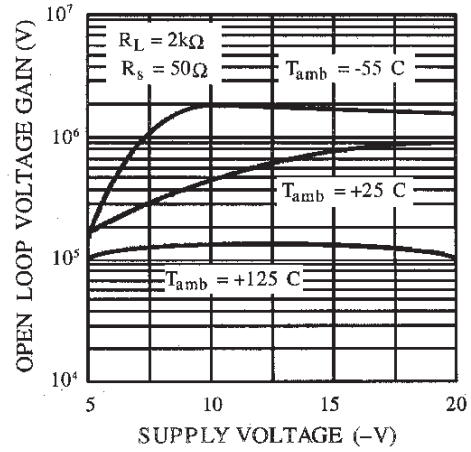
MAXIMUM POSITIVE COMMON-MODE INPUT VOLTAGE



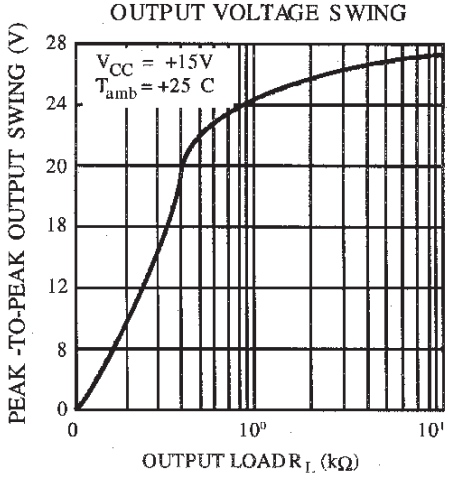
MAXIMUM NEGATIVE COMMON-MODE INPUT VOLTAGE



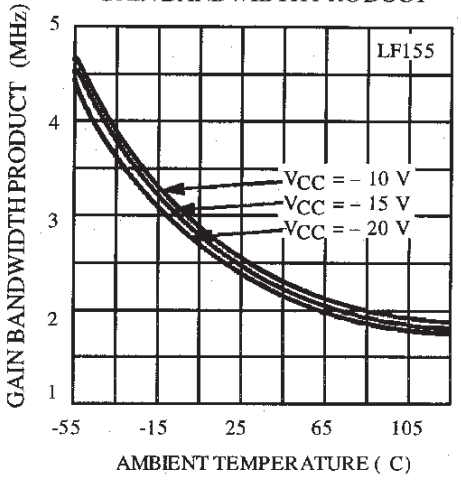
OPEN LOOP VOLTAGE GAIN



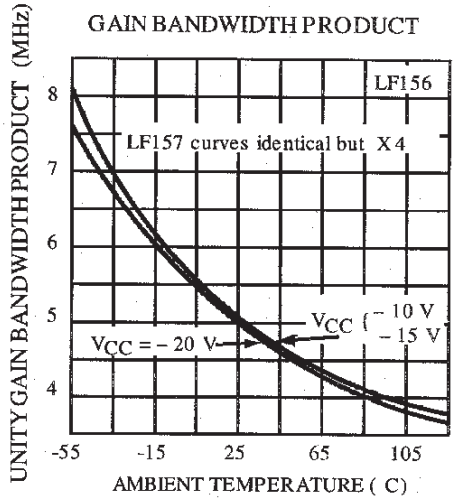
OUTPUT VOLTAGE SWING



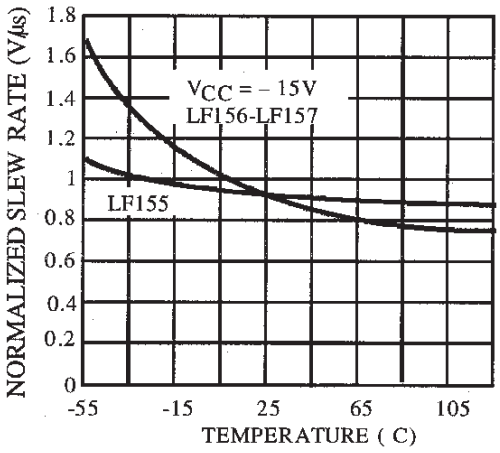
GAIN BANDWIDTH PRODUCT



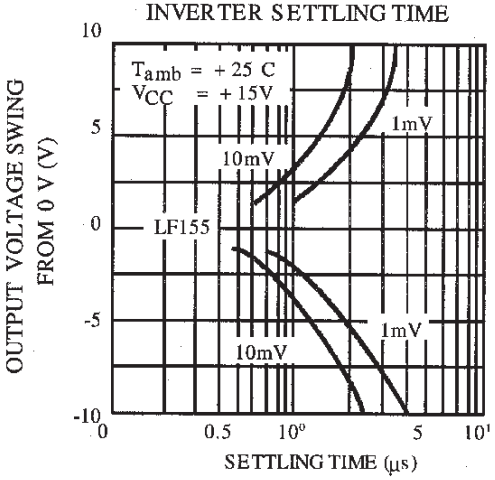
GAIN BANDWIDTH PRODUCT



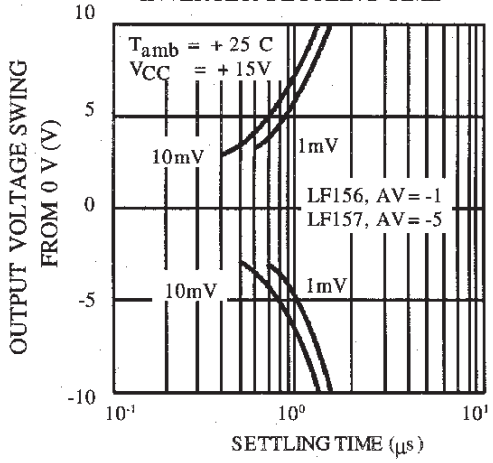
NORMALIZED SLEW RATE



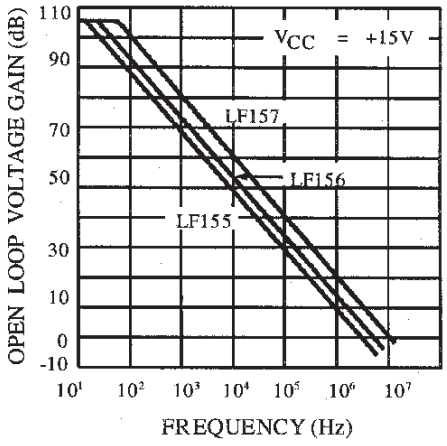
INVERTER SETTLING TIME



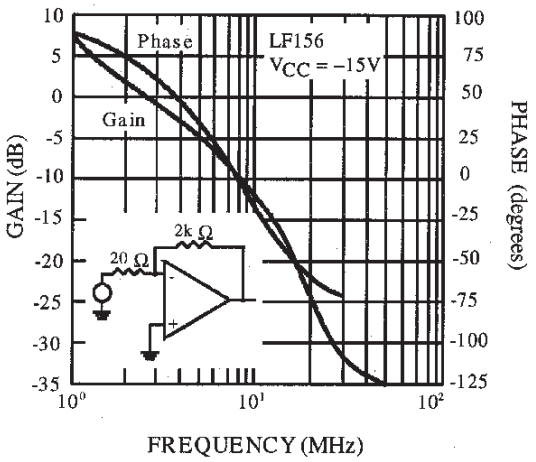
INVERTER SETTLING TIME



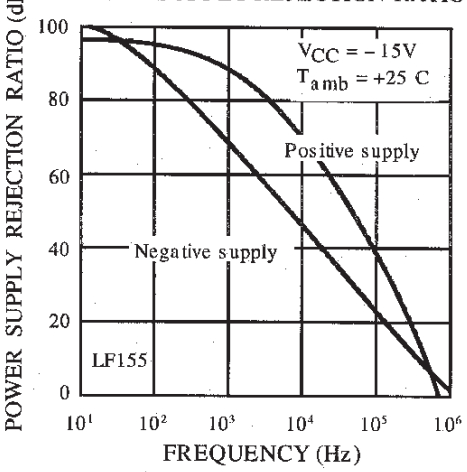
OPEN LOOP FREQUENCY RESPONSE



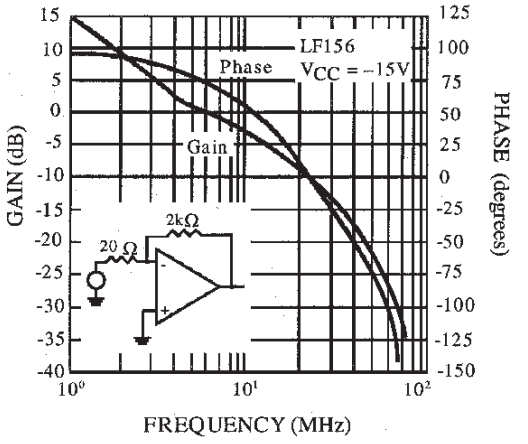
BODE PLOT



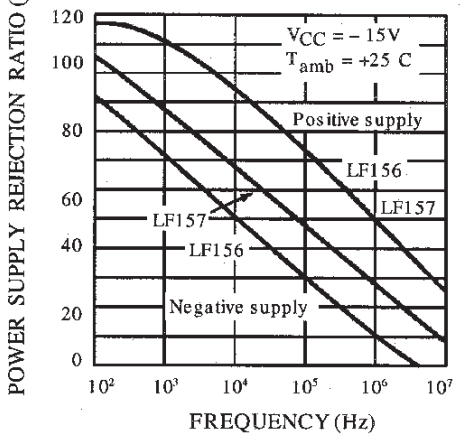
POWER SUPPLY REJECTION RATIO



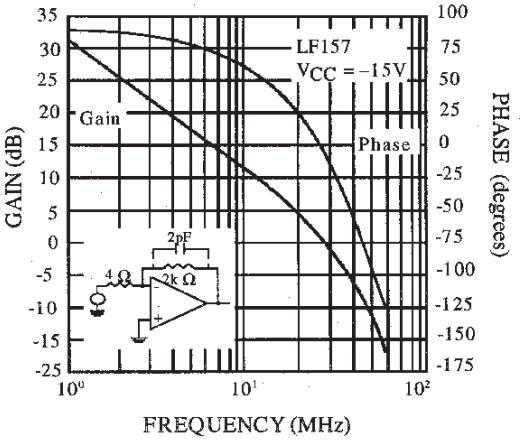
BODE PLOT



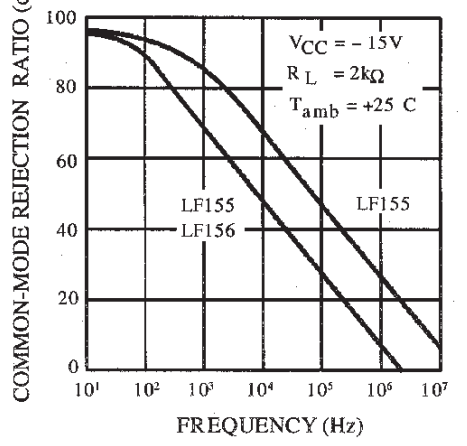
POWER SUPPLY REJECTION RATIO



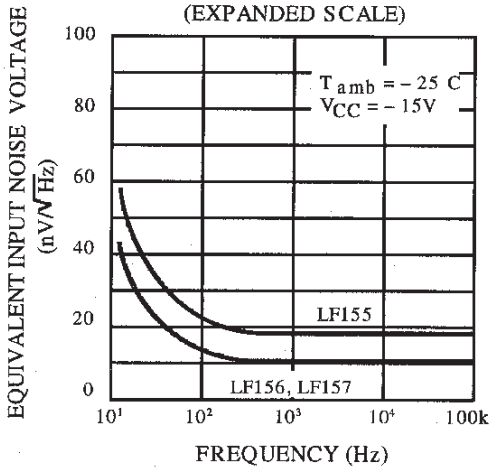
BODE PLOT



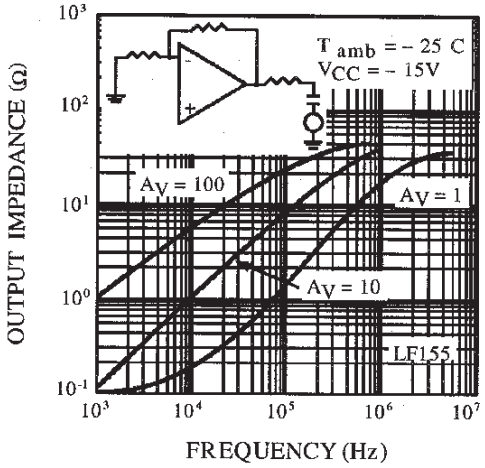
COMMON-MODE REJECTION RATIO



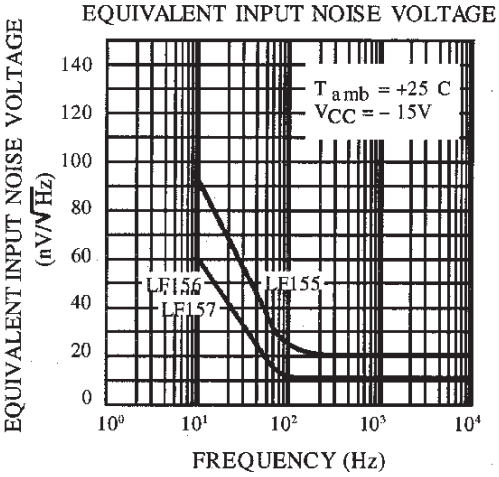
EQUIVALENT INPUT NOISE VOLTAGE
(EXPANDED SCALE)



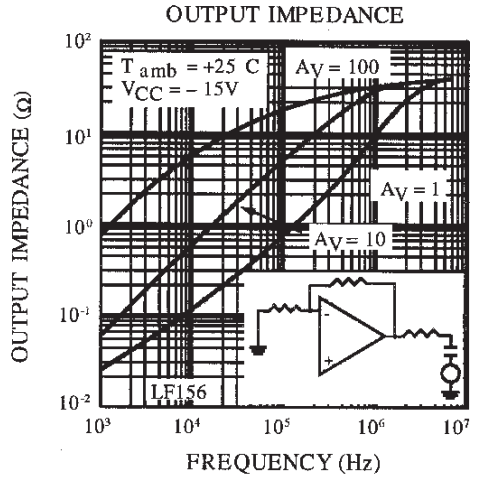
OUTPUT IMPEDANCE



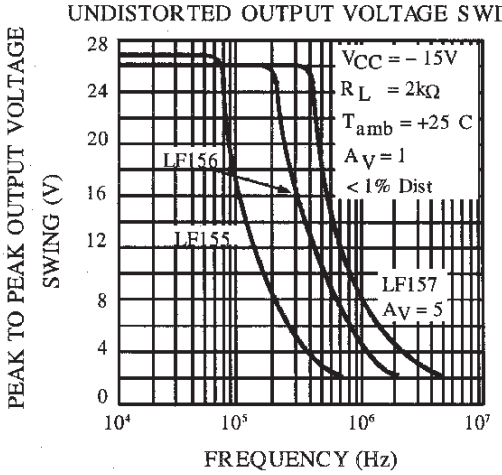
EQUIVALENT INPUT NOISE VOLTAGE



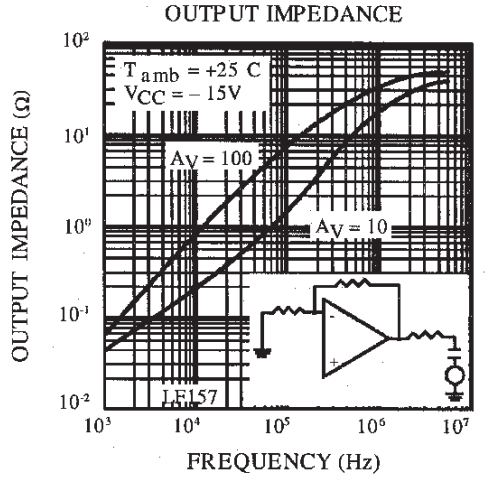
OUTPUT IMPEDANCE



UNDISTORTED OUTPUT VOLTAGE SWING

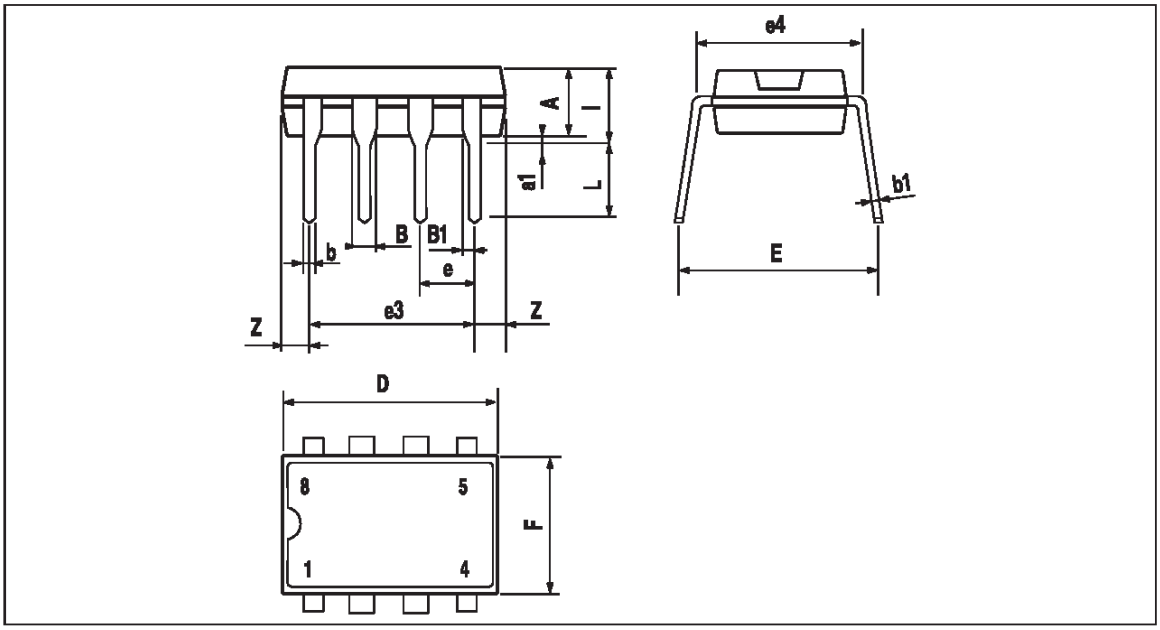


OUTPUT IMPEDANCE



PACKAGE MECHANICAL DATA

8 PINS - PLASTIC DIP



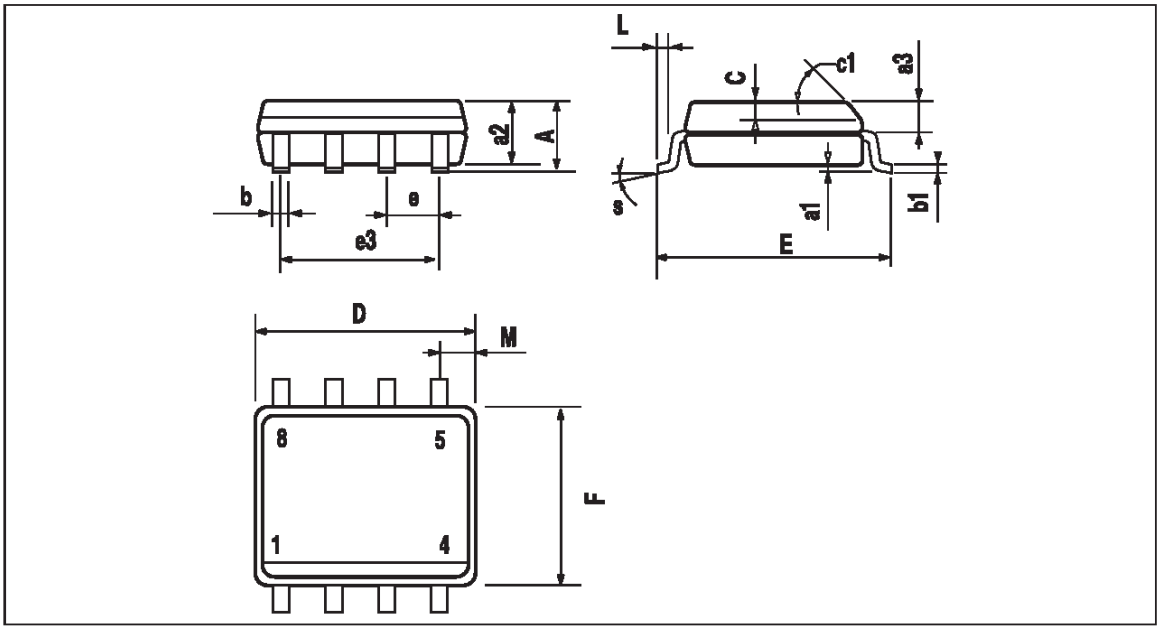
PM-DIP8.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0260
i			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

DIP8.TBL

PACKAGE MECHANICAL DATA

8 PINS - PLASTIC MICROPACKAGE (SO)



PM-SO8.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.25	0.004		0.010
a2			1.65			0.065
a3	0.65		0.85	0.026		0.033
b	0.35		0.48	0.014		0.019
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.020
c1	45° (typ.)					
D	4.8		5.0	0.189		0.197
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.150		0.157
L	0.4		1.27	0.016		0.050
M			0.6			0.024
S	8° (max.)					

SO8.TBL

ORDER CODE :