SONY

CXL5504M/P

CMOS-CCD 1H Delay Line for NTSC

Description

The CXL5504M/P are CMOS-CCD delay line ICs that provide 1H delay time for NTSC signals including the external low-pass filter.

Features

- Single power supply (5V)
- Low power consumption 90mW (Typ.)
- Built-in peripheral circuits
- Clamp level of I/O signal can be selected

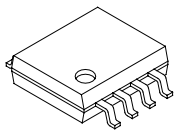
Functions

- 905-bit CCD register
- Clock driver
- Autobias circuit
- Input clamp circuit
- Sample and hold circuit

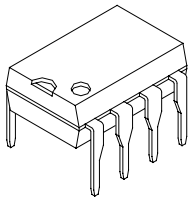
Structure

CMOS-CCD

CXL5504M
8 pin SOP (Plastic)



CXL5504P
8 pin DIP (Plastic)



Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	6	V
• Operating temperature	Topr	–10 to +60	°C
• Storage temperature	Tstg	–55 to +150	°C
• Allowable power dissipation	P_D		
	CXL5504M	350	mW
	CXL5504P	480	mW

Recommended Operating Condition (Ta = 25°C)

Supply voltage	V_{DD}	5 ± 5%	V

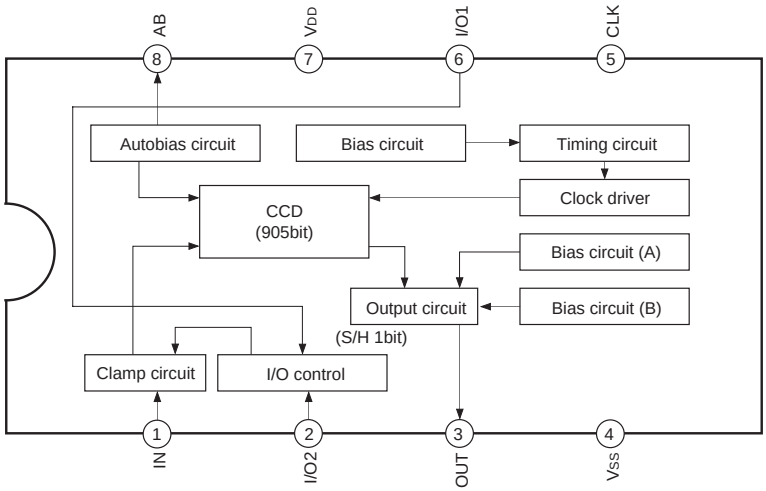
Recommended Clock Conditions (Ta = 25°C)

• Input clock amplitude	V_{CLK}	0.4 to 1.0 (0.5Vp-p typ.)	Vp-p
• Clock frequency	f_{CLK}	14.318182	MHz
• Input clock waveform	Sine wave		

Input Signal Amplitude

V_{SIG} 500mVp-p (Typ.), 572mVp-p (Max.)
(at internal clamp condition)

Blook Diagram and Pin Configration (Top View)



E89931C79-PS

Pin Description

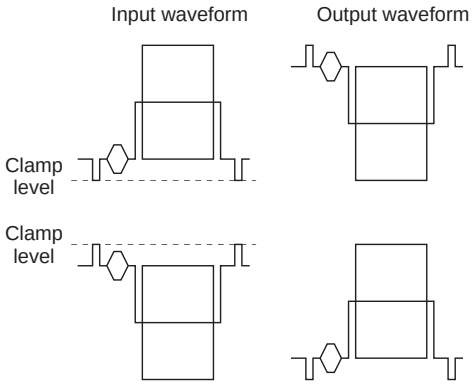
Pin No.	Symbol	I/O	Description	Impedance
1	IN	I	Signal input	> 10kΩ at no clamp
2	I/O2	I	I/O control 2	
3	OUT	O	Signal output	40 to 500Ω
4	V_{SS}	—	GND	
5	CLK	I	Clock input	> 100kΩ
6	I/O1	I	I/O control 1	
7	V_{DD}	—	Power supply (5V)	
8	AB	O	Autobias DC output	600 to 200kΩ

Description of Function

In the CXL5504M/P, the condition of I/O control pins (Pins 2 and 6) control the input signal clamp condition and the mode of the output signal with relation to its input signal.
There are 2 modes for the I/O signal.

(1) PN mode
(Low level clamp/reverse phase output mode)

(2) NP mode
(High level clamp/positive phase output mode)



I/O Control Pin

(1) I/O1 (Pin 6)
Control of the I/O signal condition
DC open ..... Input signal is low level clamped and the output signal is inverted in relation to the input signal. As the pin is biased to 2.5V by means of the resistance inside the IC, a decoupling capacitor of around 1000pF is necessary.
GND ..... Input signal is high level clamped and the output signal turns into an inverted signal.

(2) I/O2 (Pin 2)
Control of the input signal clamp condition
0V ..... Internal clamp condition
5V ..... Non internal clamp condition
Center biased to approx. 2.1V by means of the IC internal resistance (several 10kΩ).
Usage in this mode is limited to APL 50% signals and in this mode, the maximum input signal amplitude is 200mVp-p.

Electrical Characteristics (Ta = 25°C, V_{DD} = 5V, f_{CLK} = 14.318182MHz, V_{CLK} = 500mVp-p, Sine wave)

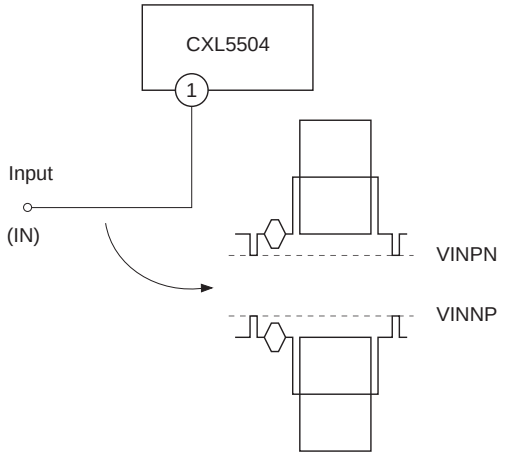
See "Electrical Characteristics Test Circuit"

Item	Symbol	Test condition	SW condition 1	2	3	4	5	6	7	Bias condition Vbias1 (V) (Note 1)	Min.	Typ.	Max.	Unit	Note
Supply current	IDDPN	—	—	c	b	b	b	a	—	—	10	18	28	mA	2
	IDDNP					a	a								
Low frequency gain	GLPN	200kHz, 500mVp-p, sine wave	a	a	b	b	b	a	b	—	–2	0	2	dB	3
	GLNP					a	a								
Frequency response	fPN	200kHz ⟷ 3.57MHz, 150mVp-p, sine wave	b ↕ c	a	a	b	b	b	b	2.1	–2	–1	0	dB	4
	fNP					a	a								
Differential gain	DGPN	5-staircase wave (See Note 5)	d	a	b	b	b	a	c	—	0	5	7	%	5
	DGNP			b		a	a								
Differential phase	DPPN	5-staircase wave (See Note 5)	d	a	b	b	b	a	c	—	0	5	7	degree	5
	DPNP			b		a	a								
S/H pulse coupling	CPPN	No signal input	—	c	a	b	b	b	a	VINPN + 0.5	—	—	350	mVp-p	6
	CPNP					a	a			VINNP					
S/N ratio	SNPN	50% white video signal (See Note 7)	e	a	b	b	b	a	d	—	52	56	—	dB	7
	SNNP			b		a	a								

Notes

(1) VINPN and VINNP are defined as follows.

VINPN and VINNP are the input signal clamp levels of PN and NP modes clamping the video signal sync tip level.



Testing of VINPN and VINNP is executed with a voltmeter under the following SW conditions.

Item	SW condition 1	2	3	4	5	6	7	Test point
VINPN	—	c	b	b	b	a	—	V1
VINNP	—	c	b	a	a	a	—	

(2) This is the IC supply current value during clock and signal input.

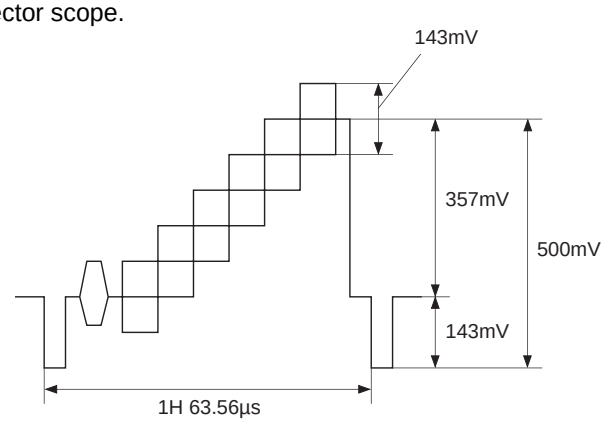
(3) GLPN, GLNP are output gain of OUT pin when a 500mVp-p, 200kHz sine wave is fed to IN pin.
(Example of calculation)

$$GLPN = 20 \log \frac{\text{OUT pin output voltage (PN mode) [mVp-p]}}{\text{500 [mVp-p]}} \text{ [dB]}$$

(4) Indicates the dissipation at 3.57MHz in relation to 200kHz.
From the output voltage at OUT pin when a 150mVp-p, 200kHz sine wave is fed to IN pin, and from the output voltage at OUT pin when a 150mVp-p, 3.57MHz sine wave is fed to same, calculation is made according to the following formula. The input part bias is tested at 2.1V.
(Example of calculation)

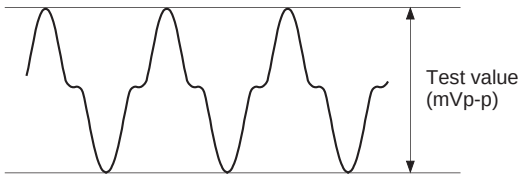
$$fPN = 20 \log \frac{\text{OUT pin otuput voltage (PN mode, 3.57MHz) [mVp-p]}}{\text{OUT pin output voltage (PN mode, 200kHz) [mVp-p]}} \text{ [dB]}$$

(5) The differential gain (DG) and the differential phase (DP), when the 5-staircase wave in the figure below is input are tested at the vector scope.

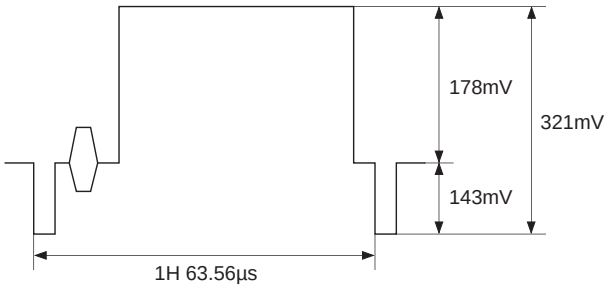


Input waveform (Input waveform of NP mode is the inverted waveform in the figure above)

(6) The internal clock component to the output signal during no-signal input and the leakage of that high harmonic component are tested. The input part bias is tested at VINPN + 0.5V and VINNP for PN and NP modes respectively.



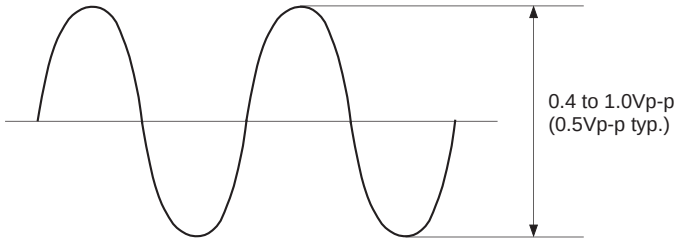
(7) S/N ratio during a 50% white video signal input shown in figure below is tested at a video noise meter, in BPF 100kHz to 4MHz, Sub Carrier Trap mode.



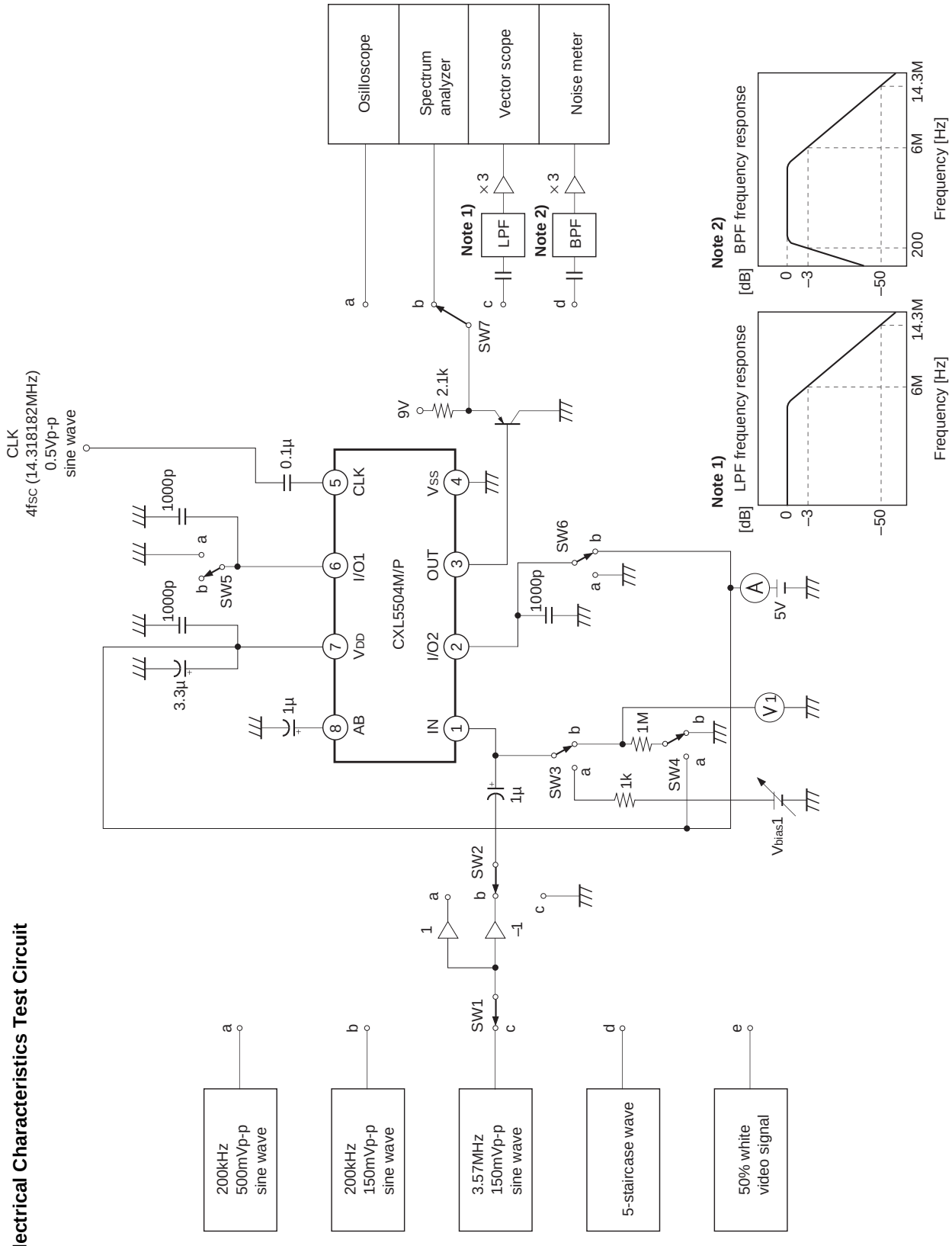
Input waveform (Input waveform of NP mode is the inverted waveform in the figure above)

Clock

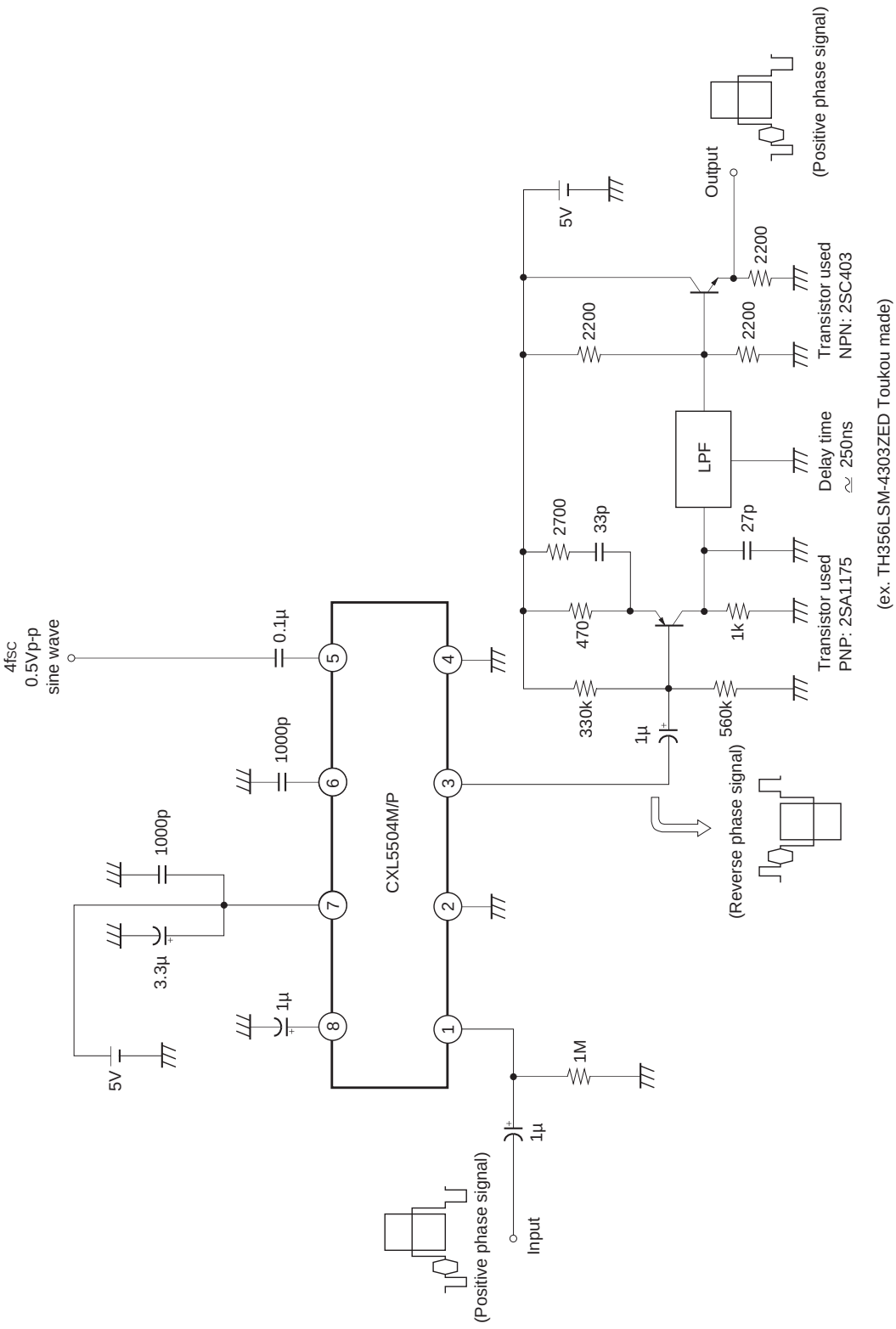
fsc (14.318182MHz) sine wave



Electrical Characteristics Test Circuit



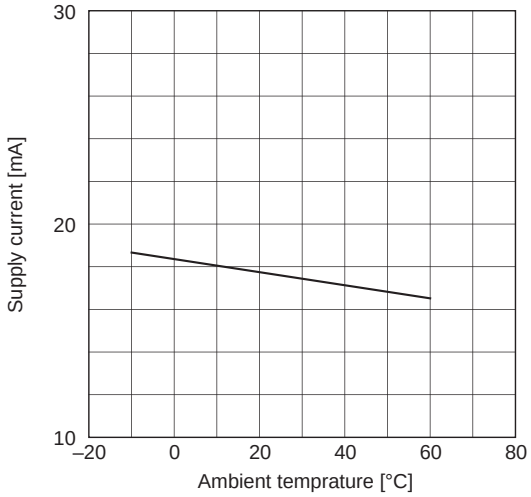
Application Circuit (Using PN mode)



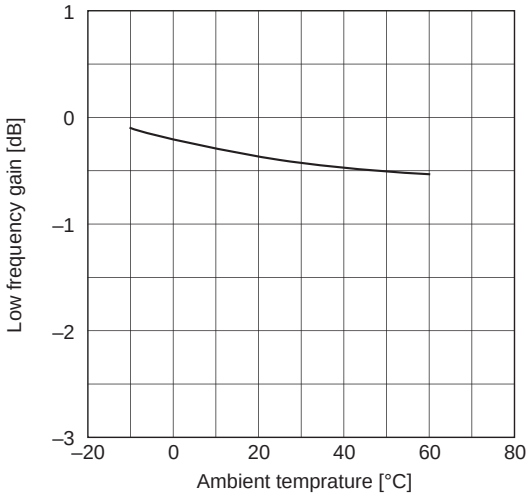
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics

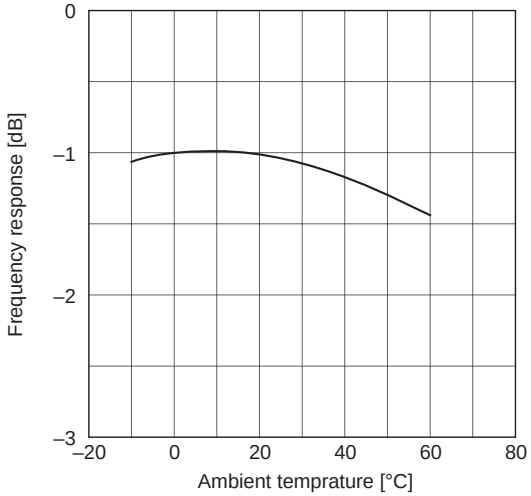
Supply current vs. Ambient temprature



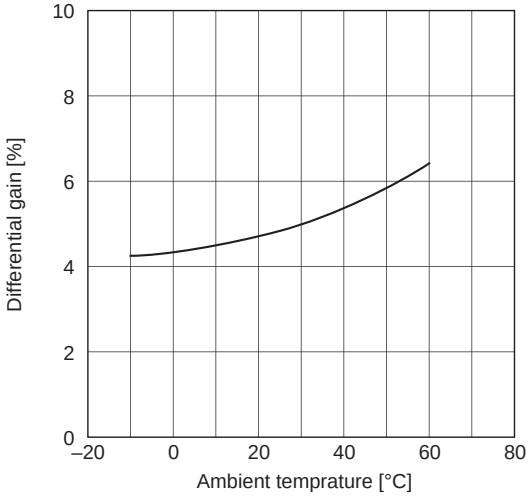
Low frequency gain vs. Ambient temprature



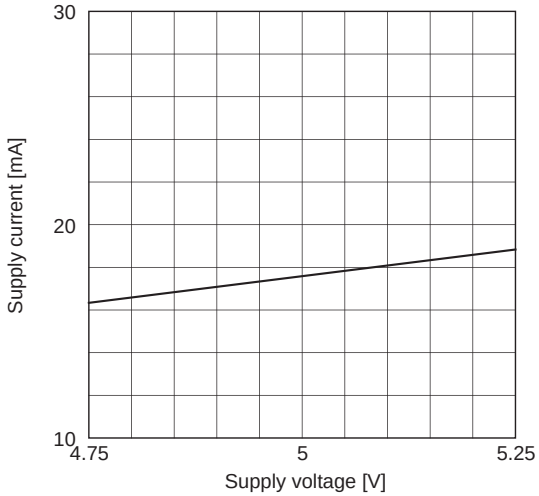
Frequency response vs. Ambient temprature



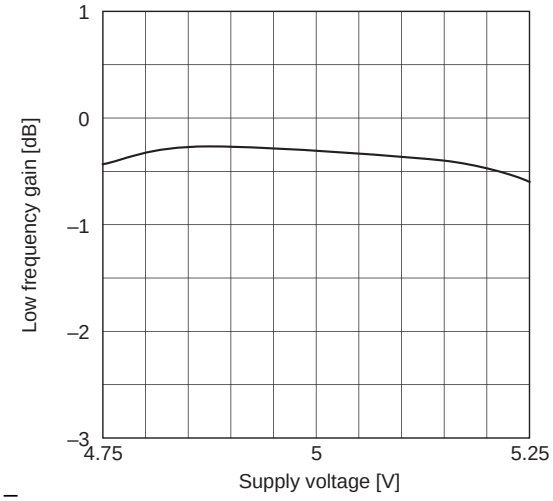
Differential gain vs. Ambient temprature



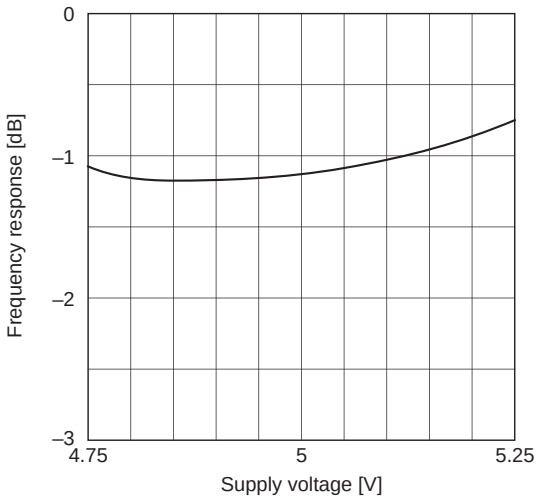
Supply current vs. Supply voltage



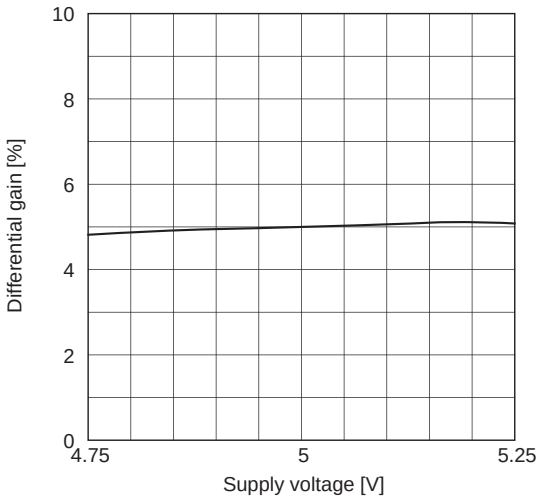
Low frequency gain vs. Supply voltage



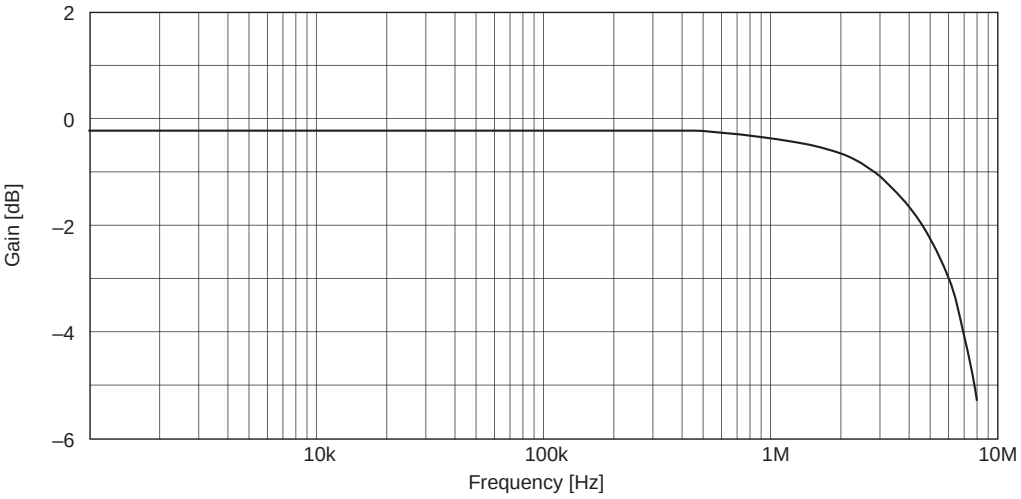
Frequency response vs. Supply voltage



Differential gain vs. Supply voltage



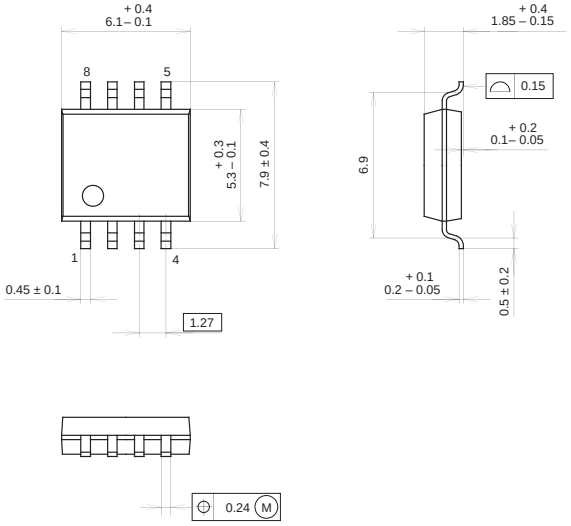
Frequency response



Package Outline Unit: mm

CXL5504M

8PIN SOP (PLASTIC)

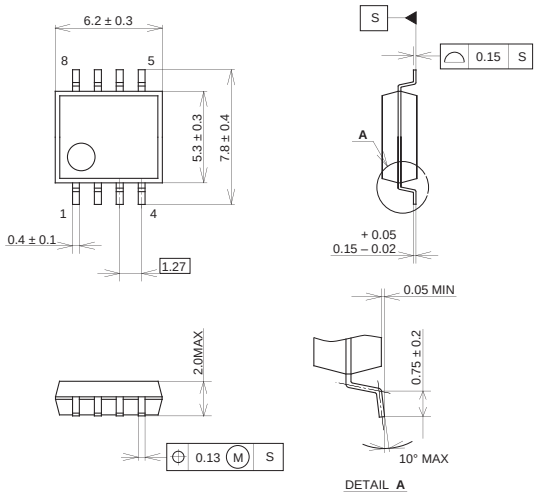


SONY CODE	SOP-8P-L01
EIAJ CODE	SOP008-P-0300
JEDEC CODE	

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.1g

8PIN SOP (PLASTIC)



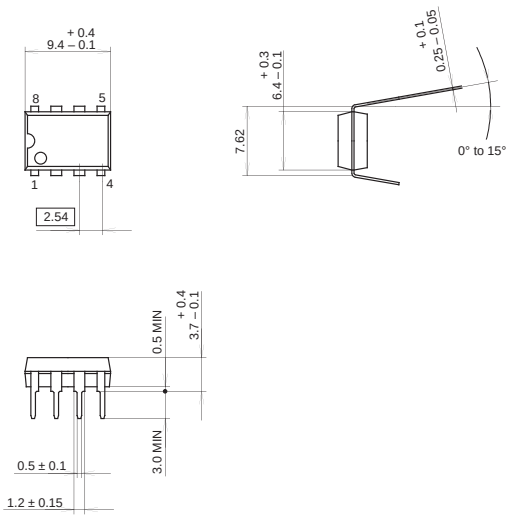
SONY CODE	SOP-8P-L121
EIAJ CODE	SOP008-P-0300
JEDEC CODE	

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.1g

CXL5504P

8PIN DIP (PLASTIC)



SONY CODE	DIP-8P-01
EIAJ CODE	DIP008-P-0300
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.5g