100mA, Low Noise Linear Regulator With Precision Current Limit And Diagnostic Functions

FEATURES

- **Output Current: 100mA**
- **Dropout Voltage: 340mV**
- **Input Voltage Range: 1.6V to 45V**
- **Programmable Precision Current Limit: ±5%**
- **Programmable Minimum I_{OUT} Monitor**
- **Output Current Monitor: 1/100th of I_{OUT}**
- **Fault Indicator: Current Limit, Minimum I_{OUT} or Thermal Limit**
- **Low Noise: 30µV_{RMS} (10Hz to 100kHz)**
- Adjustable Output (V_{REF} = $V_{OUT(MIN)}$ = 0.6V)
- Output Tolerance: ±2% Over Line, Load and Temperature
- Stable with Low ESR, Ceramic Output Capacitors (2.2µF minimum)
- Shutdown Current: <1µA
- Reverse-Battery, Reverse-Output and Reverse-Current Protection
- Thermal Limit Protection
- 12-Lead 3mm × 2mm DFN and MSOP Packages

APPLICATIONS

- Protected Antenna Supplies
- Automotive Telematics
- Industrial Applications (Trucks, Forklifts, etc.)
- High Reliability Applications

DESCRIPTION

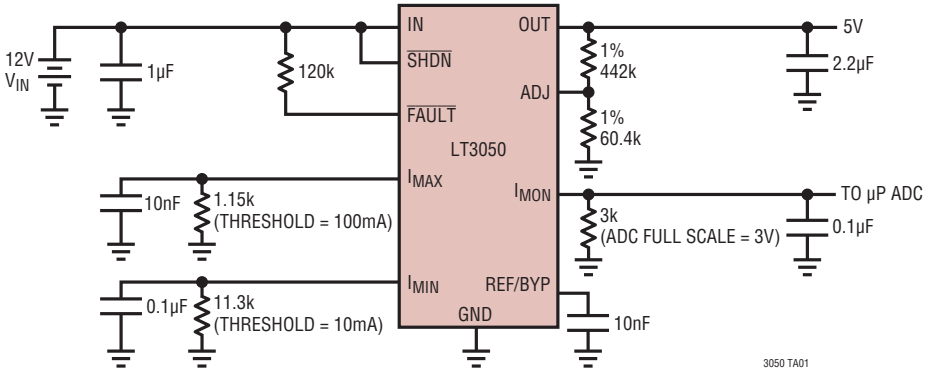
The LT®3050 is a micro-power, low noise, low dropout voltage (LDO) linear regulator. The device supplies 100mA of output current with a dropout voltage of 340mV. A 10nF bypass capacitor reduces output noise to 30µV_{RMS} in a 10Hz to 100kHz bandwidth and soft-starts the reference. The LT3050's ±45V input voltage rating combined with its precision current limit and diagnostic functions make the IC an ideal choice for robust, high reliability applications.

A single resistor programs the LT3050's current limit, accurate to ±5% over a wide input voltage and temperature range. A single resistor programs the LT3050's minimum output current monitor, useful for detecting open-circuit conditions. The current monitor function sources a current equal to 1/100th of output current. A logic $\overline{FAULT}$ pin asserts low if the LT3050 is in current limit, operating below its minimum output current (open-circuit) or is in thermal shutdown.

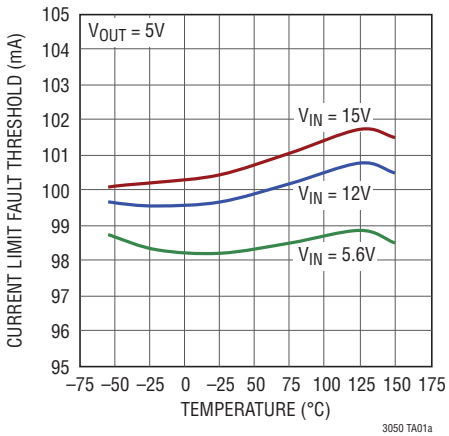
The LT3050 optimizes stability and transient response with low ESR ceramic capacitors, requiring a minimum of 2.2µF. The LT3050 is available as an adjustable device with an output voltage range down to the 0.6V reference. The LT3050 is available in the thermally-enhanced 12-Lead 3mm × 2mm DFN and MSOP packages.

TYPICAL APPLICATION

5V Supply with 100mA Precision Current Limit, 10mA I_{MIN}



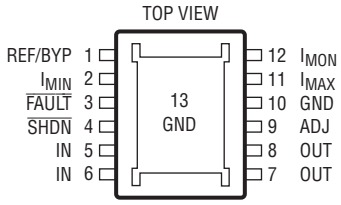
External Current Limit
R_{IMAX} = 1.15k



ABSOLUTE MAXIMUM RATINGS (Note 1)

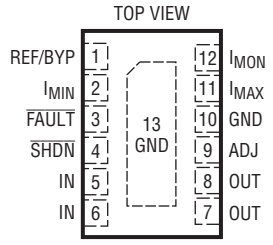
IN Pin Voltage ..... ±50V
OUT Pin Voltage ..... ±50V
Input-to-Output Differential Voltage ..... ±50V
ADJ Pin Voltage ..... ±50V
REF/BYP Pin Voltage ..... –0.3V, 1V
$\overline{SHDN}$ Pin Voltage ..... ±50V
I_{MON} Pin Voltage ..... –0.3V, 7V
I_{MIN} Pin Voltage ..... –0.3V, 7V
I_{MAX} Pin Voltage ..... –0.3V, 7V
$\overline{FAULT}$ Pin Voltage ..... –0.3V, 50V
Output Short-Circuit Duration ..... Indefinite
Operating Junction Temperature Range (Notes 2, 3)
E, I Grades ..... –40°C to 125°C
MP Grade ..... –55°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature: Soldering, 10 sec ..... 300°C
(MSOP Package Only)

PIN CONFIGURATION



MSE PACKAGE
12-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 45°C/W, θ_{JC} = 5°C/W TO 10°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB



DDB PACKAGE
12-LEAD (3mm × 2mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 49°C/W, θ_{JC} = 13.5°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3050EMSE#PBF	LT3050EMSE#TRPBF	3050	12-Lead Plastic MSOP	–40°C to 125°C
LT3050IMSE#PBF	LT3050IMSE#TRPBF	3050	12-Lead Plastic MSOP	–40°C to 125°C
LT3050MPMSE#PBF	LT3050MPMSE#TRPBF	3050	12-Lead Plastic MSOP	–55°C to 125°C
LT3050EDDB#PBF	LT3050EDDB#TRPBF	LFGC	12-Lead (3mm × 2mm) Plastic DFN	–40°C to 125°C
LT3050IDDB#PBF	LT3050IDDB#TRPBF	LFGC	12-Lead (3mm × 2mm) Plastic DFN	–40°C to 125°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LT3050EMSE	LT3050EMSE#TR	3050	12-Lead Plastic MSOP	–40°C to 125°C
LT3050IMSE	LT3050IMSE#TR	3050	12-Lead Plastic MSOP	–40°C to 125°C
LT3050MPMSE	LT3050MPMSE#TR	3050	12-Lead Plastic MSOP	–55°C to 125°C
LT3050EDDB	LT3050EDDB#TR	LFGC	12-Lead (3mm × 2mm) Plastic DFN	–40°C to 125°C
LT3050IDDB	LT3050IDDB#TR	LFGC	12-Lead (3mm × 2mm) Plastic DFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage (Notes 3, 11)	I_{LOAD} = 100mA	●		1.6	2.2	V
ADJ Pin Voltage (Notes 3, 4)	V_{IN} = 2.2V, I_{LOAD} = 1mA		594	600	606	mV
	2.2V < V_{IN} < 15V, 1mA < I_{LOAD} < 100mA (Note 15)	●	588		612	mV
Line Regulation (Note 3)	ΔV_{IN} = 2.2V to 45V, I_{LOAD} = 1mA	●		0.25	3	mV
Load Regulation (Note 3)	V_{IN} = 2.2V, I_{LOAD} = 1mA to 100mA	●		0.2	4	mV
Dropout Voltage V_{IN} = $V_{OUT(NOMINAL)}$ (Notes 5, 6)	I_{LOAD} = 1mA			110	150	mV
	I_{LOAD} = 1mA	●			220	mV
	I_{LOAD} = 10mA			195	240	mV
	I_{LOAD} = 10mA	●			340	mV
	I_{LOAD} = 50mA			280	330	mV
	I_{LOAD} = 50mA	●			450	mV
	I_{LOAD} = 100mA			340	400	mV
	I_{LOAD} = 100mA	●			550	mV
GND Pin Current V_{IN} = $V_{OUT(NOMINAL)}$ + 0.6V (Notes 6, 7, 11)	I_{LOAD} = 0mA	●		45	90	µA
	I_{LOAD} = 1mA	●		60	160	µA
	I_{LOAD} = 10mA	●		175	370	µA
	I_{LOAD} = 50mA	●		0.85	2	mA
	I_{LOAD} = 100mA	●		2.2	5.2	mA
Quiescent Current in Shutdown	V_{IN} = 12V, $V_{\overline{SHDN}}$ = 0V			0.17	1	µA
ADJ Pin Bias Current (Notes 3, 12)	V_{IN} = 12V	●		12.5	60	nA
Output Voltage Noise	C_{OUT} = 10µF, I_{LOAD} = 100mA, V_{OUT} = 600mV, BW = 10Hz to 100kHz			90		μV_{RMS}
Output Voltage Noise	C_{OUT} = 10µF, C_{BYP} = 0.01µF, I_{LOAD} = 100mA, V_{OUT} = 600mV BW = 10Hz to 100kHz			30		μV_{RMS}
Shutdown Threshold	V_{OUT} = Off to On	●		0.7	1.5	V
	V_{OUT} = On to Off	●	0.3	0.6		V
$\overline{SHDN}$ Pin Current (Note 13)	$V_{\overline{SHDN}}$ = 0V	●			1	µA
	$V_{\overline{SHDN}}$ = 45V	●		0.9	3	µA
Ripple Rejection (Note 3)	V_{IN} – V_{OUT} = 2V (AVG), V_{RIPPLE} = 0.5V_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 100mA		70	85		dB
$\overline{FAULT}$ Pin Logic Low Voltage	V_{IN} = 2.2V, $\overline{FAULT}$ Asserted, $I_{\overline{FAULT}}$ = 100µA	●		140	250	mV
$\overline{FAULT}$ Pin Leakage Current	$\overline{FAULT}$ = 5V, $\overline{FAULT}$ Not Asserted			0.01	1	µA
Input Reverse Leakage Current	V_{IN} = –45V, V_{OUT} = 0	●			300	µA
Reverse Output Current (Note 14)	V_{OUT} = 1.2V, V_{IN} = 0			0.2	10	µA
Internal Current Limit (Note 3)	V_{IN} = 2.2V, V_{OUT} = 0, I_{MAX} Pin Grounded			240		mA
	ΔV_{OUT} = –5%	●	110			
External Programmed Current Limit (Note 8)	5.6V < V_{IN} < 15V, V_{OUT} = 5V, R_{IMAX} = 2.26K $\overline{FAULT}$ Pin Threshold	●	47.8	50.4	52.9	mA
	5.6V < V_{IN} < 15V, V_{OUT} = 5V, R_{IMAX} = 1.5K $\overline{FAULT}$ Pin Threshold	●	72.1	75.9	79.7	mA
	5.6V < V_{IN} < 15V, V_{OUT} = 5V, R_{IMAX} = 1.15K $\overline{FAULT}$ Pin Threshold	●	94.4	99.3	104.3	mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum I_{MIN} Threshold Accuracy (Note 9)	5.6V < V_{IN} < 15V, V_{OUT} = 5V, R_{IMIN} = 110K	●	0.9	1	1.1	mA
I_{MIN} Threshold Accuracy (Note 9)	5.6V < V_{IN} < 15V, V_{OUT} = 5V, R_{IMIN} = 11.3K	●	9	10	11	mA
Current Monitor Ratio (Note10) Ratio = I_{OUT}/I_{MON} V_{IMON} = V_{OUT} = 5V, 5.6V < V_{IN} < 15V	I_{LOAD} = 5mA, 25mA, 50mA, 75mA, 100mA	●	95	100	105	

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime. Absolute maximum input-to-output differential voltage is not achievable with all combinations of rated IN pin and OUT pin voltages. With the IN pin at 50V, the OUT pin may not be pulled below 0V. The total differential voltage from IN to OUT must not exceed ±50V.

Note 2: The LT3050 is tested and specified under pulse load conditions such that $T_J \sim T_A$. The LT3050E is 100% production tested at T_A = 25°C. Performance at –40°C and 125°C is assured by design, characterization and correlation with statistical process controls. The LT3050I is guaranteed over the full –40°C to 125°C operating junction temperature range. The LT3050MP is 100% tested over the –55°C to 125°C operating junction temperature range.

Note 3: The LT3050 is tested and specified for these conditions with ADJ pin connected to the OUT pin.

Note 4: Maximum junction temperature limits operating conditions. Regulated output voltage specifications do not apply for all possible combinations of input voltage and output current. If operating at the maximum input voltage, limit the output current range. If operating at the maximum output current, limit the input voltage range.

Note 5: Dropout voltage is the minimum differential IN-to-OUT voltage needed to maintain regulation at a specified output current. In dropout, the output voltage equals (V_{IN} - $V_{DROPOUT}$). For some output voltages, minimum input voltage requirements limit dropout voltage.

Note 6: To satisfy minimum input voltage requirements, the LT3050 is tested and specified for these conditions with an external resistor divider (60k bottom, 440k top) which sets V_{OUT} to 5V. The external resistor divider adds 10µA of DC load on the output. This external current is not factored into GND pin current.

Note 7: GND pin current is tested with V_{IN} = $V_{OUT(NOMINAL)}$ + 0.5V and a current source load. GND pin current increases in dropout. See GND pin current curves in the Typical Performance Characteristics section.

Note 8: Current limit varies inversely with the external resistor value tied from the I_{MAX} pin to GND. For detailed information on how to set the I_{MAX} pin resistor value, please see the Operation section. If a programmed current limit is not needed, the I_{MAX} pin must be tied to GND and internal protection circuitry implements short-circuit protection as specified.

Note 9: The I_{MIN} fault condition asserts if the output current falls below the I_{MIN} threshold defined by an external resistor from the I_{MIN} pin to GND. For detailed information on how to set the I_{MIN} pin resistor value, please see the Operation section. I_{MIN} settings below the Minimum I_{MIN} Accuracy specification in the Electrical Characteristics section are not guaranteed to ± 10% tolerance. If the I_{MIN} fault condition is not needed, the I_{MIN} pin must be left floating (unconnected).

Note 10: The current monitor ratio varies slightly when $V_{IMON} \neq V_{OUT}$. For detailed information on how to calculate the output current from the I_{MON} pin, please see the Operation section. If the current monitor function is not needed, the I_{MON} pin must be tied to GND.

Note 11: To satisfy requirements for minimum input voltage, current limit is tested at V_{IN} = $V_{OUT(NOMINAL)}$ +1V or V_{IN} = 2.2V, whichever is greater.

Note 12: ADJ pin bias current flows out of the ADJ pin:

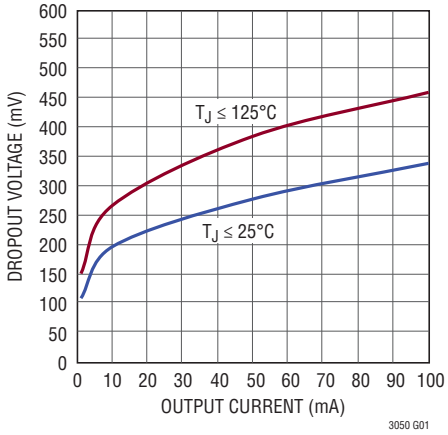
Note 13: $\overline{SHDN}$ pin current flows into the $\overline{SHDN}$ pin.

Note 14: Reverse output current is tested with the IN pin grounded and the OUT pin forced to the specified voltage. This current flows into the OUT pin and out of the GND pin.

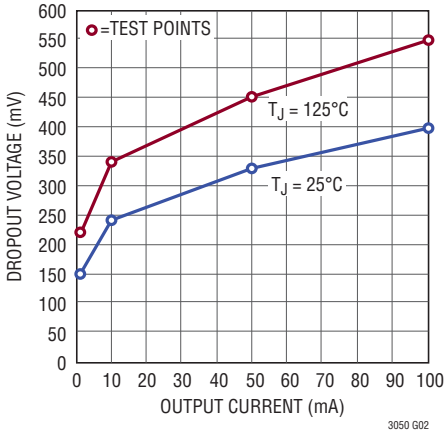
Note 15: 100mA of output current does not apply to the full range of input voltage due to the internal current limit foldback.

TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

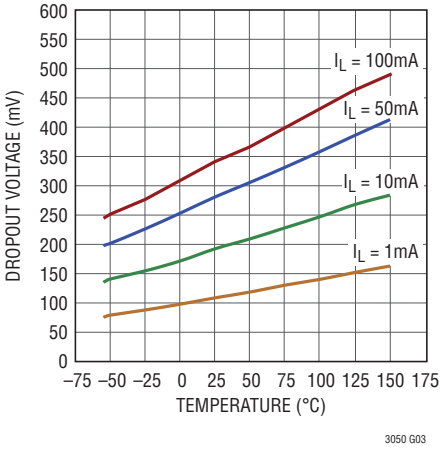
Typical Dropout Voltage



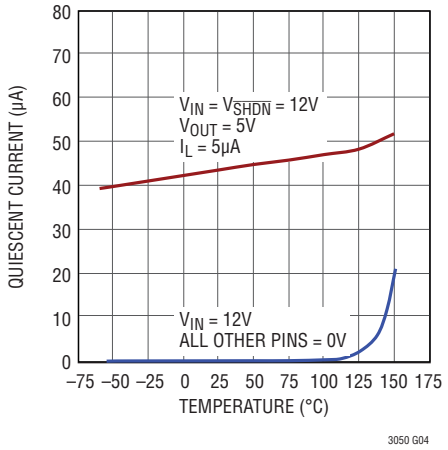
Guaranteed Dropout Voltage



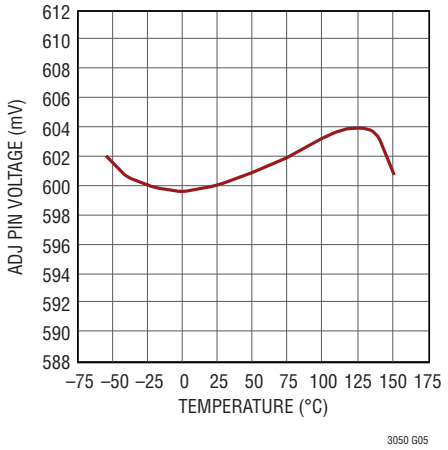
Dropout Voltage



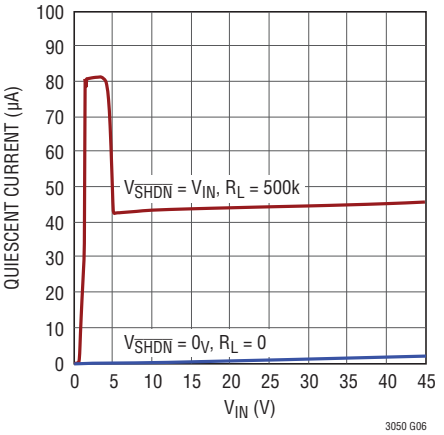
Quiescent Current



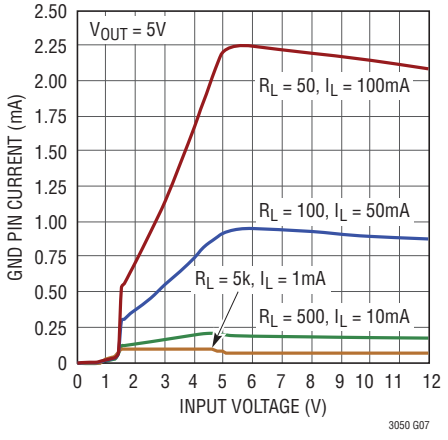
ADJ Pin Voltage



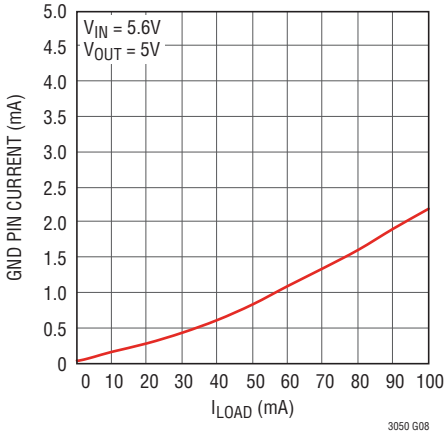
5V Quiescent Current



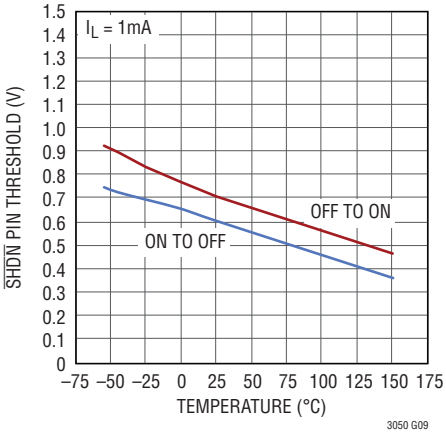
GND Pin Current



GND Pin Current vs I_{LOAD}

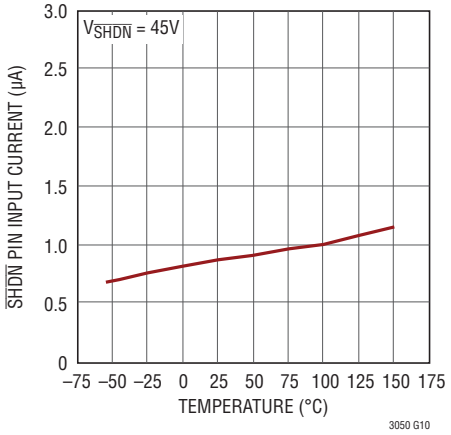


$\overline{SHDN}$ Pin Threshold

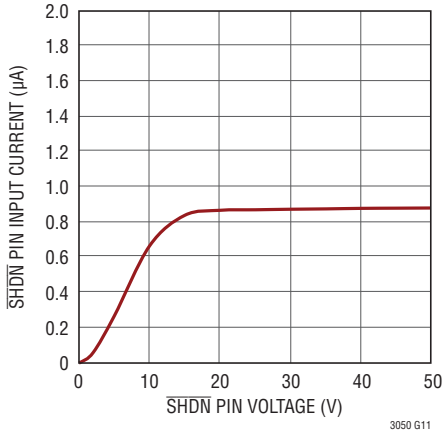


TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

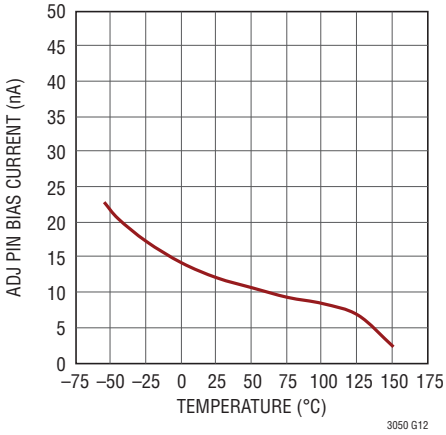
$\overline{SHDN}$ Pin Input Current



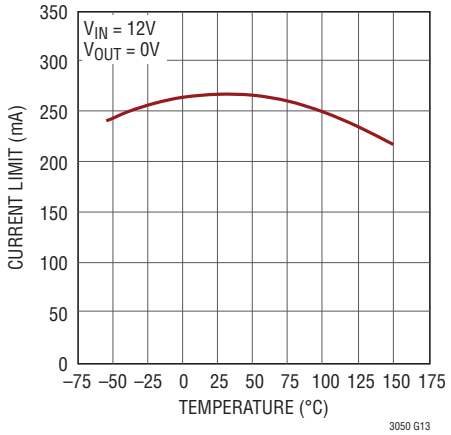
$\overline{SHDN}$ Pin Input Current



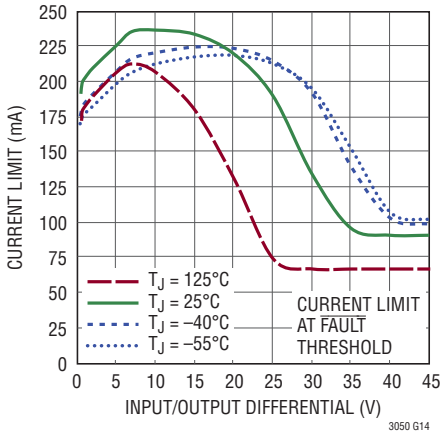
ADJ Pin Bias Current



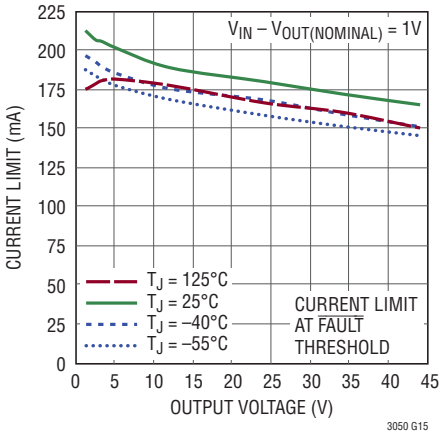
Internal Current Limit



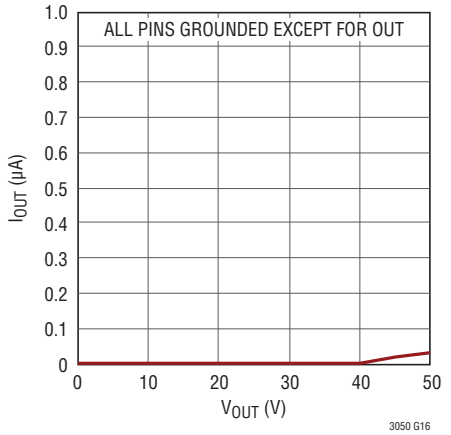
Internal Current Limit



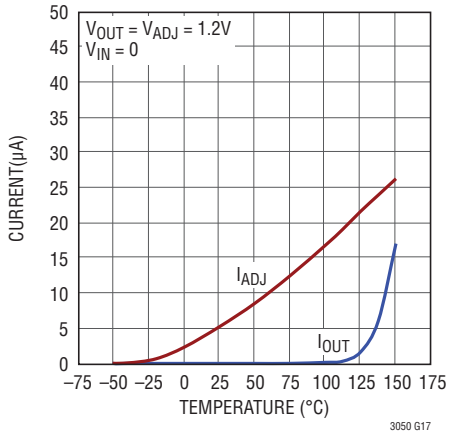
Internal Current Limit vs Output Voltage



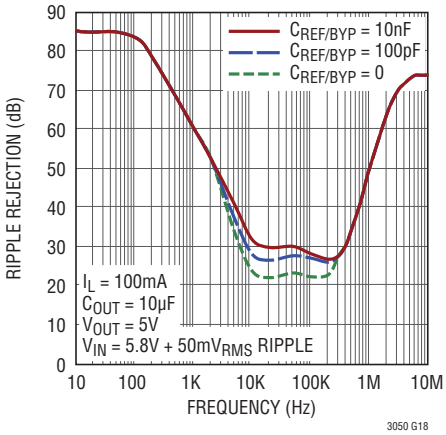
Reverse Output Current



Reverse Output Current

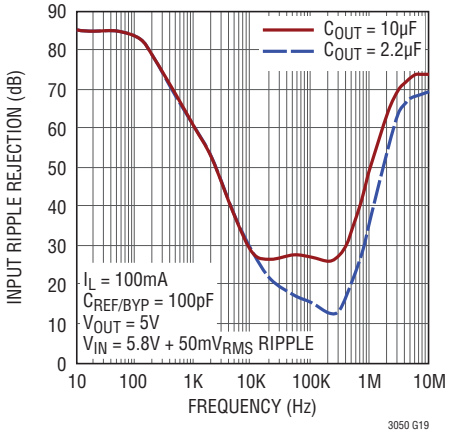


Input Ripple Rejection

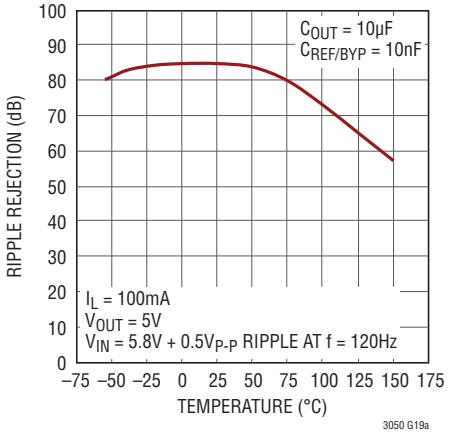


TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

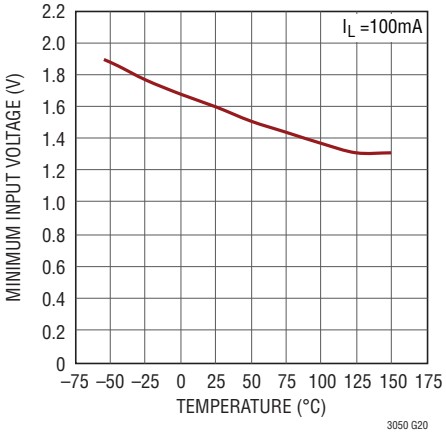
Input Ripple Rejection



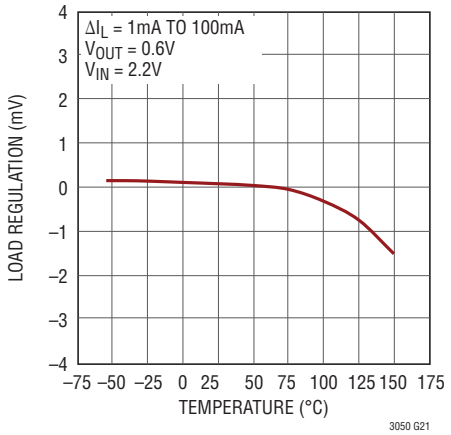
Ripple Rejection vs Temperature



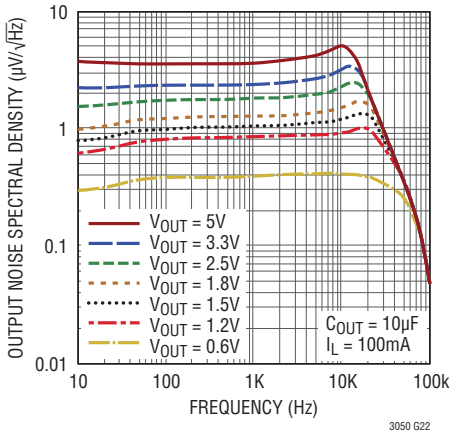
Minimum Input Voltage



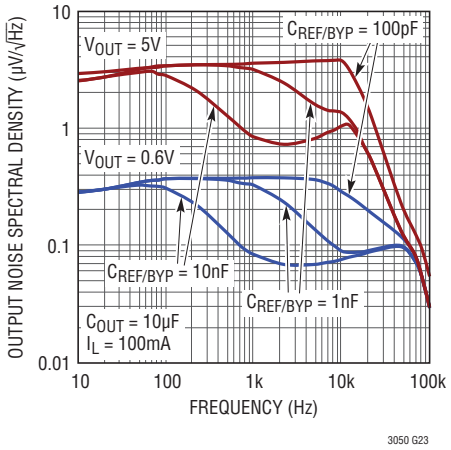
Load Regulation



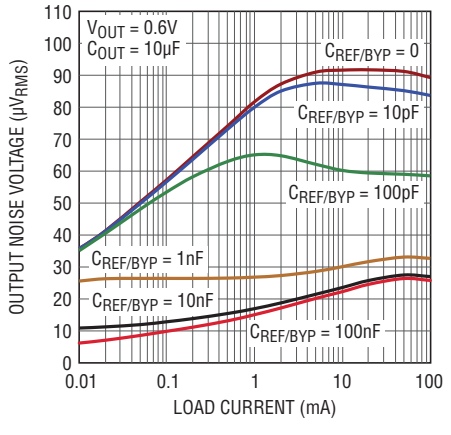
Output Noise Spectral Density $C_{REF/BYP}$ = 0



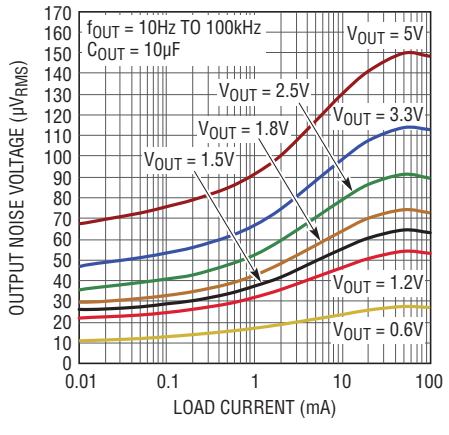
Output Noise Spectral Density vs $C_{REF/BYP}$



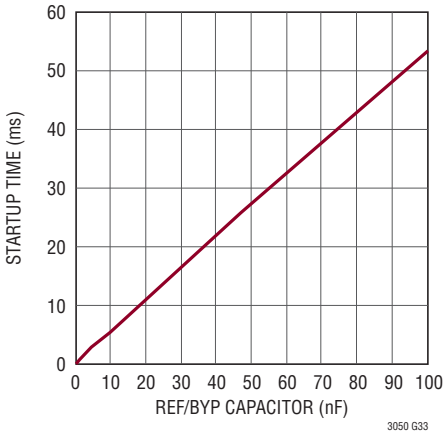
RMS Output Noise vs Load Current vs $C_{REF/BYP}$



RMS Output Noise vs Load Current $C_{REF/BYP}$ = 10nF

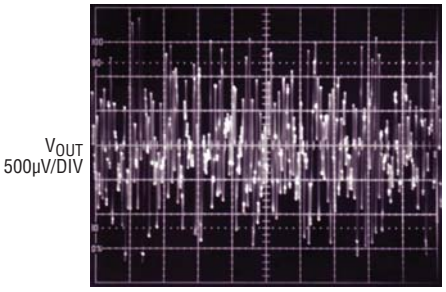


Startup Time vs REF/BYP Capacitor

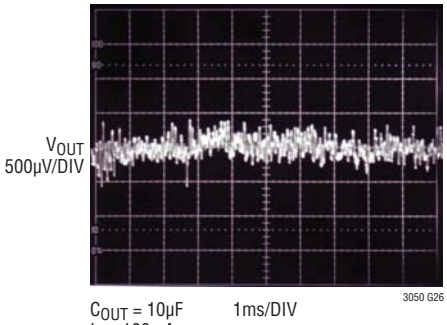


TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

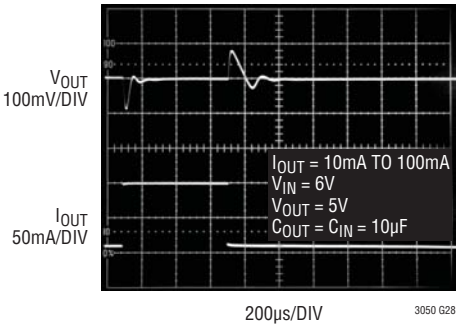
5V 10Hz to 100kHz Output Noise
$C_{REF/BYP}$ = 0



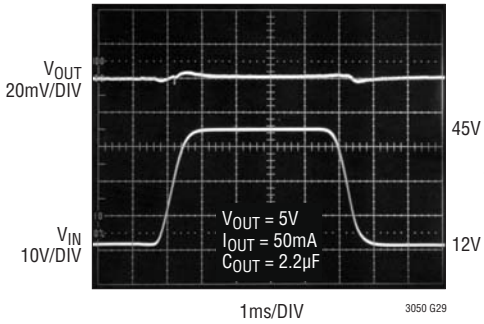
5V 10Hz to 100kHz Output Noise
$C_{REF/BYP}$ = 10nF



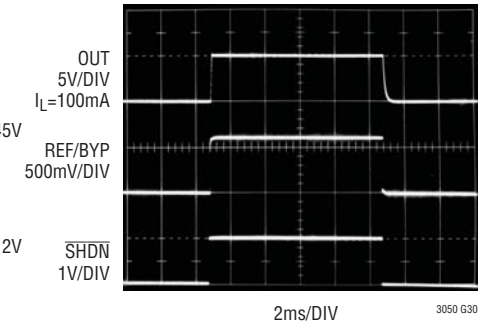
Transient Response



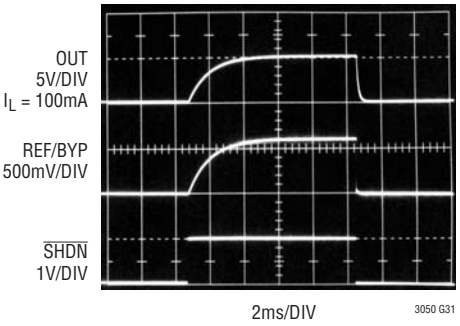
Transient Response (Load Dump)



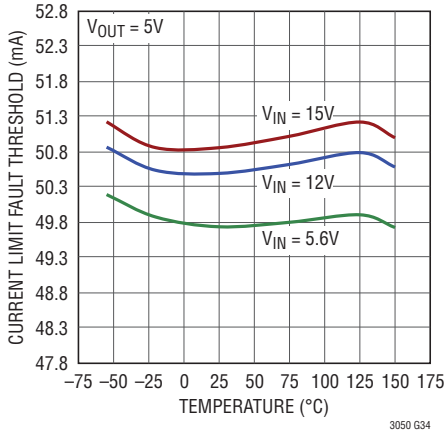
$\overline{SHDN}$ Transient Response
$C_{REF/BYP}$ =0



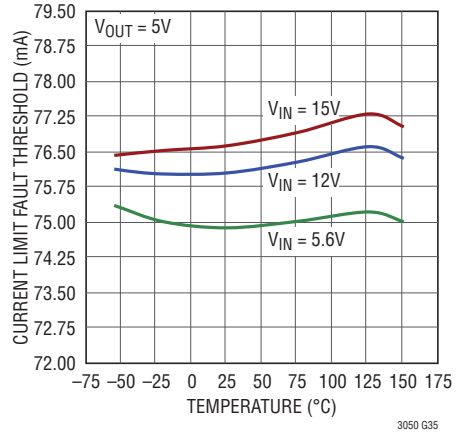
$\overline{SHDN}$ Transient Response
$C_{REF/BYP}$ = 10nF



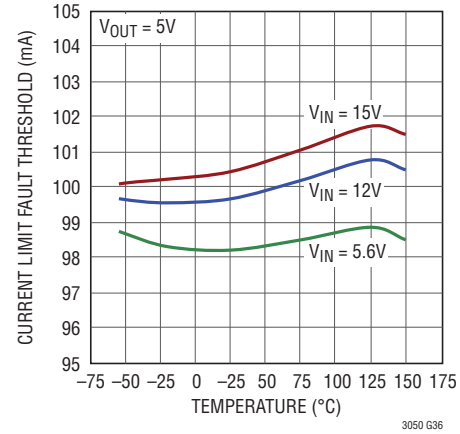
External Current Limit
R_{IMAX} = 2.26k



External Current Limit
R_{IMAX} = 1.5k

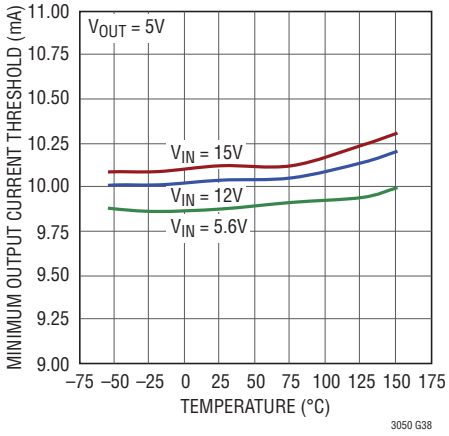


External Current Limit
R_{IMAX} = 1.5k

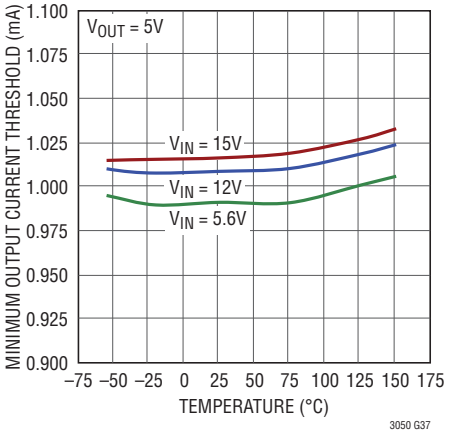


TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

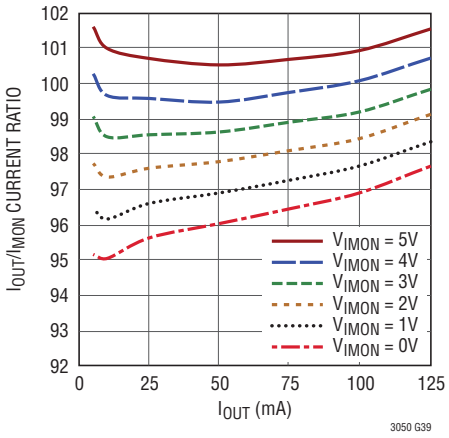
Minimum Output Current Threshold R_{IMIN} = 11.3k



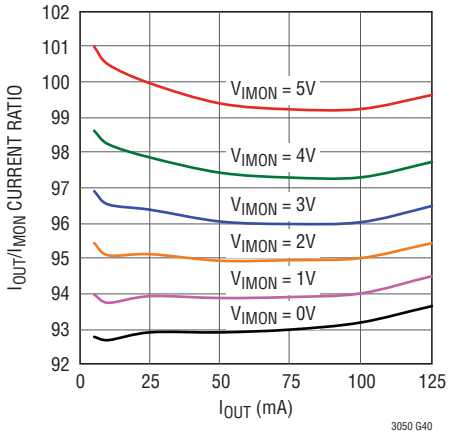
Minimum Output Current Threshold R_{IMIN} = 110k



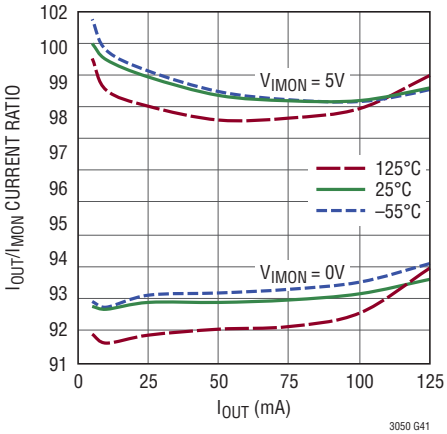
I_{OUT}/I_{MON} Current Ratio V_{OUT} = 5V, V_{IN} = 12V



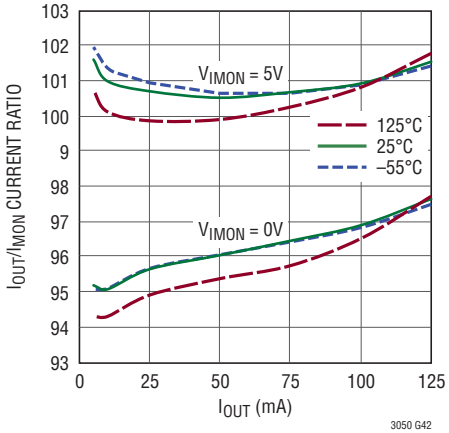
I_{OUT}/I_{MON} Current Ratio V_{OUT} = 5, V_{IN} = 5.6V



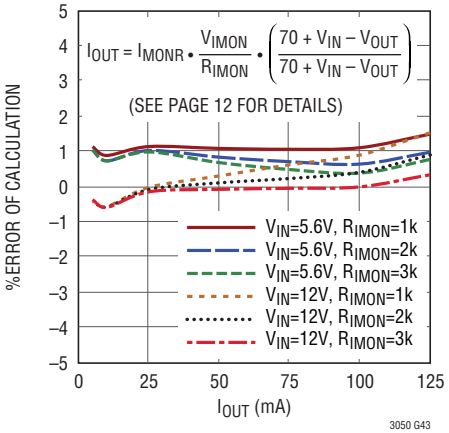
I_{OUT}/I_{MON} Current Ratio V_{OUT} = 5V, V_{IN} = 5.6V



I_{OUT}/I_{MON} Current Ratio V_{OUT} = 5V, V_{IN} = 12V



I_{OUT} Calculated From I_{MON} V_{OUT} = 5V



PIN FUNCTIONS

REF/BYP (Pin 1): Bypass/Soft-Start. Connecting a single capacitor from this pin to GND bypasses the LT3050's reference noise and soft-starts the reference. A 10nF bypass capacitor typically reduces output voltage noise to $30\mu V_{RMS}$ in a 10Hz to 100kHz bandwidth. Soft-start time is directly proportional to the REF/BYP capacitor value. If the LT3050 is placed in shutdown, REF/BYP is actively pulled low by an internal device to reset soft-start. If low noise or soft-start performance is not required, this pin must be left floating (unconnected). Do not drive this pin with any active circuitry. Because the REF/BYP pin is the reference input to the error amplifier, stray capacitance at this point should be minimized. Special attention should be given to any stray capacitances that can couple external signals onto the REF/BYP pin producing undesirable output transients or ripple. A minimum REF/BYP capacitance of 100pF is recommended.

I_{MIN} (Pin 2): Minimum Output Current Programming Pin. This pin is the collector of a PNP current mirror that outputs 1/200th of the power PNP load current. This pin is also the input to the minimum output current fault comparator. Connecting a resistor between I_{MIN} and GND sets the minimum output current fault threshold. For detailed information on how to set the I_{MIN} pin resistor value, please see the Operation section.

A small external decoupling capacitor (10nF minimum) is required to improve I_{MIN} PSRR. If minimum output current programming is not required, the I_{MIN} pin must be left floating (unconnected).

$\overline{\text{FAULT}}$ (Pin 3): $\overline{\text{Fault}}$ Pin. This is an open collector logic pin which asserts during current limit, thermal limit or a minimum current fault condition. The maximum low logic output level is defined for sinking 100µA of current. Off state logic may be as high as 45V without damaging internal circuitry regardless of the V_{IN} used.

$\overline{\text{SHDN}}$ (Pin 4): Shutdown. Pulling the $\overline{\text{SHDN}}$ pin low puts the LT3050 into a low power state and turns the output off. Drive the $\overline{\text{SHDN}}$ pin with either logic or an open collector/drain with a pull-up resistor. The resistor supplies the pull-up current to the open collector/drain logic, normally several microamperes, and the $\overline{\text{SHDN}}$ pin current, typically less than 2µA. If unused, connect the $\overline{\text{SHDN}}$ pin to IN. The LT3050 does not function if the $\overline{\text{SHDN}}$ pin is not connected. The $\overline{\text{SHDN}}$ pin cannot be driven below GND unless tied to the IN pin. If the $\overline{\text{SHDN}}$ pin is driven below GND while IN is powered, the output may turn on. $\overline{\text{SHDN}}$ pin logic cannot be referenced to a negative rail.

IN (Pin 5,6): Input. These pins supply power to the device. The LT3050 requires a local IN bypass capacitor if it is located more than six inches from the main input filter capacitor. In general, battery output impedance rises with frequency, so adding a bypass capacitor in battery powered circuits is advisable. A minimum input of 1µF generally suffices.

OUT (Pin 7,8): Output. These pins supply power to the load. Stability requirements demand a minimum 2.2µF ceramic output capacitor to prevent oscillations. Large load transient applications require larger output capacitors to limit peak voltage transients. See the Applications Information section for details on transient response and reverse output characteristics. Permissible output voltage range is 600mV to 44.5V.

ADJ (Pin 9): Adjust. This pin is the error amplifier's inverting terminal. Its typical bias of 16nA current flows out of the pin (see curve of ADJ Pin Bias Current vs. Temperature in the Typical Performance Characteristics section). The typical ADJ pin voltage is 600mV referenced to GND.

GND (PIN 10, Exposed Pad Pin 13): Ground. The exposed pad of the DFN and MSOP packages is an electrical connection to GND. To ensure proper electrical and thermal performance, solder Pin 13 to the PCB ground and tie directly to Pin 10. Connect the bottom of the output voltage setting resistor divider directly to GND (Pin 10) for optimum load regulation performance.

I_{MAX} (Pin 11): Precision Current Limit Programming Pin. This pin is the collector of a current mirror PNP that is 1/200th the size of the output power PNP. This pin is also the input to the current limit amplifier. Current limit threshold is set by connecting a resistor between the I_{MAX} pin and GND.

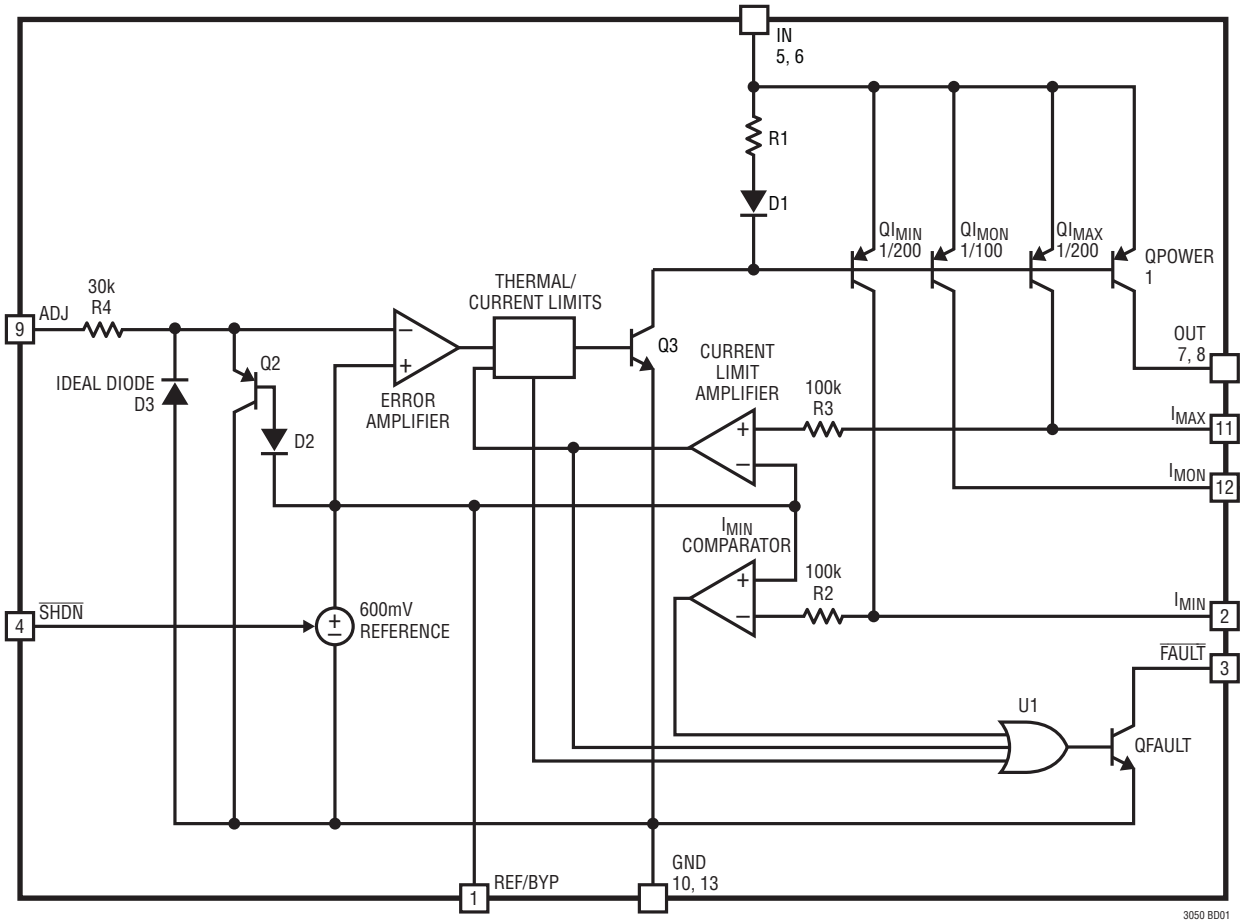
PIN FUNCTIONS

For detailed information on how to set the I_{MIN} pin resistor value, please see the Operation section.

The I_{MAX} pin requires a 10nF decoupling capacitor to ground. If not used, tie I_{MAX} to GND.

I_{MON} (Pin 12): Output Current Monitor. This pin is the collector of a PNP current mirror that outputs 1/100th of the power PNP current. When OUT = I_{MON}, the pin current exactly equals 1/100th that of the output current. For detailed information on how to calculate the output current from the I_{MON} pin, please see the Operation section. The I_{MON} pin requires a small (22nF minimum) external decoupling capacitor. If the I_{MON} pin is not used, it must be tied to GND.

BLOCK DIAGRAM



OPERATION

I_{MON} Pin Operation (Current Monitor)

The I_{MON} pin is the collector of a PNP which mirrors the LT3050 output PNP at a ratio of 1:100 (see block diagram on page 11). The current sourced by the I_{MON} pin is ~1/100th of the current sourced by the OUT pin when the I_{MON} and OUT pin voltages are equal and the device is not operating in dropout. If the I_{MON} and OUT pin voltages are not the same, the ratio deviates from 1/100 due to the Early voltages of the I_{MON} and OUT PNPs according to the equation:

$$\frac{I_{IMON}}{I_{OUT}} = \frac{1}{I_{MONR}} \bullet \underbrace{\left(\frac{70 + V_{IN} - V_{IMON}}{70 + V_{IN} - V_{OUT}}\right)}_{\text{Early Voltage Compensation}}$$

where the Early voltage of the PNPs is 70V and I_{MONR} is a variable which represents the I_{OUT} to I_{MON} current ratio. I_{MONR} varies with V_{IN} to V_{OUT} voltage according to the empirically derived equation:

$I_{MONR} = 97 + 5 \bullet \log_{10}(1+V_{IN} - V_{OUT})$ for $(V_{IN} - V_{OUT}) \geq 0.5$

$I_{MONR} = 96 + 2 \bullet (V_{IN} - V_{OUT})$ for $(V_{IN} - V_{OUT}) < 0.5$

The I_{MON} pin current can be converted into a voltage for use by monitoring circuitry simply by connecting the I_{MON} pin to a resistor.

Connecting a resistor from I_{MON} to GND converts the I_{MON} pin current into a voltage that can be monitored by circuitry such as an ADC.

For example, a 1.2k resistor results in a I_{MON} pin voltage of 1.2V for an output current of 100mA and an output voltage of 1.2V.

The output current of the device can be calculated from the I_{MON} pin voltage by the following equation:

$$I_{OUT} = \underbrace{\frac{I_{MONR}}{\frac{I_{OUT}}{I_{MON}}\text{Ratio}}} \bullet \underbrace{\frac{V_{IMON}}{R_{IMON}}}_{I_{IMON}} \bullet \underbrace{\left(\frac{70 + V_{IN} - V_{OUT}}{70 + V_{IN} - V_{IMON}}\right)}_{\text{Early Voltage Compensation}}$$

A small decoupling capacitor (22nF minimum) from I_{MON} to GND is required to improve I_{MON} pin power supply rejection. If the current monitor is not needed, it must be tied to GND.

Open Circuit Detection (I_{MIN} Pin)

The I_{MIN} pin is the collector of a PNP which mirrors the LT3050 output at a ratio of approximately 1:200 (see block diagram on page 11). The I_{MIN} fault comparator asserts the $\overline{FAULT}$ pin if the I_{MIN} pin voltage is below 0.6V. This low output current fault threshold voltage (I_{OPEN}) is set by attaching a resistor from I_{MIN} to GND.

$$R_{IMIN} = \frac{119.85 - (1.68 - 36.8 \bullet I_{OPEN}) \bullet V_{OUT}}{I_{OPEN}}$$

This equation is empirically derived and partially compensates for early voltage effects in the I_{MIN} current mirror. It is valid for an input voltage range from 0.6V above the output to 10V above the output. It is valid for output voltages up to 12V. The accuracy of this equation for setting the resistor value is approximately ±2%. Unit values are Amps, Volts, and Ohms.

If the open circuit detection function is not needed, the I_{MIN} pin must be left floating (unconnected). A small decoupling capacitor (10nF minimum) from I_{MIN} to GND is required to improve I_{MIN} pin power supply rejection and to prevent $\overline{FAULT}$ pin glitches.

See the Typical Performance Characteristics section for additional information.

OPERATION

External Programmable Current Limit (I_{MAX} Pin)

The I_{MAX} pin is the collector of a PNP which mirrors the LT3050 output at a ratio of approximately 1:200 (see Block Diagram). The I_{MAX} pin is also the input to the precision current limit amplifier. If the output load increases to the point where it causes the I_{MAX} pin voltage to reach 0.6V, the current limit amplifier takes control of output regulation so that the I_{MAX} pin clamps at 0.6V, regardless of the output voltage. The current limit threshold (I_{LIMIT}) is set by attaching a resistor (R_{IMAX}) from I_{MAX} to GND:

$$R_{IMAX} = \frac{119.22 - 0.894 \bullet V_{OUT}}{I_{LIMIT}}$$

This equation is empirically derived and partially compensates for early voltage effects in the I_{MAX} current mirror. It is valid for an input voltage range from 0.6V above the output to 10V above the output. It is valid for output voltages up to 12V. The accuracy of this equation for setting the resistor value is approximately ±1%. Unit values are Amps, Volts, and Ohms.

In cases where the IN to OUT voltage exceeds 10V, fold-back current limit will lower the internal current level limit, possibly causing it to preempt the external programmable current limit. See the Internal Current Limit vs $V_{IN} – V_{OUT}$ graph in the Typical Performance Characteristics section.

If the external programmable current limit is not needed, the I_{MAX} pin must be connected to GND. The I_{MAX} pin requires a 10nF decoupling capacitor.

See the Typical Performance Characteristics section for additional information.

$\overline{\text{FAULT}}$ Pin Operation

The $\overline{\text{FAULT}}$ pin is an open collector logic pin which asserts during internal current limit, precision current limit, thermal limit, or a minimum current fault. There is no internal pull-up on the $\overline{\text{FAULT}}$ pin; an external pull-up resistor is required. The $\overline{\text{FAULT}}$ pin provides drive for up to 100µA of pull-down current. Off state logic may be as high as 45V, regardless of the input voltage used. When asserted, the $\overline{\text{FAULT}}$ pin drive circuitry adds 50µA (nominal) of GND pin current.

Depending on the I_{MIN} capacitance, BYP capacitance, and OUT capacitance, the $\overline{\text{FAULT}}$ pin may assert during startup. Consideration should be given to masking the $\overline{\text{FAULT}}$ signal during startup. The $\overline{\text{FAULT}}$ pin circuitry is inactive (not asserted) during shutdown and when the OUT pin is pulled above the IN pin.

Operation in Dropout

The LT3050 contains circuitry which prevents the PNP output power device from saturating in dropout. This also keeps the I_{MON}, I_{MIN}, and I_{MAX} current mirrors functioning accurately, even in dropout. However, this anti-saturation circuitry becomes less active at lower output currents, so there is some degradation of current mirror function for output currents less than 10mA.

APPLICATIONS INFORMATION

The LT3050 is a micropower, low noise and low dropout voltage, 100mA linear regulator with micropower shutdown, programmable current limit, and diagnostic functions. The device supplies up to 100mA at a typical dropout voltage of 340mV and operates over a 2.2V to 45V input range.

A single external capacitor can provide low noise reference performance and output soft-start functionality. For example, connecting a 10nF capacitor from the REF/BYP pin to GND lowers output noise to 30μV_{RMS} over a 10Hz to 100kHz bandwidth. This capacitor also soft-starts the reference and prevents output voltage overshoot at turn-on.

The LT3050's quiescent current is merely 45μA but provides fast transient response with a minimum low ESR 2.2μF ceramic output capacitor. In shutdown, quiescent current is less than 1μA and the reference soft-start capacitor is reset.

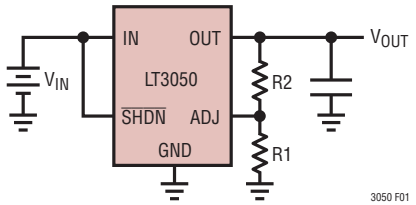
The LT3050 optimizes stability and transient response with low ESR, ceramic output capacitors. The regulator does not require the addition of ESR as is common with other regulators. The LT3050 typically provides 0.1% line regulation and 0.1% load regulation. Internal protection circuitry includes reverse-battery protection, reverse-output protection, reverse-current protection, current limit with fold-back and thermal shutdown.

This "bullet-proof" protection set makes it ideal for use in battery-powered, automotive and industrial systems.

In battery backup applications where the output is held up by a backup battery and the input is pulled to ground, the LT3050 acts like it has a diode in series with its output and prevents reverse current flow.

Adjustable Operation

The LT3050 has an output voltage range of 0.6V to 44.5V. The output voltage is set by the ratio of two external resistors, as shown in Figure 1. The device servos the output to maintain the ADJ pin voltage at 0.6V referenced to ground. The current in R1 is then equal to 0.6V/R1, and the current in R2 is the current in R1 minus the ADJ pin bias current.



$$V_{OUT} = 0.6V\left(1+\frac{R2}{R1}\right)-(I_{ADJ})\bullet R2$$

V_{ADJ} = 0.6V

I_{ADJ} = 16nA at 25°C

OUTPUT RANGE = 0.6V to 44.5V

Figure 1. Adjustable Operation

The ADJ pin bias current, 16nA at 25°C, flows from the ADJ pin through R1 to GND. Calculate the output voltage using the formula in Figure 1. The value of R1 should be no greater than 124k to provide a minimum 5μA load current so that output voltage errors, caused by the ADJ pin bias current, are minimized. Note that in shutdown, the output is turned off and the divider current is zero. Curves of ADJ Pin Voltage vs Temperature and ADJ Pin Bias Current vs Temperature appear in the Typical Performance Characteristics Section.

The LT3050 is tested and specified with the ADJ pin tied to the OUT pin, yielding V_{OUT} = 0.6V. Specifications for output voltages greater than 0.6V are proportional to the ratio of the desired output voltage to 0.6V: V_{OUT}/0.6V. For example, load regulation for an output current change of 1mA to 100mA is –0.2mV (typical) at V_{OUT} = 0.6V. at V_{OUT} = 12V, load regulation is:

$$\frac{12V}{0.6V}\bullet(-0.2mV) = -4mV$$

APPLICATIONS INFORMATION

Table 1 shows 1% resistor divider values for some common output voltages with a resistor divider current of 5µA.

Table 1. Output Voltage Resistor Divider Valves

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.2	118	118
1.5	121	182
1.8	124	249
2.5	115	365
3	124	499
3.3	124	562
5	115	845

Bypass Capacitance and Output Voltage Noise

The LT3050 regulator provides low output voltage noise over the 10Hz to 100kHz bandwidth while operating at full load with the addition of a bypass capacitor from the REF/BYP pin to GND. A good quality, low leakage capacitor is recommended. This capacitor bypasses the reference of the regulator, providing a low frequency noise pole for the internal reference. The noise pole provided by this bypass capacitor decreases the output voltage noise to as low as $30\mu V_{RMS}$ with the addition of a 10nF bypass capacitor when the output voltage is 0.6V. For higher output voltages (generated by using a resistor divider), the output voltage noise increases proportionately.

Higher values of output voltage noise are often measured if care is not exercised with regard to circuit layout and testing. Crosstalk from nearby traces induces unwanted noise onto the LT3050's output. Power supply ripple rejection must also be considered. The LT3050 regulator does not have unlimited power supply rejection and passes a small portion of the input noise through to the output.

During start-up, the internal reference will soft-start the reference if a bypass capacitor is present. Regulator start-up time is directly proportional to the size of the bypass capacitor, slowing to 5.5ms with a 10nF bypass capacitor and 2.2µF output capacitor.

Output Capacitance and Transient Response

The LT3050 regulator is stable with a wide range of output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. Use a minimum output capacitor of 2.2µF to prevent oscillations. The LT3050 is a micropower device and output load transient response is a function of output capacitance. Larger values of output capacitance decrease the peak deviations and provide improved transient response for larger load current changes. Bypass capacitors, used to decouple individual components powered by the LT3050, increase the effective output capacitor value. For applications with large load current transients, a low ESR ceramic capacitor in parallel with a bulk tantalum capacitor often provides an optimally damped response.

Give extra consideration to the use of ceramic capacitors. Manufacturers make ceramic capacitors with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics are specified with EIA temperature characteristic codes of Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics provide high C-V products in a small package at low cost, but exhibit strong voltage and temperature coefficients, as shown in Figures 2 and 3. When used with a 5V regulator, a 16V 10µF Y5V capacitor can exhibit an effective value as low as 1µF to 2µF for the DC bias voltage applied, and over the operating temperature range. The X5R and X7R dielectrics yield much more stable characteristics and are more suitable for use as the output capacitor.

The X7R type works over a wider temperature range and has better temperature stability, while the X5R is less expensive and is available in higher values. Care still must be exercised when using X5R and X7R capacitors; the X5R and X7R codes only specify operating temperature range and maximum capacitance change over temperature. Capacitance change due to DC bias with X5R and X7R capacitors is better than Y5V and Z5U capacitors, but can still be significant enough to drop capacitor values below appropriate levels. Capacitor DC bias characteristics tend to improve as component case size increases, but expected capacitance at operating voltage should be verified.

APPLICATIONS INFORMATION

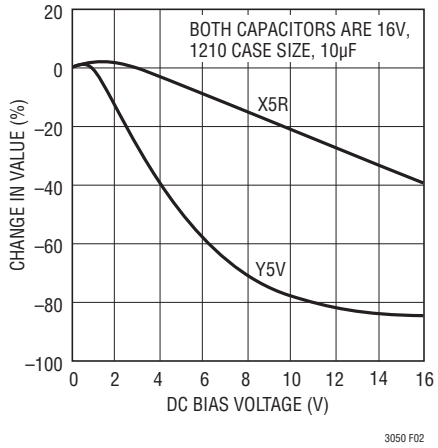


Figure 2. Ceramic Capacitor DC Bias Characteristics

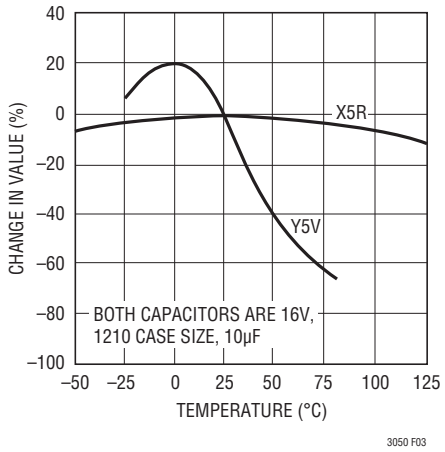


Figure 3. Ceramic Capacitor Temperature Characteristics

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to technical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor, the stress is induced by vibrations in the system or thermal transients. The resulting voltages produced cause appreciable amounts of noise. A ceramic capacitor produced the trace in Figure 4 in response to light tapping from a pencil. Similar vibration induced behavior can masquerade as increased output voltage noise.

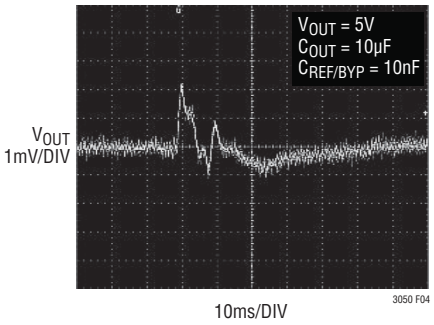


Figure 4. Noise Resulting from Tapping on a Ceramic Capacitor

Overload Recovery

Like many IC power regulators, the LT3050 has safe operating area protection. The safe area protection decreases current limit as input-to-output voltage increases, and keeps the power transistor inside a safe operating region for all values of input-to-output voltage. The LT3050 provides some output current at all values of input-to-output voltage up to the device breakdown.

When power is first applied, the input voltage rises and the output follows the input; allowing the regulator to start-up into very heavy loads. During start-up, as the input voltage is rising, the input-to-output voltage differential is small, allowing the regulator to supply large output currents. With a high input voltage, a problem can occur wherein the removal of an output short will not allow the output to recover. Other regulators, such as the LT1083/LT1084/LT1085 family and LT1764A also exhibit this phenomenon, so it is not unique to the LT3050. The problem occurs with a heavy output load when the input voltage is high and the output voltage is low. Common situations are: immediately after the removal of a short-circuit or if the shutdown pin is pulled high after the input voltage is already turned on. The load line for such a load intersects the output current curve at two points. If this happens, there are two stable output operating points for the regulator. With this double intersection, the input power supply needs to be cycled down to zero and brought up again to make the output recover.

APPLICATIONS INFORMATION

Thermal Considerations

The LT3050's maximum rated junction temperature of 125°C limits its power handling capability. Two components comprise the power dissipated by the device:

1. Output current multiplied by the input/output voltage differential: $I_{OUT} \bullet (V_{IN} – V_{OUT})$, and
2. GND pin current multiplied by the input voltage: $I_{GND} \bullet V_{IN}$

GND pin current is determined using the GND Pin Current curves in the Typical Performance Characteristics section. Power dissipation equals the sum of the two components listed above.

The LT3050 regulator has internal thermal limiting that protects the device during overload conditions. For continuous normal conditions, do not exceed the maximum junction temperature of 125°C. Carefully consider all sources of thermal resistance from junction-to-ambient including other heat sources mounted in proximity to the LT3050.

The undersides of the LT3050 DFN and MSOP packages have exposed metal from the lead frame to the die attachment. These packages allow heat to directly transfer from the die junction to the printed circuit board metal to control maximum operating junction temperature. The dual-in-line pin arrangement allows metal to extend beyond the ends of the package on the topside (component side) of a PCB. Connect this metal to GND on the PCB. The multiple IN and OUT pins of the LT3050 also assist in spreading heat to the PCB.

For surface mount devices, heat sinking is accomplished by using the heat spreading capabilities of the PC board and its copper traces. Copper board stiffeners and plated through-holes also can spread the heat generated by power devices. The following tables list thermal resistance as a function of copper area in a fixed board size. All measurements were taken in still air on a four-layer FR-4 board with one ounce solid internal planes and two ounce external trace planes with a total board thickness of 1.6mm. For further information on thermal resistance and using thermal information, refer to JEDEC standard JESD51, notably JESD51-12.

Table 1. MSOP Measured Thermal Resistance

COPPER AREA			
TOPSIDE	BACKSIDE	BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
2500 sq mm	2500 sq mm	2500 sq mm	40°C/W
1000 sq mm	2500 sq mm	2500 sq mm	41°C/W
225 sq mm	2500 sq mm	2500 sq mm	43°C/W
100 sq mm	2500 sq mm	2500 sq mm	45°C/W

Table 2. DFN Measured Thermal Resistance

COPPER AREA TOPSIDE	BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
2500 sq mm	2500 sq mm	44°C/W
1000 sq mm	2500 sq mm	45°C/W
225 sq mm	2500 sq mm	47°C/W
100 sq mm	2500 sq mm	49°C/W

Calculating Junction Temperature

Example: Given an output voltage of 5V, an input voltage range of 12V ±5%, a maximum output current range of 75mA and a maximum ambient temperature of 85°C, what will the maximum junction temperature be?

The power dissipated by the device equals:

$$I_{OUT(MAX)} * (V_{IN(MAX)} – V_{OUT}) + I_{GND} * V_{IN(MAX)}$$

where,

$I_{OUT(MAX)} = 75mA$

$V_{IN(MAX)} = 12.6V$

I_{GND} at ($I_{OUT} = 75mA$, $V_{IN} = 12V$) = 1.5mA

So,

$P = 75mA \bullet (12.6V - 5V) + 1.5mA \bullet 12.6V = 0.589W$

Using a DFN package, the thermal resistance ranges from 44°C/W to 49°C/W depending on the copper area. So the junction temperature rise above ambient approximately equals:

$0.589W \bullet 49°C/W = 28.86°C$

The maximum junction temperature equals the maximum ambient temperature plus the maximum junction temperature rise above ambient or:

$T_{JMAX} = 85°C + 28.86°C = 113.86°C$

APPLICATIONS INFORMATION

Protection Features

The LT3050 incorporates several protection features that make it ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the device also protects against reverse-input voltages, reverse-output voltages and reverse output-to-input voltages.

Current limit protection and thermal overload protection protect the device against current overload conditions at the output of the device. For normal operation, do not exceed a junction temperature of 125°C.

The LT3050 IN pin withstands reverse voltages of 50V. The device limits current flow to less than 300µA (typically less than 10µA) and no negative voltage appears at OUT. The device protects both itself and the load against batteries that are plugged in backwards.

The $\overline{SHDN}$ pin cannot be driven below GND unless tied to the IN pin. If the $\overline{SHDN}$ pin is driven below GND while IN is powered, the output may turn on. $\overline{SHDN}$ pin logic cannot be referenced to a negative rail.

The LT3050 incurs no damage if its output is pulled below ground. If the input is left open-circuit or grounded, the output can be pulled below ground by 50V. No current flows through the pass transistor from the output. However, current flows in (but is limited by) the resistor divider that sets the output voltage. Current flows from the bottom resistor in the divider and from the ADJ pin's internal clamp through the top resistor in the divider to the external circuitry pulling OUT below ground. If the input is powered by a voltage source, the output sources current equal to its current limit capability and the LT3050 protects itself by thermal limiting. In this case, grounding the $\overline{SHDN}$ pin turns off the device and stops the output from sourcing current.

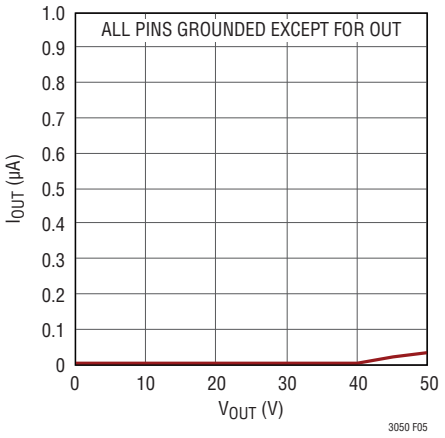
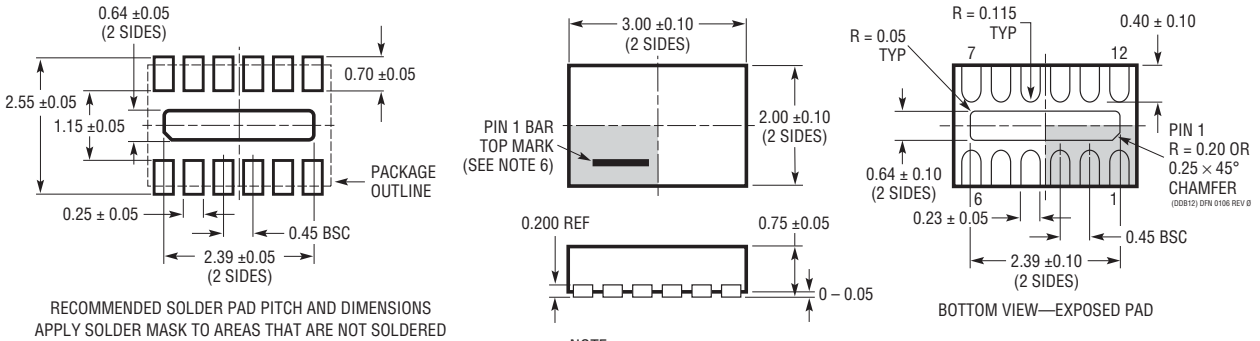


Figure 5. Reverse Output Current

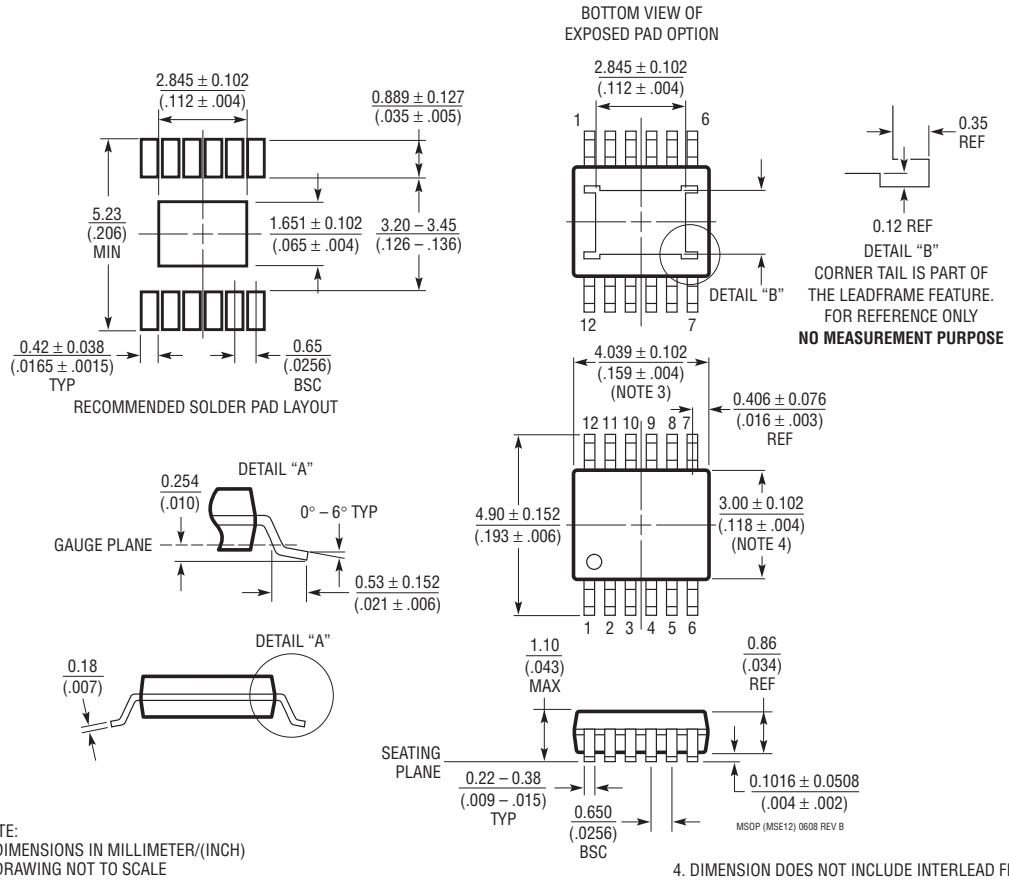
PACKAGE DESCRIPTION

DDB Package
12-Lead Plastic DFN (3mm × 2mm)
(Reference LTC DWG # 05-08-1723 Rev Ø)



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAG

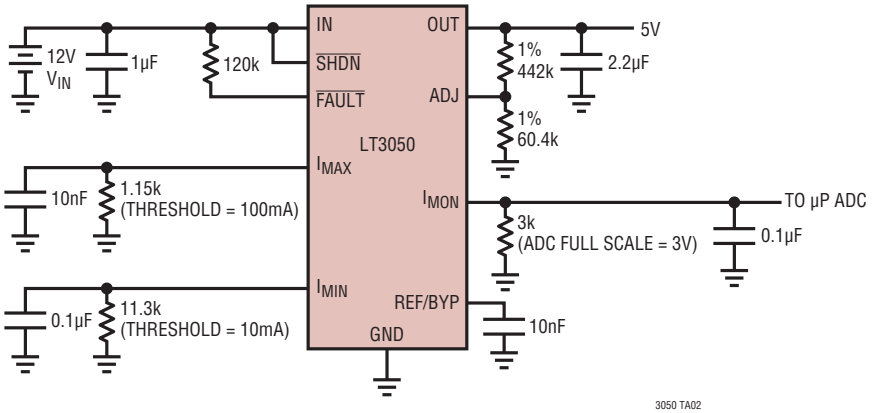
MSE Package
12-Lead Plastic MSOP Exposed Die Pad
(Reference LTC DWG # 05-08-1666 Rev B)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

TYPICAL APPLICATION

5V Protected Antenna Supply with 100mA Current Limit, 10mA I_{MIN}



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1761	100mA, Low Noise LDO	300mV Dropout Voltage, Low Noise: 20µV_{RMS}, V_{IN} = 1.8V to 20V, ThinSOT Package
LT1762	150mA, Low Noise LDO	300mV Dropout Voltage, Low Noise: 20µV_{RMS}, V_{IN} = 1.8V to 20V, MS8 Package
LT1763	500mA, Low Noise LDO	300mV Dropout Voltage, Low Noise: 20µV_{RMS}, V_{IN} = 1.8V to 20V, SO-8 Package
LT1962	300mA, Low Noise LDO	270mV Dropout Voltage, Low Noise: 20µV_{RMS}, V_{IN} = 1.8V to 20V, MS8 Package
LT1963/A	1.5A Low Noise, Fast Transient Response LDO	340mV Dropout Voltage, Low Noise: 40µV_{RMS}, V_{IN} = 2.5V to 20V, "A" Version Stable with Ceramic Capacitors, TO-220, DD-PAK, SOT-223 and SO-8 Packages
LT1965	1.1A, Low Noise, Low Dropout Linear Regulator	290mV Dropout Voltage, Low Noise: 40µV_{RMS}, V_{IN}: 1.8V to 20V, V_{OUT}: 1.2V to 19.5V, Stable with Ceramic Capacitors, TO-220, DD-PAK, MSOP and 3 × 3 DFN Packages
LT3008	20mA, 45V, 3uA I_Q Micropower LDO	300mV Dropout Voltage, Low I_Q: 3µA, V_{IN} = 2.0V to 45V, V_{OUT} = 0.6V to 39.5V; ThinSOT and 2mm × 2mm DFN-6 Packages
LT3009	20mA, 3uA I_Q Micropower LDO	280mV Dropout Voltage, Low I_Q: 3µA, V_{IN} = 1.6V to 20V, ThinSOT and SC-70 Packages
LT3010	50mA, High Voltage, Micropower LDO	V_{IN}: 3V to 80V, V_{OUT}: 1.275V to 60V, VDO = 0.3V, I_Q = 30µA, ISD < 1µA, Low Noise: <100µV_{RMS}, Stable with 1µF Output Capacitor, Exposed MS8 Package
LT3011	50mA, High Voltage, Micropower LDO with PWRGD	V_{IN}: 3V to 80V, V_{OUT}: 1.275V to 60V, VDO = 0.3V, I_Q = 46µA, ISD < 1µA, Low Noise: <100µV_{RMS}, Power Good, Stable with 1µF Output Capacitor, 3 × 3 DFN-10 and Exposed MS12E Packages
LT3012	250mA, 4V to 80V, Low Dropout Micropower Linear Regulator	V_{IN}: 4V to 80V, V_{OUT}: 1.24V to 60V, VDO = 0.4V, I_Q = 40µA, ISD < 1µA, TSSOP-16E and 4mm × 3mm DFN-12 Packages
LT3013	250mA, 4V to 80V, Low Dropout Micropower Linear Regulator with PWRGD	V_{IN}: 4V to 80V, V_{OUT}: 1.24V to 60V, VDO = 0.4V, I_Q = 65µA, ISD < 1µA, Power Good feature; TSSOP-16E and 4mm × 3mm DFN-12 Packages
LT3014/HV	20mA, 3V to 80V, Low Dropout Micropower Linear Regulator	V_{IN}: 3V to 80V (100V for 2ms, "HV" version), V_{OUT}: 1.22V to 60V, VDO = 0.35V, I_Q = 7µA, ISD < 1µA, ThinSOT and 3mm × 3mm DFN-8 Packages
LT3060	100mA, Low Noise LDO with Soft Start	300mV Dropout Voltage, Low Noise: 20µV_{RMS}, V_{IN} = 1.8V to 45V, DFN Package
LT3080/-1	1.1A, Parallelable, Low Noise, Low Dropout Linear Regulator	300mV Dropout Voltage (2-supply operation), Low Noise: 40µV_{RMS}, V_{IN}: 1.2V to 36V, V_{OUT}: 0V to 35.7V, Current-Based Reference with 1-Resistor V_{OUT} set; Directly Parallelable (no op amp required), Stable with Ceramic Caps, TO-220, SOT-223, MSOP and 3mm × 3mm DFN Packages; "–1" Version has Integrated Internal Ballast Resistor
LT3085	500mA, Parallelable. Low Noise, Low Dropout Linear Regulator	275mV Dropout Voltage (2-supply operation), Low Noise: 40µV_{RMS}, V_{IN}: 1.2V to 36V, V_{OUT}: 0V to 35.7V, Current-Based Reference with 1-Resistor V_{OUT} set; Directly Parallelable (no op amp required), Stable with Ceramic Caps, MSOP-8 and 2mm × 3mm DFN Packages

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