

M48Z02 M48Z12

16 Kbit (2Kb x 8) ZEROPOWER[®] SRAM

- INTEGRATED ULTRA LOW POWER SRAM, POWER-FAIL CONTROL CIRCUIT and BATTERY
- UNLIMITED WRITE CYCLES
- READ CYCLE TIME EQUALS WRITE CYCLE TIME
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- WRITE PROTECT VOLTAGES (V_{PFD} = Power-fail Deselect Voltage):
 - M48Z02: 4.50V \leq V_{PFD} \leq 4.75V
 - M48Z12: 4.20V \leq V_{PFD} \leq 4.50V
- SELF-CONTAINED BATTERY in the CAPHAT DIP PACKAGE
- PIN and FUNCTION COMPATIBLE with JEDEC STANDARD 2K x 8 SRAMs

DESCRIPTION

Table 1. Signal Names

The M48Z02/12 ZEROPOWER[®] RAM is a 2K x 8 non-volatile static RAM which is pin and functional compatible with the DS1220.

A special 24 pin 600mil DIP CAPHAT[™] package houses the M48Z02/12 silicon with a long life lithium button cell to form a highly integrated battery backed-up memory solution.

The M48Z02/12 button cell has sufficient capacity and storage life to maintain data and clock functionality for an accumulated time period of at least 10 years in the absence of power over the operating temperature range.

A0-A10	Address Inputs		
DQ0-DQ7	Data Inputs / Outputs		
Ē	Chip Enable		
G	Output Enable		
W	Write Enable		
V _{CC}	Supply Voltage		
V _{SS}	Ground		

May 1999

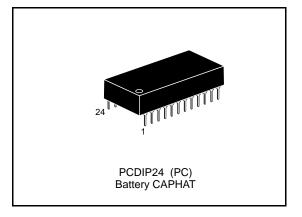
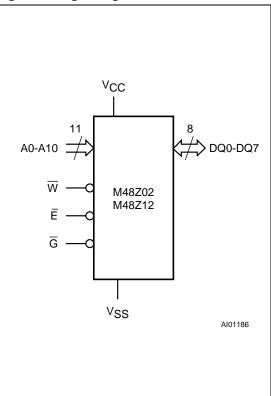


Figure 1. Logic Diagram



Symbol	Parameter	Value	Unit
T _A	Ambient Operating Temperature	-40 to 85	°C
T _{STG}	Storage Temperature (V _{CC} Off)	-40 to 85	°C
T _{SLD} ⁽²⁾	Lead Solder Temperature for 10 seconds	260	°C
V _{IO}	Input or Output Voltages	–0.3 to 7	V
V _{CC}	Supply Voltage	–0.3 to 7	V
lo	Output Current	20	mA
PD	Power Dissipation	1	W

 Table 2. Absolute Maximum Ratings ⁽¹⁾

Notes: 1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum rating conditions for extended periods of time may affect reliability.

2. Soldering temperature not to exceed 260°C for 10 seconds (total thermal budget not to exceed 150°C for longer than 30 seconds). CAUTION: Negative undershoots below –0.3 volts are not allowed on any pin while in the Battery Back-up mode.

Mode	Vcc	E	G	W	DQ0-DQ7	Power
Deselect		VIH	Х	Х	High Z	Standby
Write	4.75V to 5.5V or	VIL	Х	VIL	D _{IN}	Active
Read	4.5V to 5.5V	V _{IL}	V _{IL}	VIH	D _{OUT}	Active
Read		VIL	VIH	VIH	High Z	Active
Deselect	V _{SO} to V _{PFD} (min)	Х	Х	Х	High Z	CMOS Standby
Deselect	$\leq V_{SO}$	Х	Х	Х	High Z	Battery Back-up Mode

Table 3. Operating Modes

Notes: $X = V_{IH}$ or V_{IL} ; V_{SO} = Battery Back-up Switchover Voltage.

Figure 2. DIP Pin Connections

A7 [] 1 A6 [] 2 A5 [] 3 A4 [] 4		24] V _{CC} 23] A8 22] A9 21] W
A3 [5	M49700	20]G
A2 [] 6 A1 [] 7	M48Z02 M48Z12	19] A10 18] Ē
A0 🛛 8		17] DQ7
DQ0 [9		16 🛛 DQ6
DQ1 🛛 10		15] DQ5
DQ2 [11		14 🛛 DQ4
V _{SS} [12		13] DQ3
	A	101187

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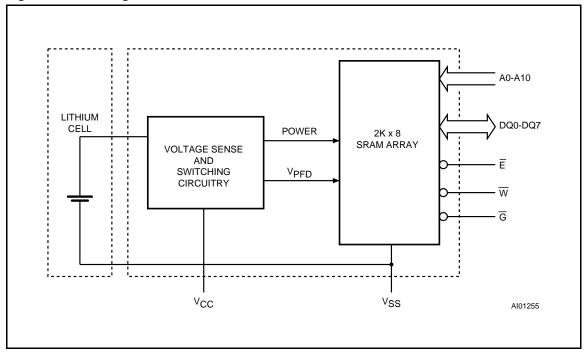
DESCRIPTION (cont'd)

The M48Z02/12 is a non-volatile pin and function equivalent to any JEDEC standard 2K x 8 SRAM. It also easily fits into many ROM, EPROM, and EEPROM sockets, providing the non-volatility of PROMs without any requirement for special write timing or limitations on the number of writes that can be performed.

The M48Z02/12 also has its own Power-fail Detect circuit. The control circuitry constantly monitors the single 5V supply for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the SRAM, providing a high degree of data security in the midst of unpredictable system operation brought on by low V_{CC} . As V_{CC} falls below approximately 3V, the control circuitry connects the battery which maintains data and clock operation until valid power returns.

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Figure 3. Block Diagram



READ MODE

The M48Z02/12 is in the Read Mode whenever \overline{W} (Write Enable) is high and \overline{E} (Chip Enable) is low. The device architecture allows ripple-through access of data from eight of 16,384 locations in the static storage array. Thus, the unique address specified by the 11 Address Inputs defines which one of the 2,048 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within Address Access time (t_{AVQV}) after the last address input signal is stable, providing that the \overline{E} and \overline{G} access times are also satisfied. If the \overline{E} and \overline{G} access times are not met, valid data will be available after the latter of the Chip Enable Access time (t_{ELQV}) or Output Enable Access time (t_{GLQV}).

The state of the eight three-state Data I/O signals is controlled by \overline{E} and \overline{G} . If the outputs are activated before t_{AVQV} , the data lines will be driven to an indeterminate state until t_{AVQV} . If the Address Inputs are changed while \overline{E} and \overline{G} remain active, output data will remain valid for Output Data Hold time (t_{AXQX}) but will go indeterminate until the next Address Access.

Table 4. AC Measurement Conditions

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0V to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 4. AC Testing Load Circuit

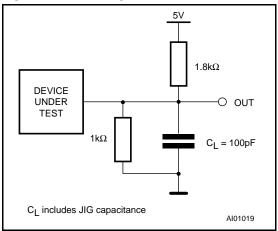


Table 5. Capacitance ⁽¹⁾

(T_A = 25 °C)

Symbol	Parameter	Test Condition	Min	Max	Unit
C _{IN}	Input Capacitance	$V_{IN} = 0V$		10	pF
C _{IO} ⁽²⁾	Input / Output Capacitance	$V_{OUT} = 0V$		10	pF

Notes: 1. Effective capacitance measured with power supply at 5V. 2. Outputs deselected

Table 6. DC Characteristics

(T_A = 0 to 70°C or -40 to 85°C; V_{CC} = 4.75V to 5.5V or 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Мах	Unit
I _{LI} ⁽¹⁾	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$		±1	μA
I _{LO} ⁽¹⁾	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$		±5	μA
Icc	Supply Current	Outputs open		80	mA
I _{CC1}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		3	mA
I _{CC2}	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} - 0.2V$		3	mA
VIL ⁽²⁾	Input Low Voltage		-0.3	0.8	V
VIH	Input High Voltage		2.2	V _{CC} + 0.3	V
V _{OL}	Output Low Voltage	I _{OL} = 2.1mA		0.4	V
V _{OH}	Output High Voltage	$I_{OH} = -1mA$	2.4		V

Notes: 1. Outputs Deselected. 2. Negative spikes of –1V allowed for up to 10ns once per cycle.

Table 7. Power Down/Up Trip Points DC Characteristics ⁽¹⁾ (T_A = 0 to 70°C or -40 to 85°C)

Symbol	Parameter	Min	Тур	Max	Unit
Vpfd	Power-fail Deselect Voltage (M48Z02)	4.5	4.6	4.75	V
V _{PFD}	Power-fail Deselect Voltage (M48Z12)	4.2	4.3	4.5	V
V _{SO}	Battery Back-up Switchover Voltage		3.0		V
t _{DR}	Expected Data Retention Time	10			YEARS

Note: 1. All voltages referenced to V_{SS}.

Table 8. Power Down/Up Mode AC Characteristics

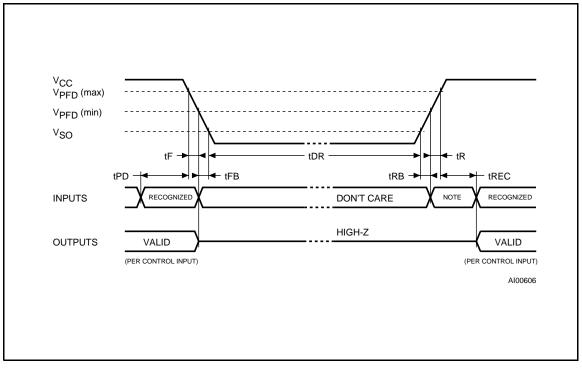
$(T_A = 0 \text{ to } 70^\circ \text{C})$	or –40 to 85°C)
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Symbol	Parameter	Min	Мах	Unit
t _{PD}	\overline{E} or \overline{W} at V_{IH} before Power Down	0		μs
t_{F} ⁽¹⁾	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		μs
t_{FB} ⁽²⁾	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		μs
t _R	V _{PFD} (min) to V _{PFD} (max) V _{CC} Rise Time	0		μs
t _{RB}	V_{SO} to V_{PFD} (min) V_{CC} Rise Time	1		μs
t _{REC}	\overline{E} or \overline{W} at V _{IH} after Power Up	2		ms

Notes: 1. VPFD (max) to VPFD (min) fall time of less than tF may result in deselection/write protection not occurring until 50 µs after

V Cc passes V Fr D (min). 2. V PFD (min) to V So fall time of less than tFB may cause corruption of RAM data.





Note: Inputs may or may not be recognized at this time. Caution should be taken to keep \overline{E} high as V_{CC} rises past V_{PFD}(min). Some systems may perform inadvertent write cycles after V_{CC} rises above V_{PFD}(min) but before normal system operations begin. Even though a power on reset is being applied to the processor, a reset condition may not occur until after the system clock is running.

Table 9. Read Mode AC Characteristics

 $(T_A = 0 \text{ to } 70^{\circ}\text{C or } -40 \text{ to } 85^{\circ}\text{C}; V_{CC} = 4.75\text{V to } 5.5\text{V or } 4.5\text{V to } 5.5\text{V})$

		M48Z02 / M48Z12						
Symbol	Parameter	-7	70	-1	50	-2	00	Unit
		Min	Мах	Min	Max	Min	Мах	
t _{AVAV}	Read Cycle Time	70		150		200		ns
t _{AVQV}	Address Valid to Output Valid		70		150		200	ns
t _{ELQV}	Chip Enable Low to Output Valid		70		150		200	ns
t _{GLQV}	Output Enable Low to Output Valid		35		75		80	ns
t _{ELQX}	Chip Enable Low to Output Transition	5		10		10		ns
t _{GLQX}	Output Enable Low to Output Transition	5		5		5		ns
t _{EHQZ}	Chip Enable High to Output Hi-Z		25		35		40	ns
t _{GHQZ}	Output Enable High to Output Hi-Z		25		35		40	ns
t _{AXQX}	Address Transition to Output Transition	10		5		5		ns

Figure 6. Read Mode AC Waveforms

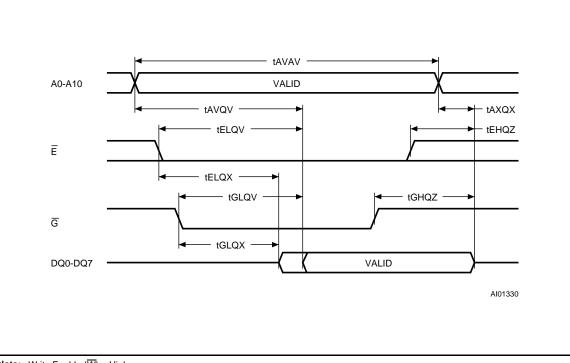






Table 10. Write Mode AC Characteristics

 $(T_A = 0 \text{ to } 70^{\circ}\text{C} \text{ or } -40 \text{ to } 85^{\circ}\text{C}; V_{CC} = 4.75\text{V to } 5.5\text{V or } 4.5\text{V to } 5.5\text{V})$

	Parameter	M48Z02 / M48Z12						
Symbol		-7	-70		50	-200		Unit
		Min	Max	Min	Max	Min	Max	
t _{AVAV}	Write Cycle Time	70		150		200		ns
t _{AVWL}	Address Valid to Write Enable Low	0		0		0		ns
t _{AVEL}	Address Valid to Chip Enable Low	0		0		0		ns
twLWH	Write Enable Pulse Width	50		90		120		ns
t _{ELEH}	Chip Enable Low to Chip Enable High	55		90		120		ns
t _{WHAX}	Write Enable High to Address Transition	0		10		10		ns
t _{EHAX}	Chip Enable High to Address Transition	0		10		10		ns
t _{DVWH}	Input Valid to Write Enable High	30		40		60		ns
t _{DVEH}	Input Valid to Chip Enable High	30		40		60		ns
t _{WHDX}	Write Enable High to Input Transition	5		5		5		ns
t _{EHDX}	Chip Enable High to Input Transition	5		5		5		ns
t _{WLQZ}	Write Enable Low to Output Hi-Z		25		50		60	ns
t _{AVWH}	Address Valid to Write Enable High	60		120		140		ns
t _{AVEH}	Address Valid to Chip Enable High	60		120		140		ns
t _{WHQX}	Write Enable High to Output Transition	5		10		10		ns

WRITE MODE

The M48Z02/12 is in the Write Mode whenever \overline{W} and \overline{E} are active. The start of a write is referenced from the latter occurring falling edge of \overline{W} or \overline{E} . A write is terminated by the earlier rising edge of \overline{W} or \overline{E} . The addresses must be held valid throughout the cycle. \overline{E} or \overline{W} must return high for a minimum

of t_{EHAX} from Chip Enable or t_{WHAX} from Write Enable prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} afterward. G should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on E and G, a low on W will disable the outputs t_{WLQZ} after W falls.

M48Z02, M48Z12

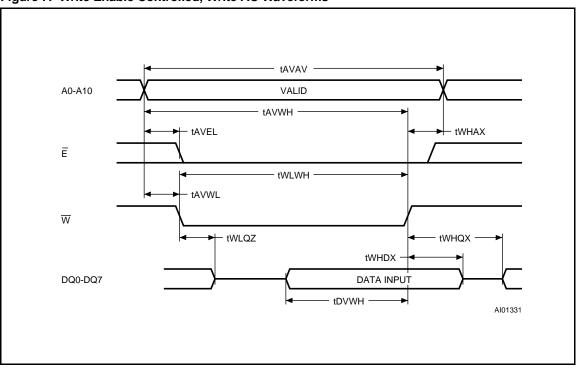
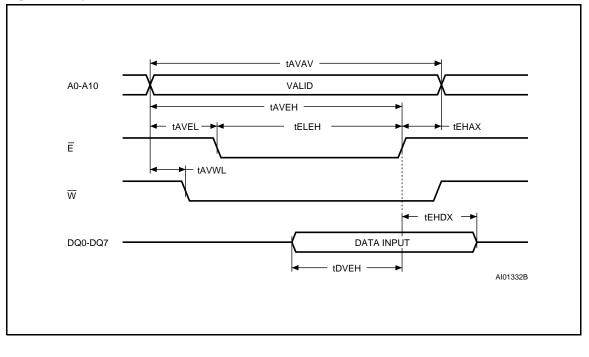


Figure 7. Write Enable Controlled, Write AC Waveforms





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DATA RETENTION MODE

With valid V_{CC} applied, the M48Z02/12 operates as a conventional BYTEWIDE[™] static RAM. Should the supply voltage decay, the RAM will automatically power-fail deselect, write protecting itself when V_{CC} falls within the V_{PFD}(max), V_{PFD}(min) window. All outputs become high impedance, and all inputs are treated as "don't care."

Note: A power failure during a write cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the RAM's content. At voltages below $V_{PFD}(min)$, the user can be assured the memory will be in a write protected state, provided the V_{CC} fall time is not less than tF. The M48Z02/12 may respond to transient noise spikes on V_{CC} that reach into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

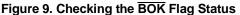
The power switching circuit connects external V_{CC} to the RAM and disconnects the battery when V_{CC} rises above V_{SO}. As V_{CC} rises, the battery voltage is checked. If the voltage is too low, an internal Battery Not OK (BOK) flag will be set. The BOK flag can be checked after power up. If the BOK flag is set, the first write attempted will be blocked. The flag is automatically cleared after the first write, and normal RAM operation resumes. Figure 9 illustrates how a BOK check routine could be structured.

POWER SUPPLY DECOUPLING and UNDER-SHOOT PROTECTION

Icc transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the Vcc bus. These transients can be reduced if capacitors are used to store energy, which stabilizes the Vcc bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of $0.1\mu F$ (as shown in Figure 10) is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on V_{CC} that drive it to values below V_{SS} by as much as one Volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, it is recommeded to connect a schottky diode from V_{CC} to V_{SS} (cathode connected to V_{CC} , anode to V_{SS}). Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface mount.

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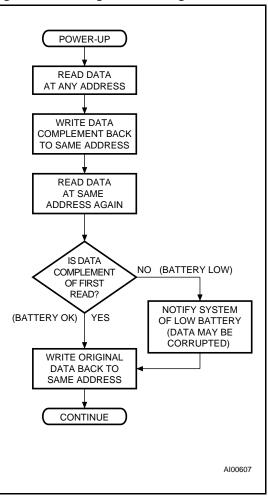
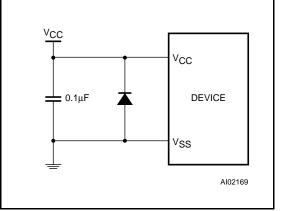


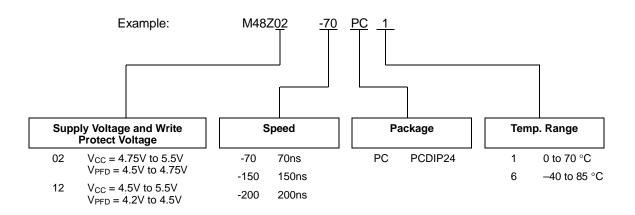
Figure 10. Supply Voltage Protection



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ORDERING INFORMATION SCHEME

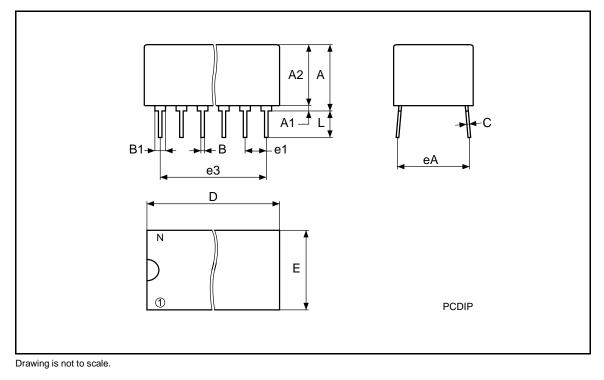


For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

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Symb	mm			inches		
	Тур	Min	Max	Тур	Min	Мах
А		8.89	9.65		0.350	0.380
A1		0.38	0.76		0.015	0.030
A2		8.38	8.89		0.330	0.350
В		0.38	0.53		0.015	0.021
B1		1.14	1.78		0.045	0.070
С		0.20	0.31		0.008	0.012
D		34.29	34.80		1.350	1.370
E		17.83	18.34		0.702	0.722
e1		2.29	2.79		0.090	0.110
e3		25.15	30.73		0.990	1.210
eA		15.24	16.00		0.600	0.630
L		3.05	3.81		0.120	0.150





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