17 CHANNEL ESD PROTECTION ARRAY

Features

- 17-channel ESD protection
- 8kV contact discharge ESD protection per IEC 61000-4-2
- 15kV ESD protection (HBM)
- Low loading capacitance, 5.5pF typ.
- 20-pin SOIC or QSOP package

Applications

- Parallel printer port protection
- ESD protection for sensitive electronic equipment
- Drop-in replacement for PDN 002

Product Description

The PAC DN002™ is a diode array designed to provide 17 channels of ESD protection for electronic components or sub-systems. Each channel consists of a pair of diodes which steers the ESD current pulse either to the positive (V_P) or negative (V_N) supply. The PAC DN002 will protect against ESD pulses up to 15KV Human Body Model.

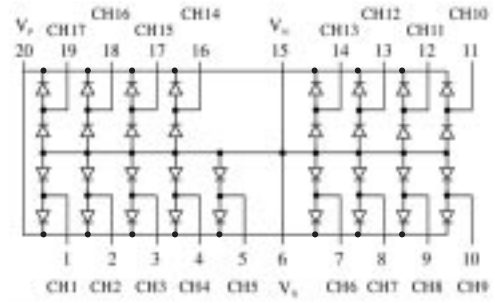
This device is particularly well-suited to provide additional ESD protection for parallel printer ports. It exhibits low loading capacitance for all signal lines.

ABSOLUTE MAXIMUM RATINGS

Diode Forward DC Current (Note 1)	20mA
Storage Temperature	-65°C to 150°C
Operating Temperature Range	-20°C to 85°C
DC Voltage at any Channel Input	V_N-0.5V to V_P+0.5V

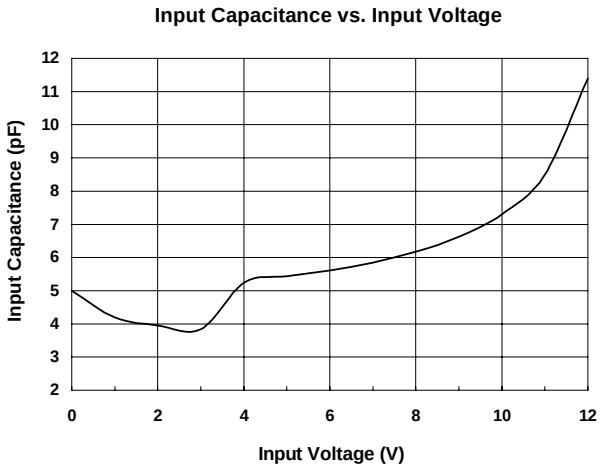
Note 1: Only one diode conducting at a time.

SCHEMATIC CONFIGURATION



STANDARD SPECIFICATIONS			
Parameter	Min.	Typ.	Max.
Operating Supply Voltage (V_P - V_N)			12.0V
Supply Current (V_P - V_N) = 12.0V, T = 25°C			10 µA
Diode Forward Voltage, I_F = 20mA, T = 25°C	0.65 V		1.0 V
ESD Protection Voltage at any Channel Input Human Body Model, Method 3015 (See Note 2, 3) Contact Discharge per IEC 1000-4-2 (See Note 4)	 ±15KV ±8KV		
Channel Clamp Voltage under ESD test conditions specified above, T = 25°C (Notes 2,3,4) Positive transients Negative transients			 V_P + 13.0 V V_N - 13.0 V
Channel Leakage Current, T = 25°C		±0.1 µA	±1.0 µA
Channel Input Capacitance (Measured @ 1 MHz) V_P = 12V, V_N = 0V, V_{IN} = 6V (See Note 4)		5.5pF	12pF
Package Power Rating			1.00W

Note 2: From I/O pins to V_P or V_N only. V_P bypassed to V_N with 0.2 µF ceramic capacitor.
Note 3: Human Body Model per MIL-STD-883, Method 3015, $C_{Discharge}$=100pF, $R_{Discharge}$=1.5KΩ, V_P=12V, V_N=GND.
Note 4: This parameter is guaranteed by characterization.



Typical variation of C_{IN} with V_{IN}
(V_P = 12V, V_N = 0V, 0.1µF chip capacitor between V_P & V_N)

STANDARD PART ORDERING INFORMATION		
Package		Ordering Part Number
Pins	Style	Part Marking
20	SOIC	PACDN002S
20	QSOP	PACDN002Q

When placing an order please specify desired shipping: Tubes or Tape & Reel.

Application Information

See also California Micro Devices Application note AP209, "Design Considerations for ESD protection."

In order to realize the maximum protection against ESD pulses, care must be taken in the PCB layout to minimize parasitic series inductances to the Supply and Ground rails. Refer to Figure 1, which illustrates the case of a positive ESD pulse applied between an input channel and Chassis Ground. The parasitic series inductance back to the power supply is represented by L_1. The voltage V_Z on the line being protected is:

$$V_Z = \text{Forward voltage drop of } D_1 + L_1 \times d(I_{esd})/dt + V_{Supply}$$

where I_{esd} is the ESD current pulse, and V_{Supply} is the positive supply voltage.

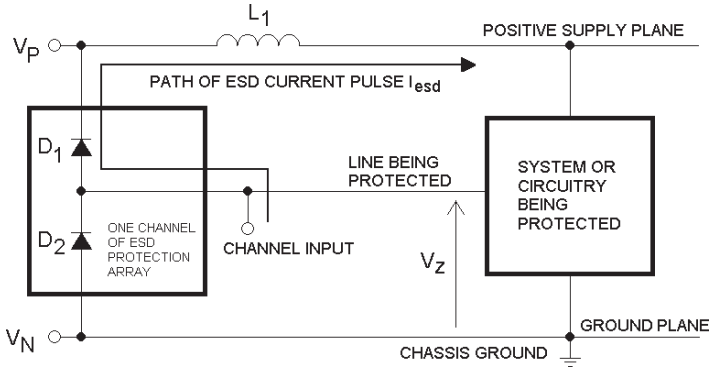


Figure 1

An ESD current pulse can rise from zero to its peak value in a very short time. As an example, a level 4 contact discharge per the IEC 61000-4-2 standard results in a current pulse that rises from zero to 30 Amps in 1nS. Here $d(I_{esd})/dt$ can be approximated by $\Delta I_{esd}/\Delta t$, or $30/(1 \times 10^{-9})$. So just 10nH of series inductance (L_1) will lead to a 300V increment in V_Z!

Similarly for negative ESD pulses, parasitic series inductance from the V_N pin to the ground rail will lead to drastically increased negative voltage on the line being protected.

Another consideration is the output impedance of the power supply for fast transient currents. Most power supplies exhibit a much higher output impedance to fast transient current spikes. In the V_Z equation above, the V_{Supply} term, in reality, is given by $(V_{DC} + I_{esd} \times R_{out})$, where V_{DC} and R_{out} are the nominal supply DC output voltage and effective output impedance of the power supply respectively. As an example, a R_{out} of 1 ohm would result in a 10V increment in V_Z for a peak I_{esd} of 10A.

To mitigate these effects, a high frequency bypass capacitor should be connected between the V_P pin of the ESD Protection Array and the ground plane. The value of this bypass capacitor should be chosen such that it will absorb the charge transferred by the ESD pulse with minimal change in V_P. Typically a value in the 0.1 μF to 0.2 μF range is adequate for IEC-61000-4-2 level 4 contact discharge protection (8KV). For higher ESD voltages, the bypass capacitor should be increased accordingly. Ceramic chip capacitors mounted with short printed circuit board traces are good choices for this application. Electrolytic capacitors should be avoided as they have poor high frequency characteristics. For extra protection, connect a zener diode in parallel with the bypass capacitor to mitigate the effects of the parasitic series inductance inherent in the capacitor. The breakdown voltage of the zener diode should be slightly higher than the maximum supply voltage.

As a general rule, the ESD Protection Array should be located as close as possible to the point of entry of expected electrostatic discharges. The power supply bypass capacitor mentioned above should be as close to the V_P pin of the Protection Array as possible, with minimum PCB trace lengths to the power supply and ground planes to minimize stray series inductance.