

**2.0A, 60V, 0.150 Ohm, N-Channel, Logic Level, ESD Rated, Power MOSFET**

This product is an N-Channel power MOSFET manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI circuits, gives optimum utilization of silicon, resulting in outstanding performance. It was designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

Formerly developmental type TA49158.

**Ordering Information**

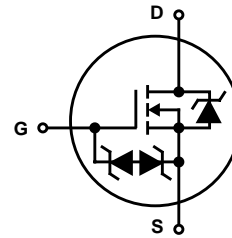
PART NUMBER	PACKAGE	BRAND
RFT3055LE	SOT-223	3055L

NOTE: RFT3055LE is available only in tape and reel.

**Features**

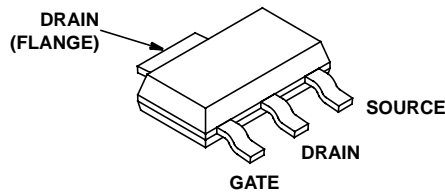
- 2.0A, 60V
- $r_{DS(ON)} = 0.150\Omega$
- 2kV ESD Protected
- Temperature Compensating PSPICE® Model
- Thermal Impedance SPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"

**Symbol**



**Packaging**

SOT-223



# RFT3055LE

## Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ , Unless Otherwise Specified

	RFT3055LE	UNITS
Drain to Source Voltage (Note 1) . . . . .	$V_{DSS}$	60 V
Drain to Gate Voltage ( $R_{GS} = 20k\Omega$ ) (Note 1) . . . . .	$V_{DGR}$	60 V
Gate to Source Voltage . . . . .	$V_{GS}$	$\pm 10$ V
Drain Current		
Continuous (Figure 2) (Note 2) . . . . .	$I_D$	2.0 A
Pulsed Drain Current . . . . .	$I_{DM}$	Figure 5
Pulsed Avalanche Rating . . . . .	$E_{AS}$	Figures 6, 16, 17
Power Dissipation (Note 2) . . . . .	$P_D$	1.1 W
Derate Above $25^\circ\text{C}$ . . . . .		9.09 $\text{mW}/^\circ\text{C}$
Operating and Storage Temperature . . . . .	$T_J, T_{STG}$	$-55$ to $150$ $^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s . . . . .	$T_L$	300 $^\circ\text{C}$
Package Body for 10s, See Techbrief 334 . . . . .	$T_{pkg}$	260 $^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

- $T_J = 25^\circ\text{C}$  to  $125^\circ\text{C}$ .

## Electrical Specifications $T_A = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	$BV_{DSS}$	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$ (Figure 11)	60	-	-	V
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$ (Figure 10)	1	-	2	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 60\text{V}, V_{GS} = 0\text{V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 60\text{V}, V_{GS} = 0\text{V}, T_A = 150^\circ\text{C}$	-	-	50	$\mu\text{A}$
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 10\text{V}$	-	-	10	$\mu\text{A}$
Drain to Source On Resistance	$r_{DS(ON)}$	$I_D = 2.0\text{A}, V_{GS} = 5\text{V}$ (Figure 9)	-	0.110	0.150	$\Omega$
Turn-On Time	$t_{ON}$	$V_{DD} = 30\text{V}, I_D \cong 2.0\text{A},$ $R_L = 15\Omega, V_{GS} = 5\text{V},$ $R_{GS} = 5\Omega$ (Figure 12)	-	-	120	ns
Turn-On Delay Time	$t_{d(ON)}$		-	10	-	ns
Rise Time	$t_r$		-	70	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	30	-	ns
Fall Time	$t_f$		-	25	-	ns
Turn-Off Time	$t_{OFF}$		-	-	85	ns
Total Gate Charge	$Q_{g(TOT)}$	$V_{GS} = 0\text{V}$ to $10\text{V}$	-	28	35	nC
Gate Charge at 10V	$Q_{g(5)}$	$V_{GS} = 0\text{V}$ to $5\text{V}$				
Threshold Gate Charge	$Q_{g(TH)}$	$V_{GS} = 0\text{V}$ to $1\text{V}$				
Input Capacitance	$C_{ISS}$	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V},$ $f = 1\text{MHz}$ (Figure 12)	-	850	-	pF
Output Capacitance	$C_{OSS}$		-	170	-	pF
Reverse Transfer Capacitance	$C_{RSS}$		-	100	-	pF
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Pad Area = $0.171\text{in}^2$ (see note 2)	-	-	110	$^\circ\text{C}/\text{W}$
		Pad Area = $0.068\text{in}^2$	-	-	128	$^\circ\text{C}/\text{W}$
		Pad Area = $0.026\text{in}^2$	-	-	147	$^\circ\text{C}/\text{W}$

## Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	$V_{SD}$	$I_{SD} = 2.0\text{A}$	-	-	1.5	V
Reverse Recovery Time	$t_{rr}$	$I_{SD} = 2.0\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	100	ns

### NOTE:

- $110^\circ\text{C}/\text{W}$  measured using FR-4 board with  $0.171\text{in}^2$  footprint for 1000 seconds.

Typical Performance Curves Unless otherwise specified

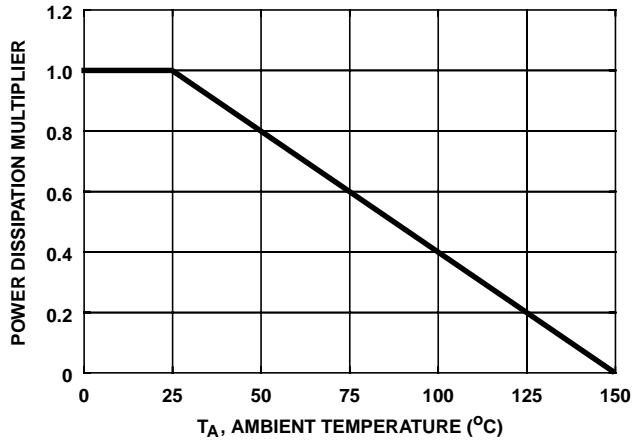


FIGURE 1. NORMALIZED POWER DISSIPATION vs AMBIENT TEMPERATURE

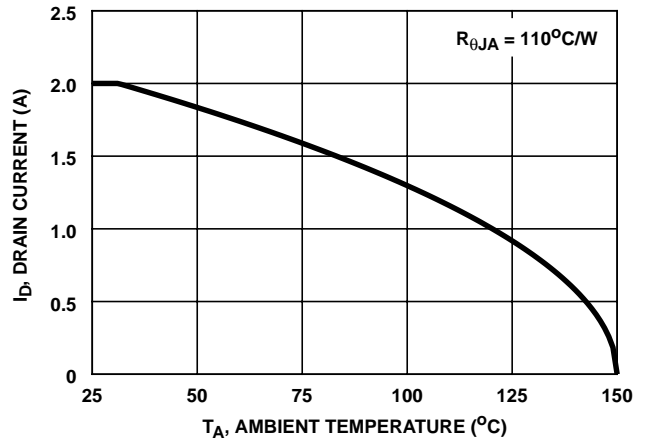


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs AMBIENT TEMPERATURE

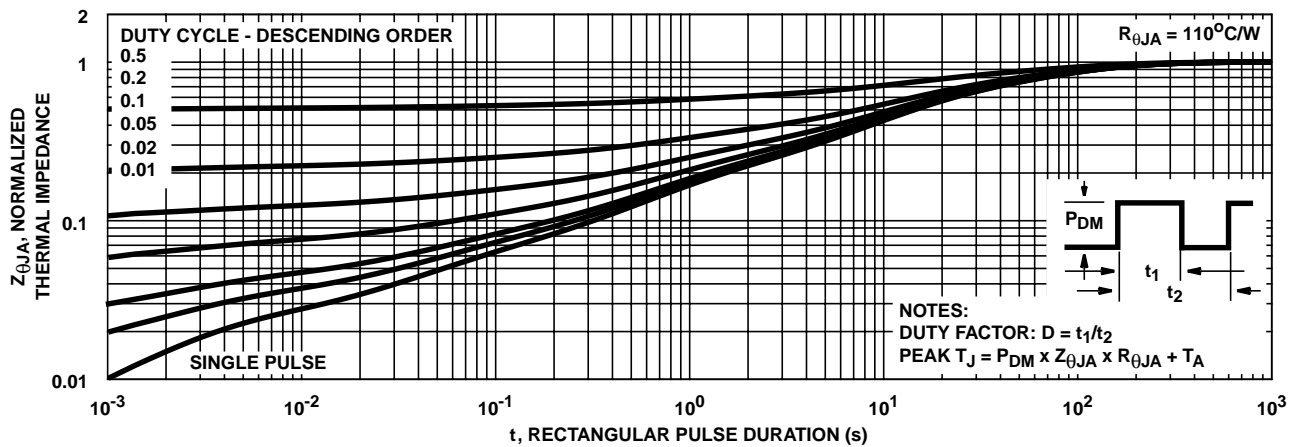


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

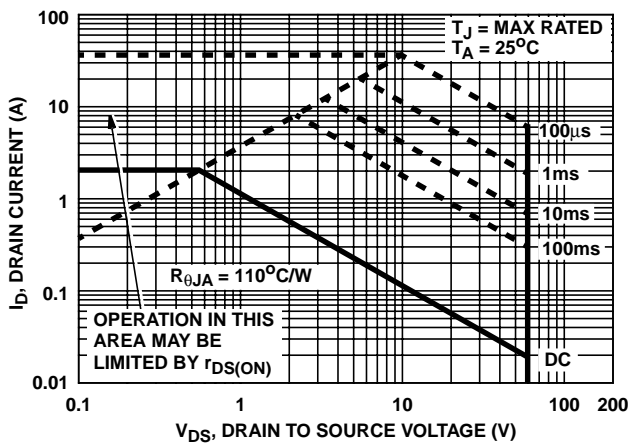


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

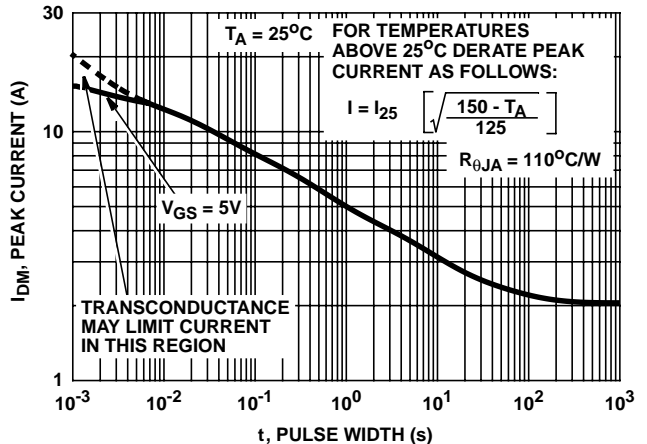
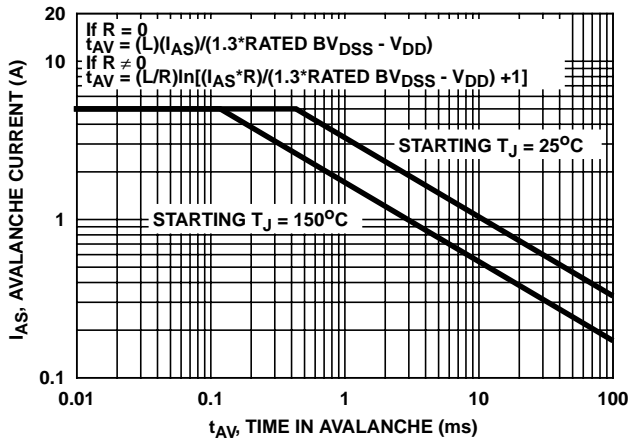


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves Unless otherwise specified (Continued)



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.  
 FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

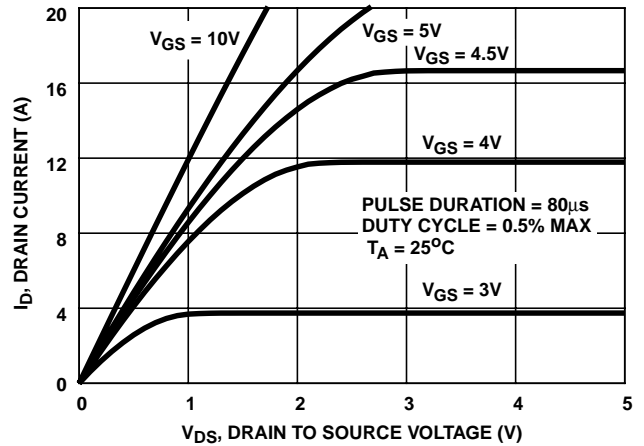


FIGURE 7. SATURATION CHARACTERISTICS

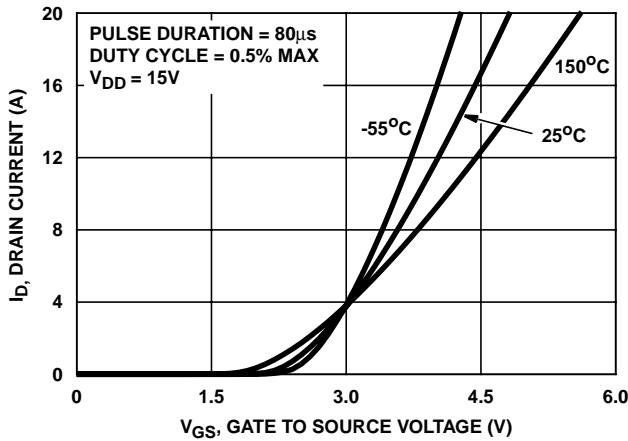


FIGURE 8. TRANSFER CHARACTERISTICS

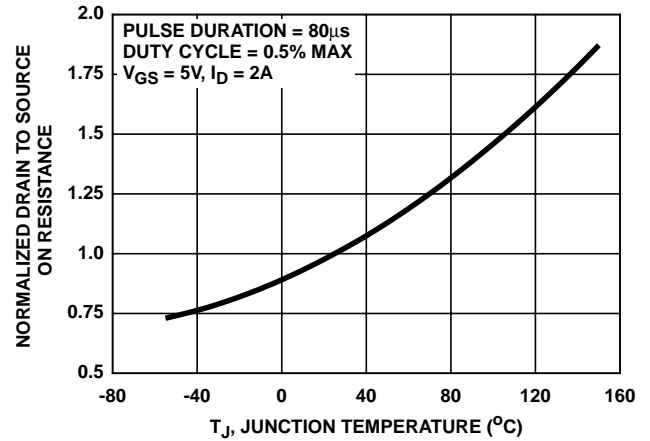


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

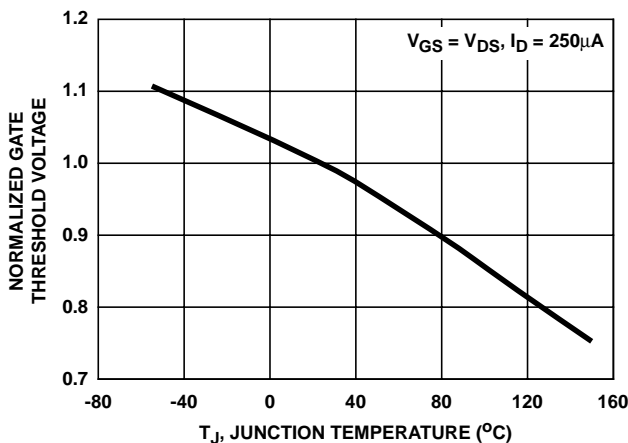


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

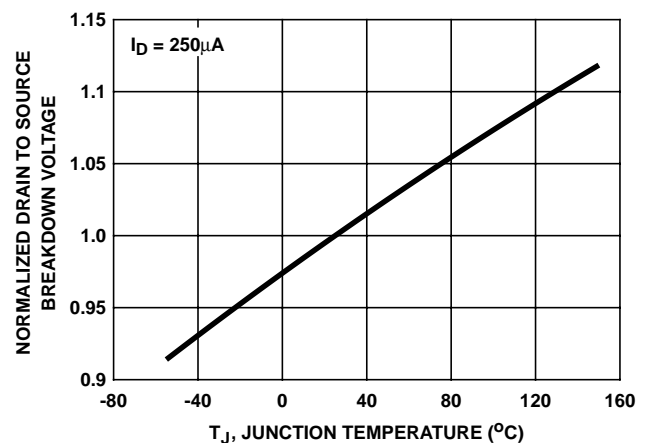


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

**Typical Performance Curves** Unless otherwise specified (Continued)

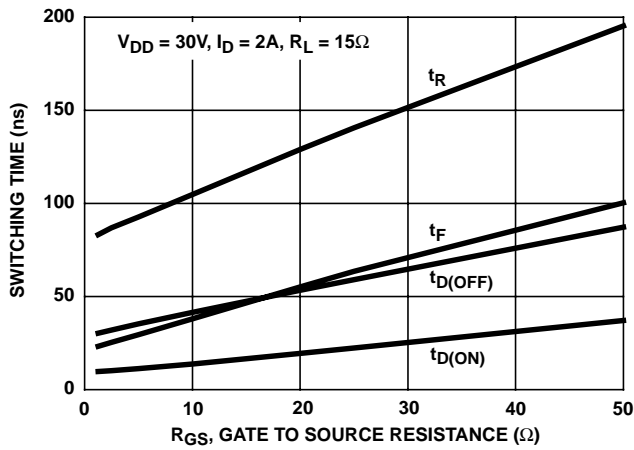


FIGURE 12. SWITCHING TIME vs GATE RESISTANCE

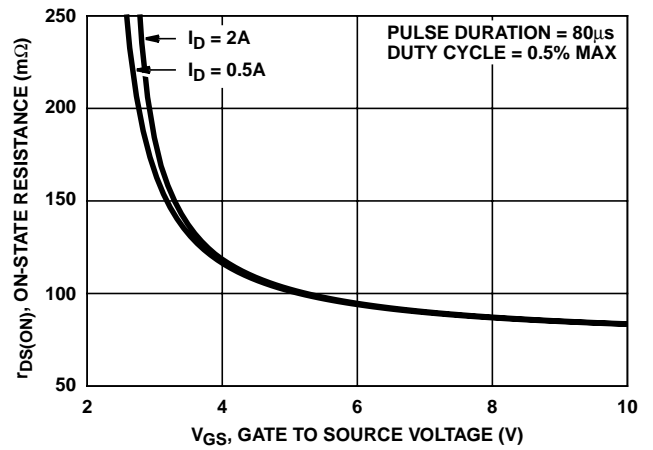


FIGURE 13. SOURCE TO DRAIN ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

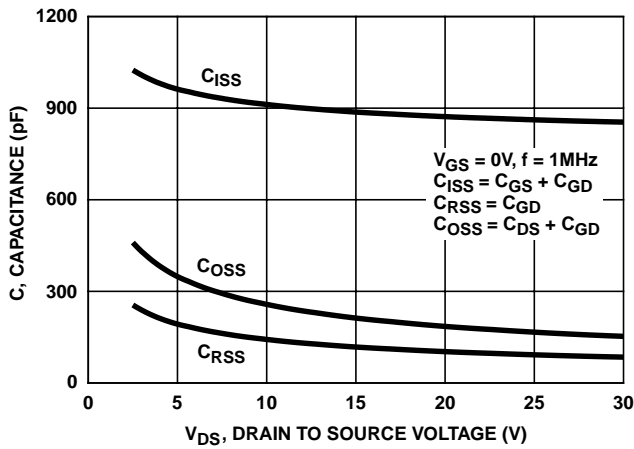
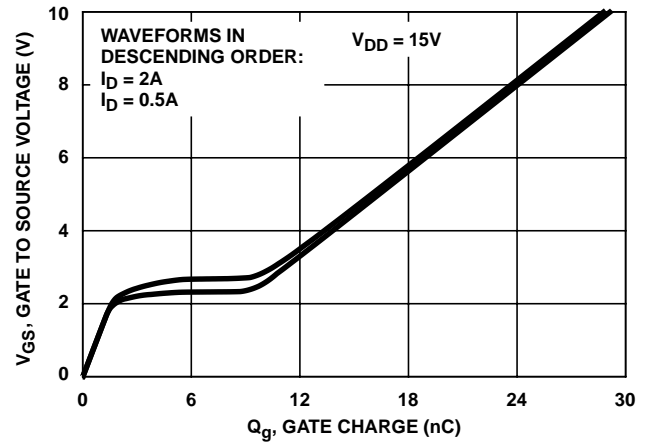


FIGURE 14. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 15. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

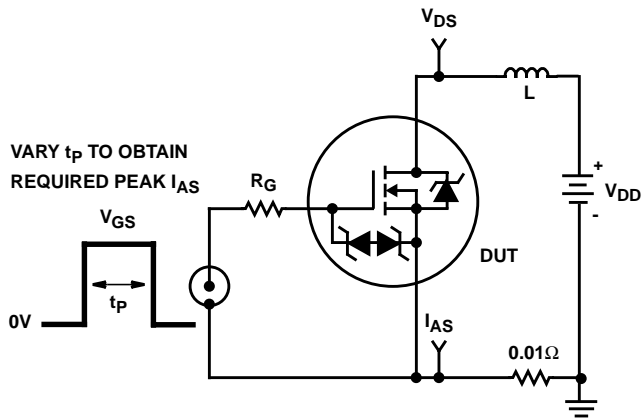


FIGURE 16. UNCLAMPED ENERGY TEST CIRCUIT

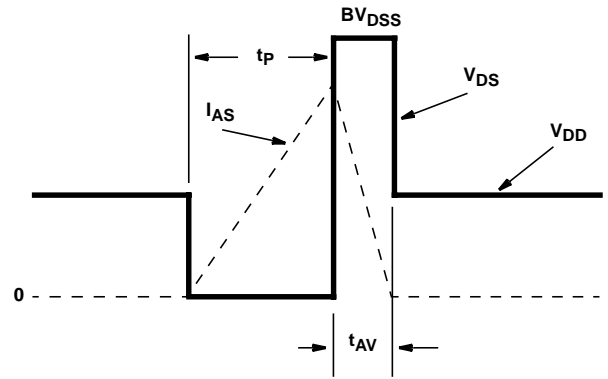


FIGURE 17. UNCLAMPED ENERGY WAVEFORMS

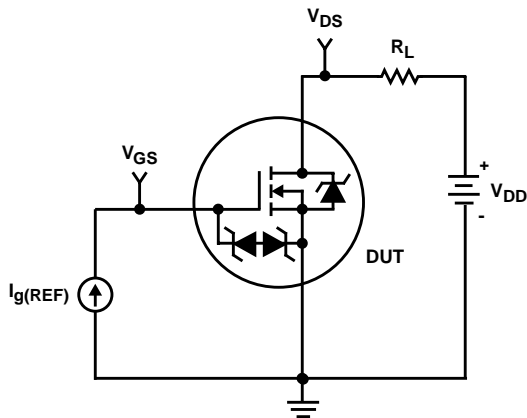


FIGURE 18. GATE CHARGE TEST CIRCUIT

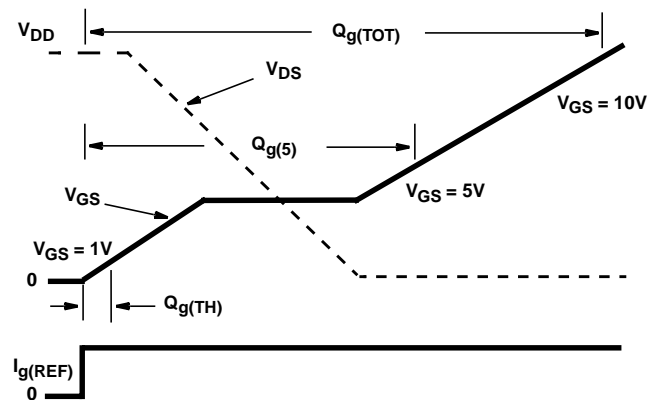


FIGURE 19. GATE CHARGE WAVEFORM

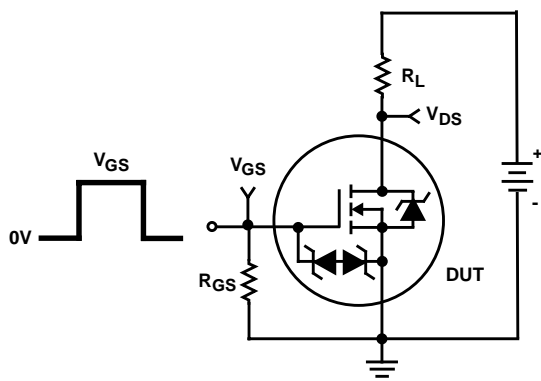


FIGURE 20. SWITCHING TIME TEST CIRCUIT

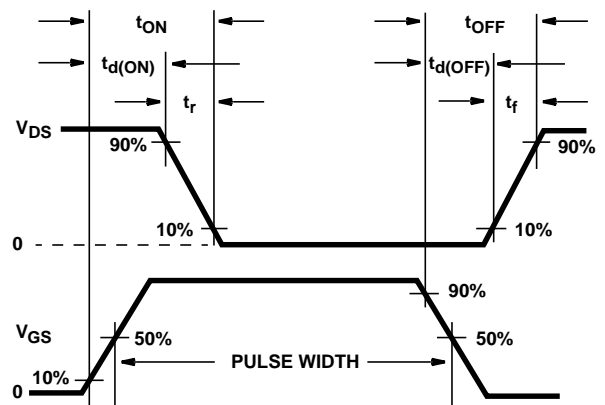


FIGURE 21. RESISTIVE SWITCHING WAVEFORMS

## Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature,  $T_{J(MAX)}$ , and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation,  $P_{D(MAX)}$ , in an application. Therefore the application's ambient temperature,  $T_A$  ( $^{\circ}C$ ), and thermal impedance  $R_{\theta JA}$  ( $^{\circ}C/W$ ) must be reviewed to ensure that  $T_{J(MAX)}$  is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_A)}{R_{\theta JA}} \quad (\text{EQ. 1})$$

In using surface mount devices such as the SOT-223 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of the  $P_{D(MAX)}$  is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Intersil provides thermal information to assist the designer's preliminary application evaluation. Figure 22 defines the  $R_{\theta JA}$  for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Intersil device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

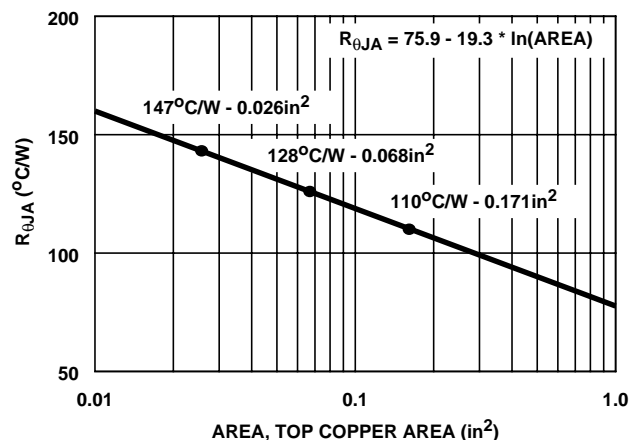


FIGURE 22. THERMAL RESISTANCE vs MOUNTING PAD AREA

Displayed on the curve are the three  $R_{\theta JA}$  values listed in the Electrical Specifications table. The three points were chosen to depict the compromise between the copper board area, the thermal resistance and ultimately the power dissipation,  $P_{D(MAX)}$ . Thermal resistances corresponding to other component side copper areas can be obtained from Figure 22 or by calculation using Equation 2. The area, in square inches is the top copper area including the gate and source pads.

$$R_{\theta JA} = 75.9 - 19.3 \times \ln(\text{Area}) \quad (\text{EQ. 2})$$

**PSPICE Electrical Model**

.SUBCKT RFT3055LE 2 1 3 ; REV May 98

CA 12 8 1.68e-9  
 CB 15 14 1.78e-9  
 CIN 6 8 7.69e-10

DBODY 7 5 DBODYMOD  
 DBREAK 5 11 DBREAKMOD  
 DESD1 91 9 DESD1MOD  
 DESD2 91 7 DESD2MOD  
 DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 64.28  
 EDS 14 8 5 8 1  
 EGS 13 8 6 8 1  
 ESG 6 10 6 8 1  
 EVTHRES 6 21 19 8 1  
 EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-9  
 LGATE 1 9 4.6e-9  
 LSOURCE 3 7 4.6e-9

MMED 16 6 8 8 MMEDMOD  
 MSTRO 16 6 8 8 MSTROMOD  
 MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1  
 RDRAIN 50 16 RDRAINMOD 24e-3  
 RGATE 9 20 9.84  
 RLDRAIN 2 5 10  
 RLGATE 1 9 46  
 RLSOURCE 3 7 46  
 RSLC1 5 51 RSLCMOD 1e-6  
 RSLC2 5 50 1e3  
 RSOURCE 8 7 RSOURCEMOD 49e-3  
 RVTHRES 22 8 RVTHRESMOD 1  
 RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD  
 S1B 13 12 13 8 S1BMOD  
 S2A 6 15 14 13 S2AMOD  
 S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

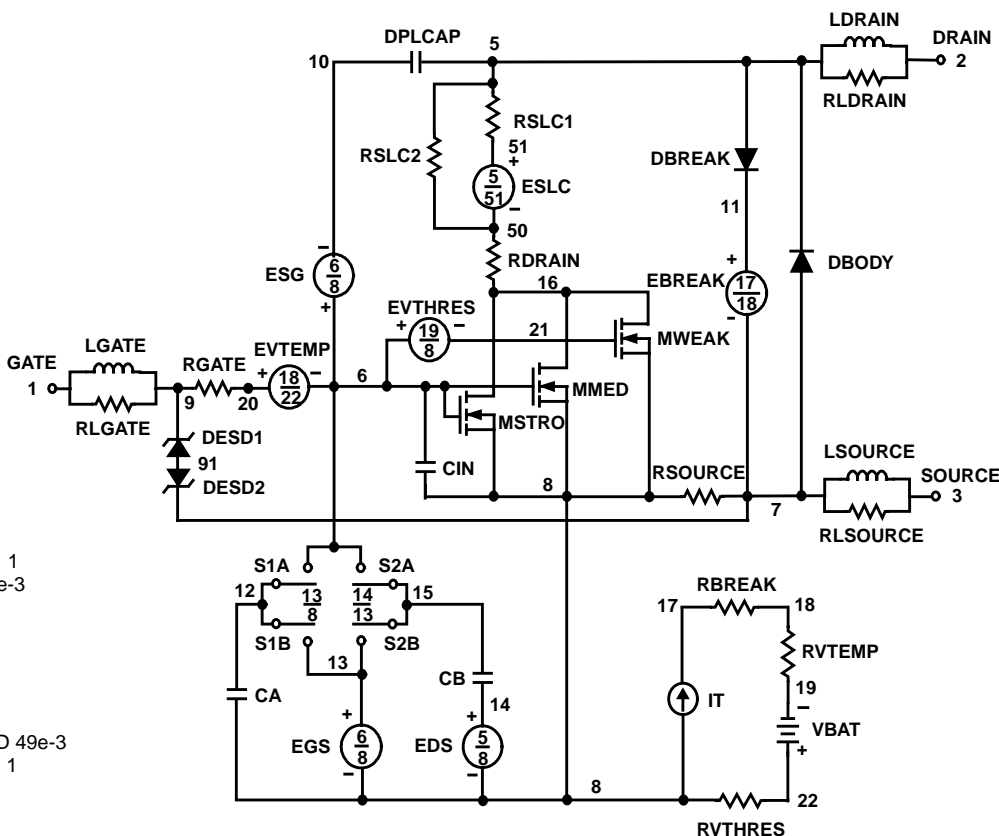
ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))\*(PWR(V(5,51)/(1e-6\*45),4))}

```
.MODEL DBODYMOD D (IS = 3.61e-13 RS = 1.78e-2 TRS1 = 1.7e-2 TRS2 = -4.69e-6 CJO = 3.88e-10 TT = 3.6e-8)
.MODEL DBREAKMOD D (RS = 4.73e-1 TRS1 = -2.19e-3 TRS2 = 4.7e-5)
.MODEL DESD1MOD D (BV = 12.5 NBV = 17.5 IBV = 2.5e-4 RS = 0)
.MODEL DESD2MOD D (BV = 12.86 NBV = 22 IBV = 2.5e-4 RS = 0)
.MODEL DPLCAPMOD D (CJO = 4.803e-10 IS = 1e-30 N = 10)
.MODEL MMEDMOD NMOS (VTO = 1.78 KP = 1.5 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 9.84)
.MODEL MSTROMOD NMOS (VTO = 2.08 KP = 10.5 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 1.55 KP = 0.1 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 98.4 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 1.06e-3 TC2 = -6.22e-7)
.MODEL RDRAINMOD RES (TC1 = 4.5e-3 TC2 = 6e-5)
.MODEL RSLCMOD RES (TC1 = 0 TC2 = 0)
.MODEL RSOURCEMOD RES (TC1 = 0 TC2 = 0)
.MODEL RVTHRESMOD RES (TC = 0 TC2 = -4e-6)
.MODEL RVTEMPMOD RES (TC1 = -1.9e-3 TC2 = 1.3e-7)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.4 VOFF = -2.4)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.4 VOFF = -4.4)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.0 VOFF = 1.15)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 1.15 VOFF = -2.0)
```

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.





**SPICE Thermal Model**

REV May 98

RFT3055LE

Copper Area = 0.077in<sup>2</sup>

CTHERM1 9 8 7.5e-5

CTHERM2 8 7 3.5e-4

CTHERM3 7 6 1.2e-3

CTHERM4 6 5 1.5e-2

CTHERM5 5 4 6.0e-2

CTHERM6 4 3 3.0e-1

CTHERM7 3 2 1.6

CTHERM8 2 1 6

RTHERM1 9 8 8.2e-2

RTHERM2 8 7 2.7e-1

RTHERM3 7 6 1.9

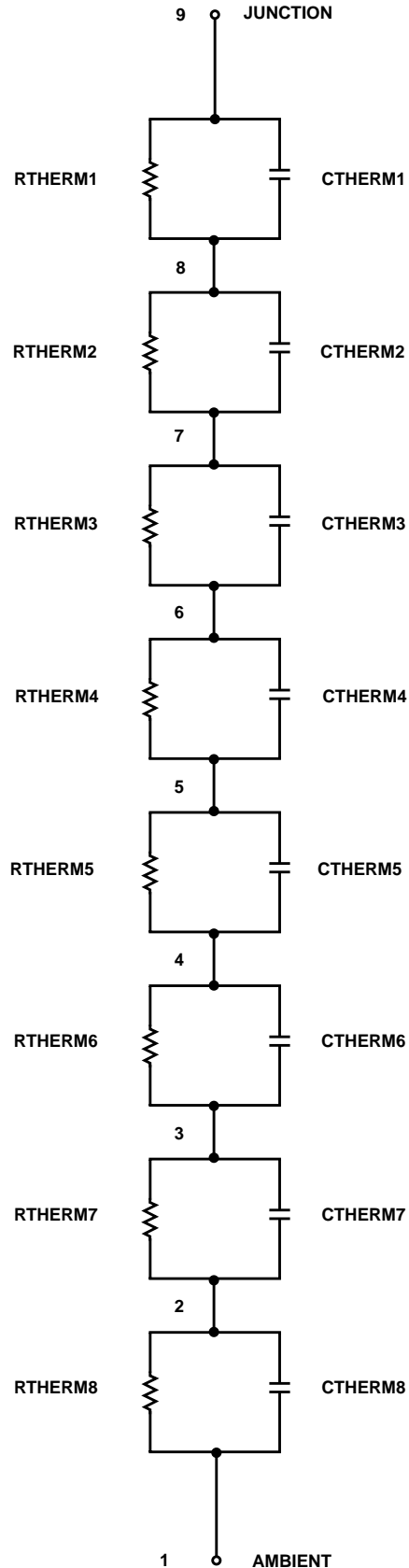
RTHERM4 6 5 3.1

RTHERM5 5 4 12

RTHERM6 4 3 38

RTHERM7 3 2 32

RTHERM8 2 1 22



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