TOSHIBA

DISCONTINUATION NOTICE
TB62705CPG,TB62705CFG,TB62705CFNG SERIES

THE FOLLOWING HAVE BEEN DISCONTINUED AS OF MAR 2009:

TB62705CPG
TB62705CFG
TB62705CFGEL
TB62705CFNG
TB62705CFNGEL

STOCK IS LIMITED ON ABOVE PLEASE SEE SUGGESTED REPLACEMENT DRIVERS:

TB62777FNGEL
TB62778FNGEL

CONTACT MARKTECH ENGINEERING OR SALES FOR APPLICATION ASSISTANCE

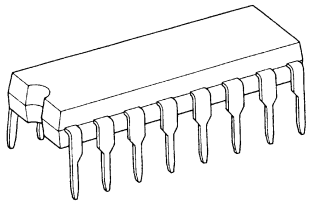
TOSHIBA Bi−CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

TB62705CPG, TB62705CFG, TB62705CFNG

8-BIT SHIFT REGISTER, LATCHES & CONSTANT-CURRENT DRIVERS

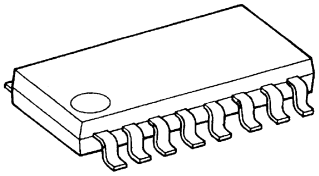
The TB62705CPG / CFG / CFNG are specifically designed for LED and LED DISPLAY constant-current drivers.
These constant-current output circuits can support the set-up of an external resistor (I_{OUT} = 5~90mA).
This I_C is a monolithic integrated circuit designed to be used together with Bi-CMOS process.
The devices consist of an 8-bit shift register, latch, AND-GATE and constant-current drivers.
This devices are a product for the Pb free(Sn-Ag).

TB62705CPG



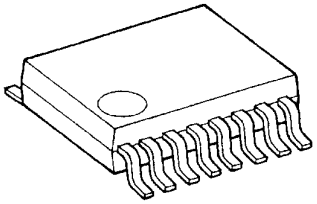
DIP16-P-300-2.54A

TB62705CFG



SSOP16-P-225-1.00A

TB62705CFNG



SSOP16-P-225-0.65B

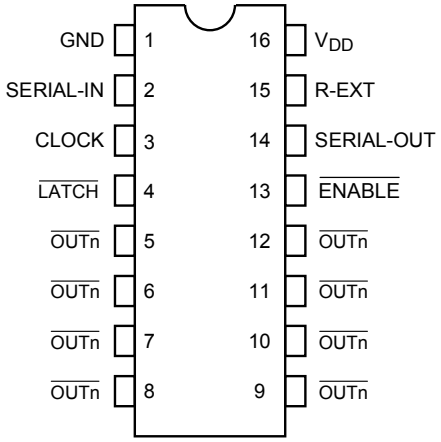
Weight
DIP16−P−300−2.54A : 1.11 g (typ.)
SSOP16−P−225−1.00A : 0.14 g (typ.)
SSOP16−P−225−0.65B : 0.07 g (typ.)

FEATURES

- Constant-current Output : current with one resistor for 5 to 90mA.
- Maximum Clock Frequency : f_{CLK} = 15 (MHz) (Cascade Connecte Operate, Topr = 25°C)
- 5V C−MOS Compatible Input
- Package : DIP16−P−300−2.54A (TB62705CPG)
  SSOP16−P−225−1.00A (TB62705CFG)
  SSOP16−P−225−0.65B (TB62705CFNG)
- Constant Output Current Matching:

OUTPUT-GND VOLTAGE	CURRENT MATCHING	OUTPUT CURRENT
≥ 0.4 V	±6.0%	5~40 mA
≥ 0.7 V	±6.0%	5~90 mA

PIN CONNECTION (Top view)



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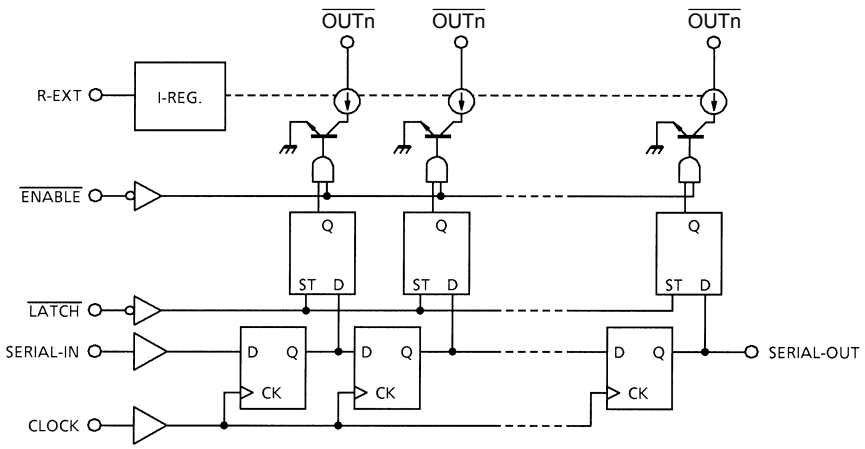
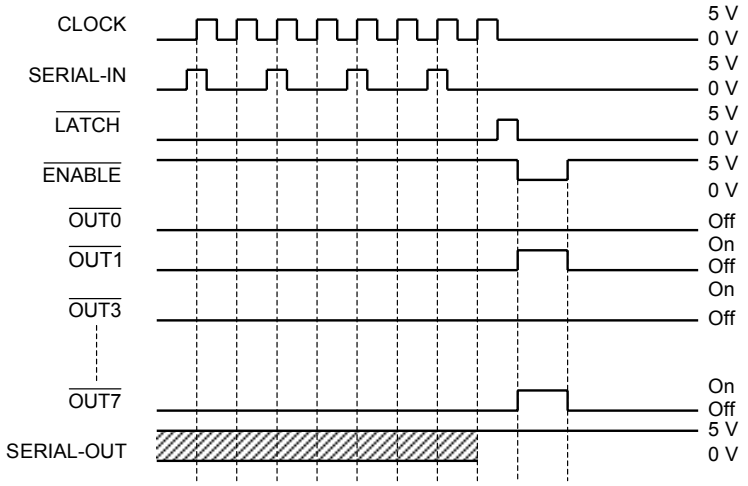
BLOCK DIAGRAM



TIMING DIAGRAM



Note: Latches are level-sensitive, not rising edge-sensitive, and are not synchronized with the CLOCK signal. The data will pass through the latch circuit if the latch input is set at “H” level, and will be retained if the input is set at “L”.

PIN DESCRIPTION

PIN No.	PIN NAME	FUNCTION
1	GND	GND terminal for control logic
2	SERIAL−IN	Input pin for shift register serial data
3	CLOCK	Clock input terminal for data shift to up-edge.
4	$\overline{\text{LATCH}}$	Data strobe input terminal. Latches pass $\overline{\text{LATCH}}$ data with “H” level input and retain data with “L” level input.
5~12	$\overline{\text{OUTn}}$	Output terminals
13	$\overline{\text{ENABLE}}$	Input terminal for output enable. All outputs ($\overline{\text{OUTn}}$) go off with $\overline{\text{ENABLE}}$ data input at "H" level and go on with data input at "L" level.
14	SERIAL−OUT	Output terminal for serial data for the next SERIAL-IN terminal.
15	R−EXT	Input terminal for connecting a resistor to regulate all output currents.
16	V_{DD}	5-V supply pin of the IC

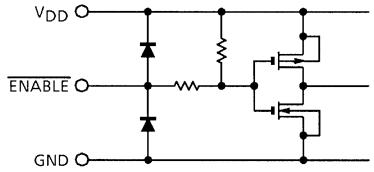
TRUTH TABLE

CLOCK	$\overline{\text{LATCH}}$	$\overline{\text{ENABLE}}$	SERIAL−IN	$\overline{\text{OUTn}}$	SERIAL−OUT
UP	H	L	D_n	$D_n \cdots D_{n-5} \cdots D_{n-7}$	D_{n-7}
UP	L	L	D_{n+1}	No change	D_{n-6}
UP	H	L	D_{n+2}	$D_{n+2} \cdots D_{n-3} \cdots D_{n-5}$	D_{n-5}
DOWN	X	L	D_{n+3}	$D_{n+2} \cdots D_{n-3} \cdots D_{n-5}$	D_{n-5}
DOWN	X	H	D_{n+3}	Off	D_{n-5}

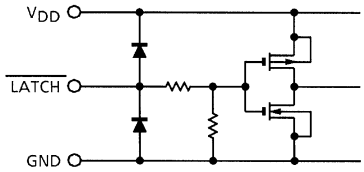
Note: $\overline{\text{OUTn}}$ = on if D_n = H level, and $\overline{\text{OUTn}}$ = off if D_n = L level.
An external resistor is connected with R−EXT and GND. Be sure to administer the correct power supply voltage.

INPUT/OUTPUT EQUIVALENT CIRCUITS

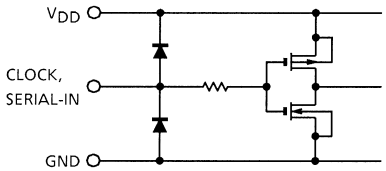
1. $\overline{\text{ENABLE}}$ terminal



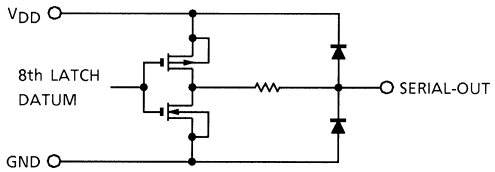
2. $\overline{\text{LATCH}}$ terminal



3. CLOCK, SERIAL−IN terminal



4. SERIAL−OUT terminal



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	0~7.0	V
Input Voltage	V_{IN}	−0.4~V_{DD} + 0.4	V
Output Current	I_{OUT}	90	mA
Output Voltage	V_{CE}	−0.5~17.0	V
Clock Frequency	f_{CK}	15	MHz
GND Terminal Current	I_{GND}	720	mA
Power Dissipation	P_D	1.47 (CPG−type : FREE AIR, Ta = 25°C)	W
		0.78 (CFG / CFNG−type : ON PCB, Ta = 25°C)	
Thermal Resistance	$R_{th\ (j-a)}$	85 (CPG−type : FREE AIR, Ta = 25°C)	°C / W
		160 (CFG / CFNG−type : ON PCB, Ta = 25°C)	
Operating Temperature	T_{opr}	−40~85	°C
Storage Temperature	T_{stg}	−55~150	°C

Note: CPG type: For an ambient temperature above 25°C, the derating is 11.8 mW/°C.
CFG and CFNG type: For an ambient temperature above 25°C, the derating is 6.3 mW/°C.

RECOMMENDED OPERATING CONDITION (Ta = −40~85°C unless otherwise stated)

CHARACTERISTIC	SYMBOL	CONDITION	MIN	TYP.	MAX	UNIT
Supply Voltage	V_{DD}	—	4.5	5.0	5.5	V
Output Voltage	V_{OUT}	—	—	—	15.0	V
Output Current	I_O	$\overline{OUTn}$, DC 1 circuit	5	—	88	mA
	I_{OH}	SERIAL−OUT	—	—	1.0	
	I_{OL}	SERIAL−OUT	—	—	−1.0	
Input Voltage	V_{IH}	—	0.7 V_{DD}	—	V_{DD} +0.3	V
	V_{IL}	—	−0.3	—	0.3 V_{DD}	
LATCH Pulse Width	$t_{w\ LAT}$	V_{DD} = 4.5~5.5 V	100	—	—	ns
CLOCK Pulse Width	$t_{w\ CLK}$		50	—	—	ns
ENABLE Pulse Width	$t_{w\ EN}$		4500	—	—	ns
Set-up Time for DATA	$t_{setup\ (D)}$		60	—	—	ns
Hold Time for DATA	$t_{hold\ (D)}$		20	—	—	ns
Set-up Time for LATCH	$t_{setup\ (L)}$		100	—	—	ns
Hold Time for LATCH	$t_{hold\ (L)}$		60	—	—	ns
Clock Frequency	f_{CK}	Cascade operation	10.0	—	—	MHz
Power Dissipation	P_D	Ta = 85°C (CPG−type FREE AIR)	—	—	0.82	W
		Ta = 85°C (CFG / CFNG−type ON PCB)	—	—	0.40	

ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 V, Ta = 25°C unless otherwise stated)

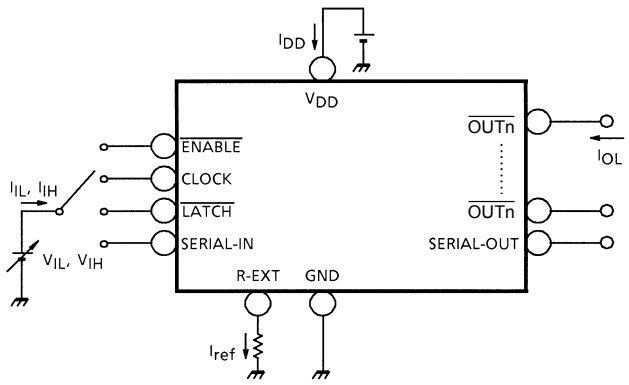
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	CONDITION		MIN	TYP.	MAX	UNIT
Input Voltage	"H" Level	V_{IH}	—	—		0.7 V_{DD}	—	V_{DD}	V
	"L" Level	V_{IL}	—	—		GND	—	0.3 V_{DD}	
Output Leakage Current		I_{OH}	—	V_{OH} = 15.0 V		—	—	10	μA
Output Voltage	S-OUT	V_{OL}	—	I_{OL} = 1.0 mA		—	—	0.4	V
		V_{OH}	—	I_{OH} = −1.0 mA		4.6	—	—	
Output Current 1		I_{OL1}	—	V_{CE} = 0.7 V	R_{EXT} = 470 Ω (Include skew)	34.1	40.0	45.9	mA
		I_{OL2}	—	V_{CE} = 0.4 V		33.7	39.5	45.3	
	Current Skew	ΔI_{OL1}	—	I_O = 40 mA, VCE = 0.4 V	R_{EXT} = 470 Ω	—	±1.5	±6.0	%
Output Current 2		I_{OL3}	—	V_{CE} = 1.0 V	R_{EXT} = 250 Ω (Include skew)	64.2	75.5	86.8	mA
		I_{OL4}	—	V_{CE} = 0.7 V		63.8	75.0	86.2	
	Current Skew	ΔI_{OL2}	—	I_O = 75 mA, V_{CE} = 0.7 V	R_{EXT} = 250 Ω	—	±1.5	±6.0	%
Supply Voltage Regulation		% / V_{DD}	—	R_{EXT} = 470 Ω, Ta = −40~85°C		—	1.5	5.0	% / V
Pull-Up Resistor		$R_{IN (up)}$	—	—		150	300	600	kΩ
Pull-Down Resistor		$R_{IN (down)}$	—	—		100	200	400	kΩ
Supply Current	"OFF"	$I_{DD (off) 1}$	—	R_{EXT} = OPEN, $\overline{OUT0 \sim 7}$ = off		—	0.6	1.2	mA
		$I_{DD (off) 2}$	—	R_{EXT} = 470 Ω, $\overline{OUT0 \sim 7}$ = off		3.5	5.8	8.0	
		$I_{DD (off) 3}$	—	R_{EXT} = 250 Ω, $\overline{OUT0 \sim 7}$ = off		6.5	10.7	15.0	
	"ON"	$I_{DD (on) 1}$	—	R_{EXT} = 470 Ω, $\overline{OUT0 \sim 7}$ = on		7.0	12.0	18.0	
		$I_{DD (on) 2}$	—	R_{EXT} = 250 Ω, $\overline{OUT0 \sim 7}$ = on		10.0	22.0	32.0	

SWITCHING CHARACTERISTICS (Ta = 25°C unless otherwise stated)

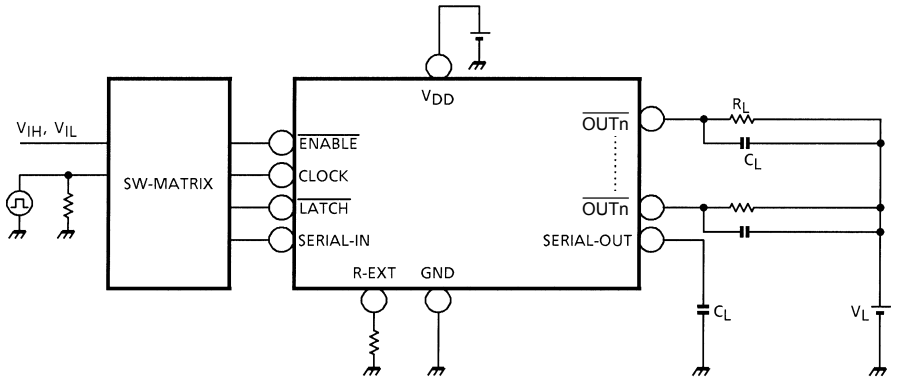
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	CONDITION	MIN	TYP.	MAX	UNIT
Propagation Delay Time ("L" to "H")	SIN- $\overline{OUTn}$	t_{pLH}	—	V_{DD} = 5.0 V V_{CE} = 0.4 V V_{IH} = V_{DD} V_{IL} = GND R_{EXT} = 470 Ω I_{OUT} = 40 mA V_L = 3.0 V R_L = 65 Ω C_L = 10.5 pF	—	1200	1500	ns
	$\overline{LATCH}$ - $\overline{OUTn}$				—	1200	1500	
	$\overline{ENABLE}$ - $\overline{OUTn}$				—	1200	1500	
	CLK-SOUT				—	30	70	
Propagation Delay Time ("H" to "L")	SIN - $\overline{OUTn}$	t_{pHL}	—		—	700	1000	ns
	$\overline{LATCH}$ - $\overline{OUTn}$				—	700	1000	
	$\overline{ENABLE}$ - $\overline{OUTn}$				—	700	1000	
	CLK-SOUT				—	30	70	
Pulse Width	CK	$t_{w\ CLK}$	—		—	20	30	ns
	LATCH	$t_{w\ LAT}$	—		—	10	25	
Set-up Time for LATCH	L-H	t_{setup}	—		—	25	50	ns
	H-L				—	25	50	
Hold Time for LATCH	L-H	t_{hold}	—		—	0	30	ns
	H-L				—	0	30	
Maximum CLOCK Rise Time		t_r	—		—	—	10	μs
Maximum CLOCK Fall Time		t_f	—		—	—	10	μs
Output Rise Time		t_{or}	—		300	600	1000	ns
Output Fall Time		t_{of}	—		150	300	600	ns

TEST CIRCUIT

DC characteristics



AC characteristics

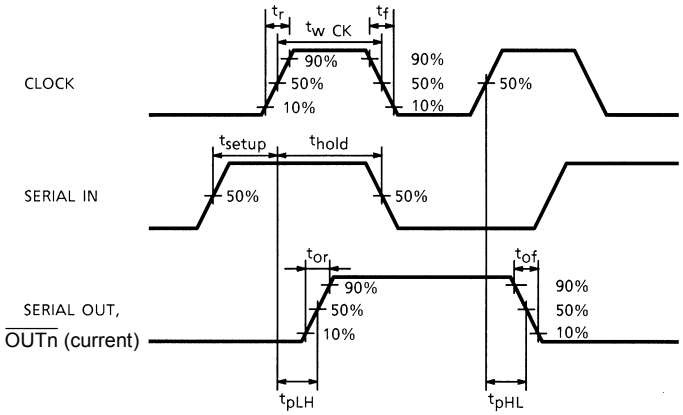


Precaution on Use

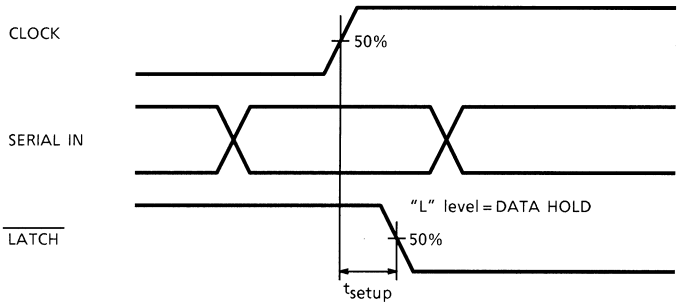
Utmost care is necessary in the design of the output line, V_{CC} (V_{DD}) and GND line since the IC may be damaged due to short-circuits between outputs, air contamination faults, or faults caused by improper grounding.

TIMING WAVEFORM

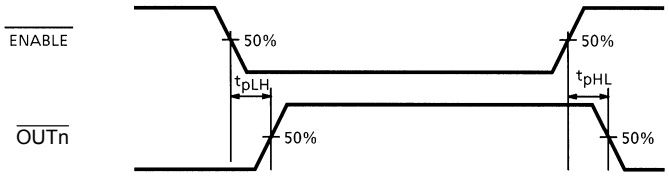
1. CLOCK−SERIAL OUT, $\overline{OUTn}$



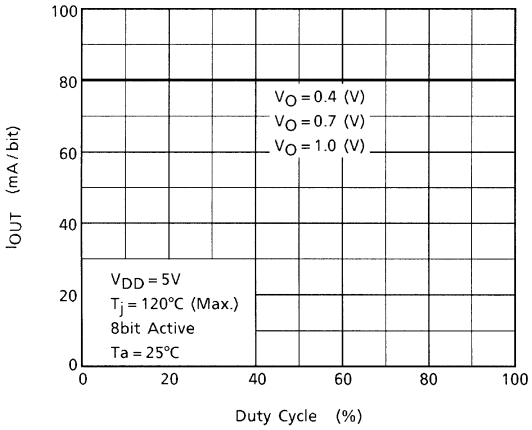
2. CLOCK− $\overline{LATCH}$



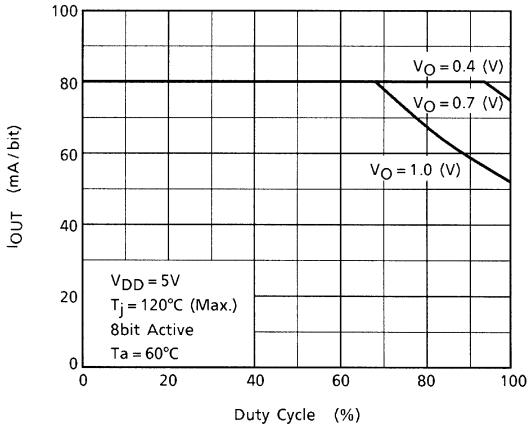
3. $\overline{ENABLE}$ − $\overline{OUTn}$



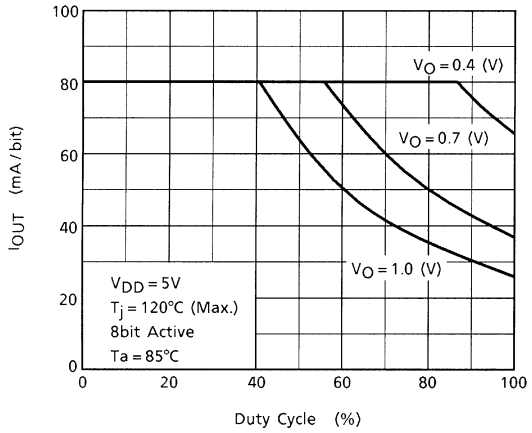
Iout-Duty Cycle (TB62705CFG/CFNG)



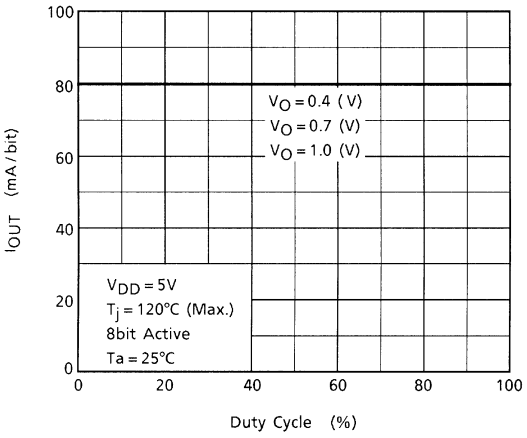
Iout-Duty Cycle (TB62705CFG/CFNG)



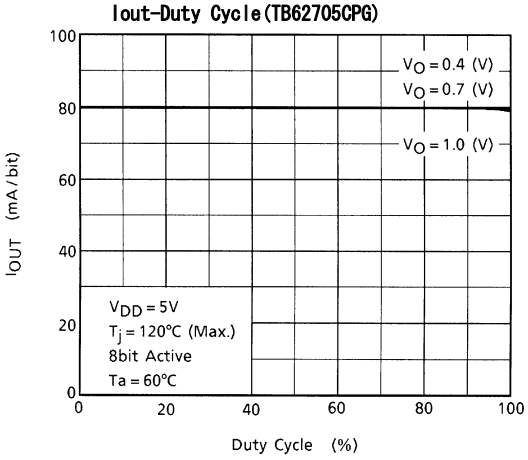
Iout-Duty Cycle (TB62705CFG/CFNG)



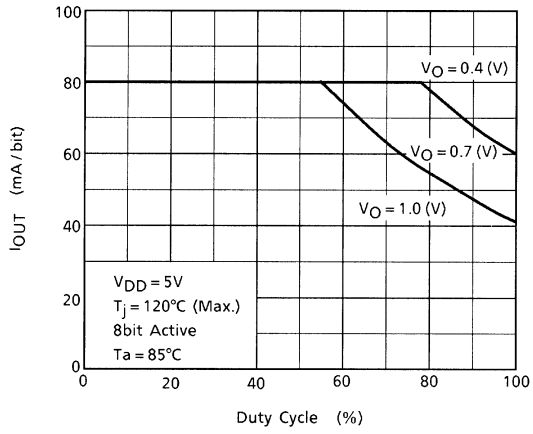
Iout-Duty Cycle (TB62705CPG)



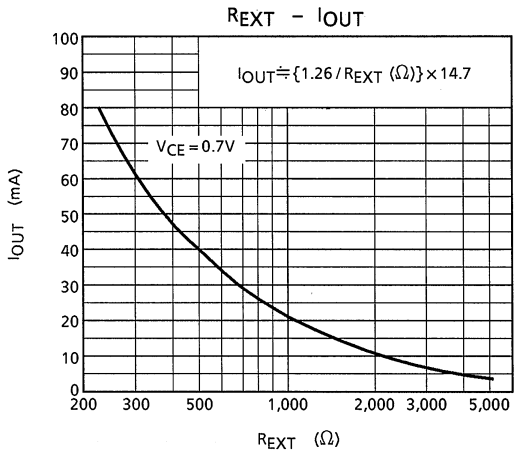
Iout-Duty Cycle (TB62705CPG)

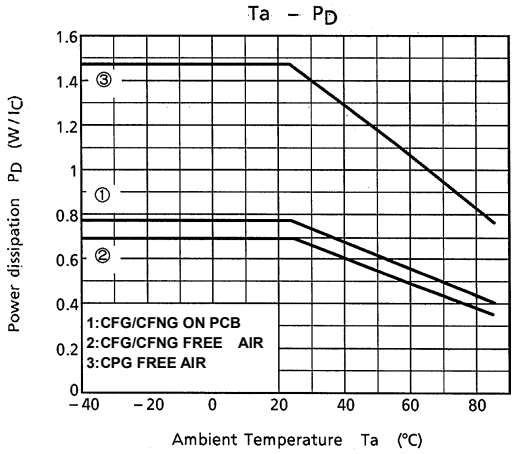


Iout-Duty Cycle (TB62705CPG)



LED DRIVER TB6270X SERIES APPLICATION NOTE





[1] Output current (I_{OUT})

I_{OUT} is set by the external resistor (R−EXT), as shown in Fig. 1.

[2] Total supply voltage (VLED)

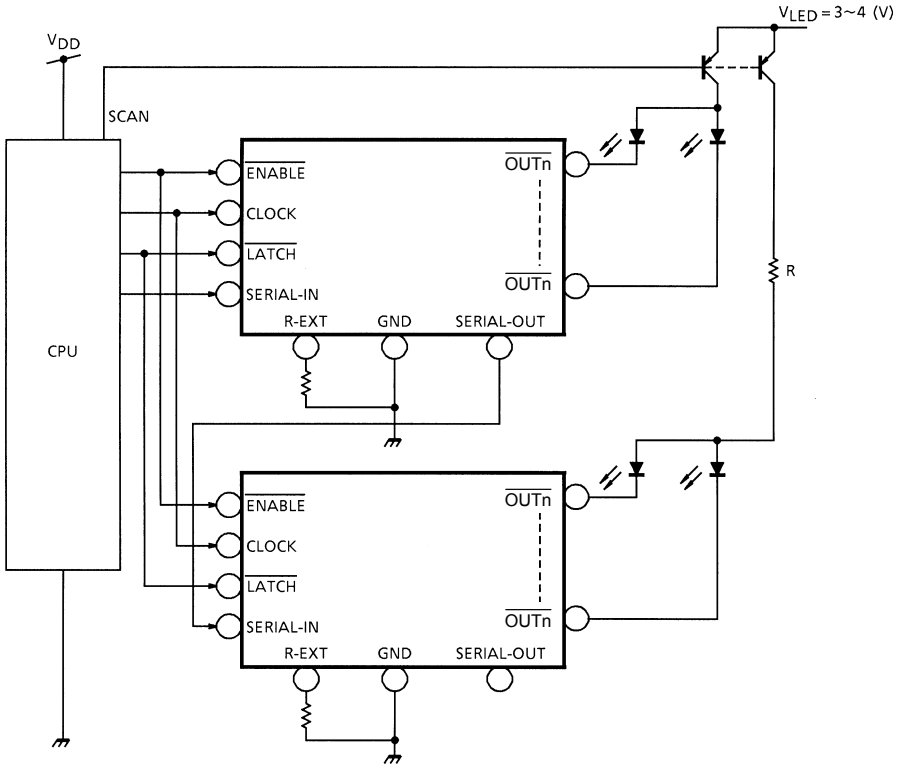
This device can operate on 0.4~0.7 V (V_O).

When a higher voltage is input to the device, the excess voltage is consumed inside the device, which leads to power dissipation. To minimize power dissipation and loss, we recommend that the total supply voltage be set as follows:

V_{LED} (total supply voltage) = V_{CE} (T_r V_{sat}) + V_f (LED forward voltage) + V_O (I_C supply voltage).

When the total supply is too high in the light of the power dissipation of this device, an additional resistor (R) can be used to decrease the supply voltage (V_O).

PATTERN LAYOUT



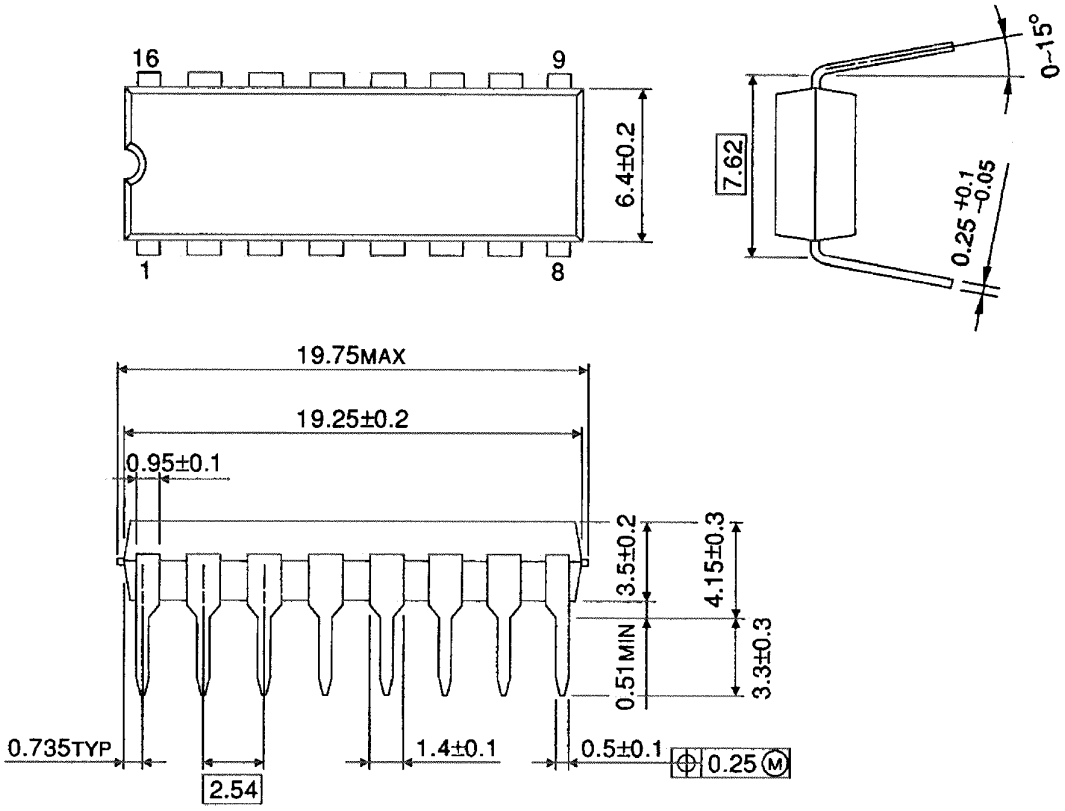
[3] Pattern layout

This device has only one ground pin, i.e., the combined signal ground pin and power ground pin.

If the ground pattern layout contains a large amount of inductance and impedance, and the voltage between the ground and LATCH or CLOCK terminals exceeds 2.5 V due to switching noise, the device may not operate correctly. Be sure to pay attention to pattern layout to minimize inductance.

PACKAGE DIMENSIONS

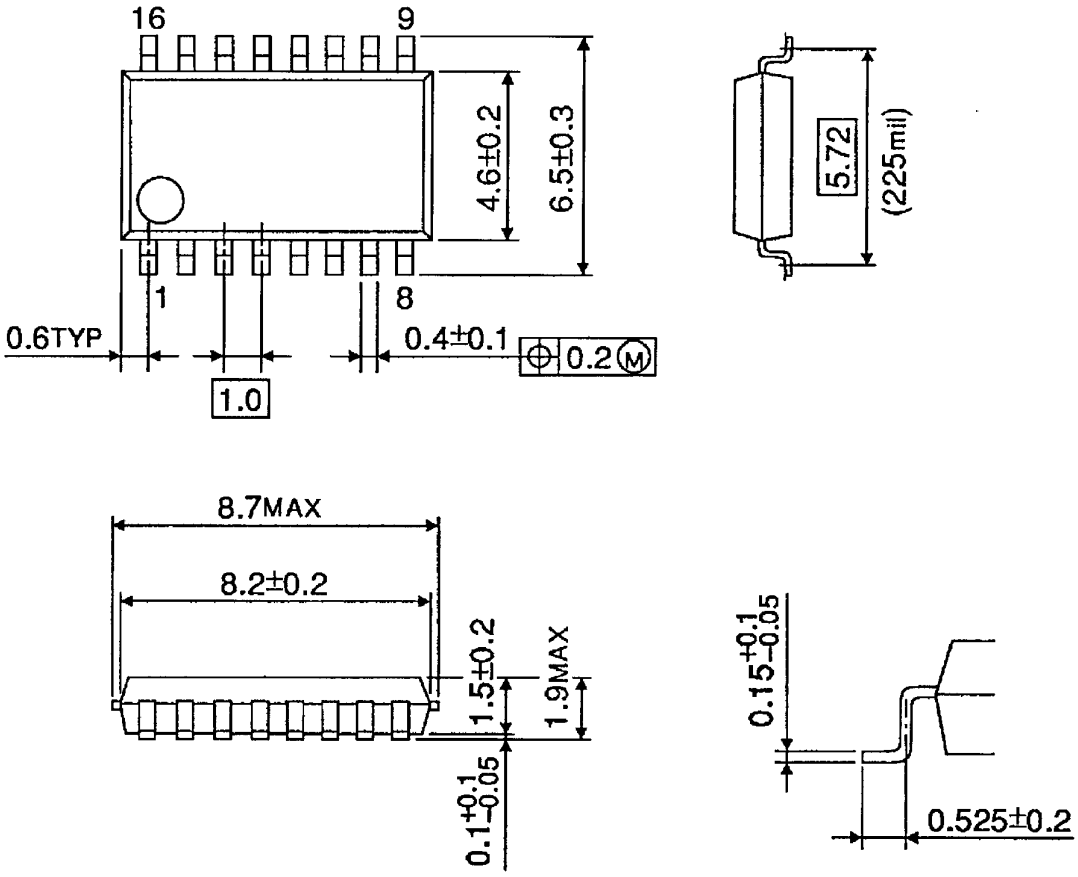
DIP16-P-300-2.54A Unit : mm



Weight: 1.11 g (Typ.)

PACKAGE DIMENSIONS

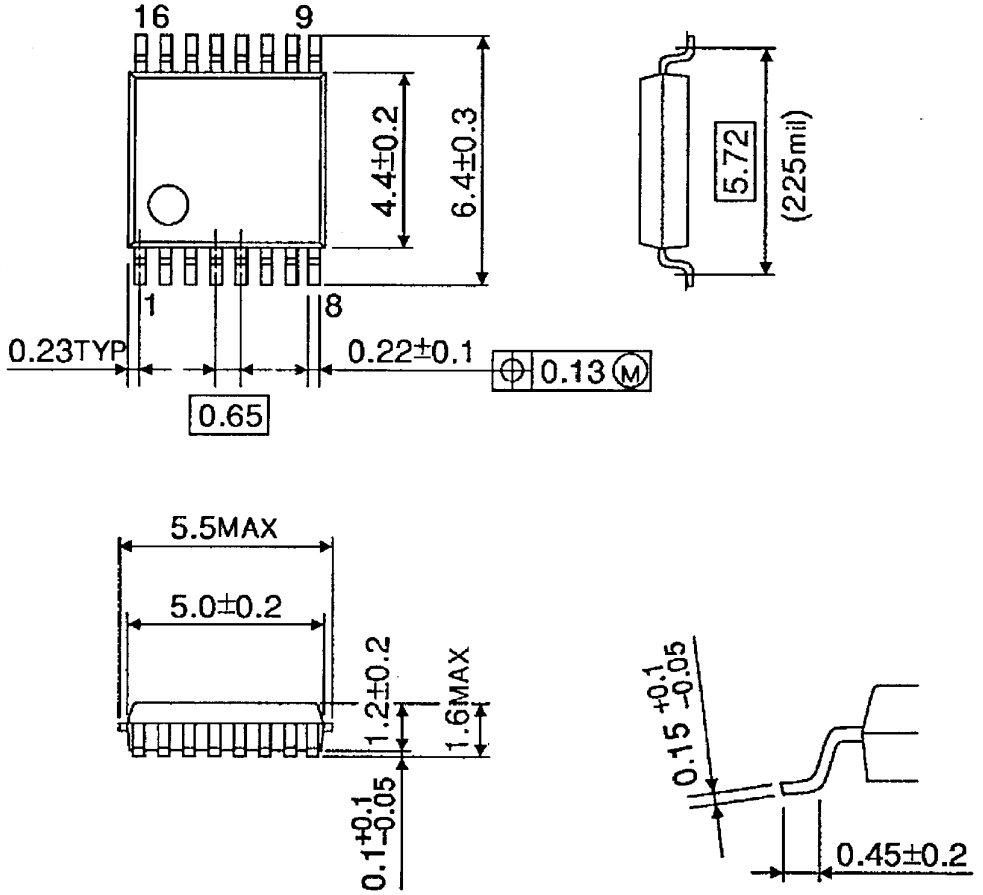
SSOP16-P-225-1.00A Unit : mm



Weight: 0.14 g (Typ.)

PACKAGE DIMENSIONS

SSOP16-P-225-0.65B Unit : mm



Weight: 0.07 g (Typ.)

About solderability, following conditions were confirmed

- Solderability

  (1) Use of Sn-63Pb solder Bath
  - solder bath temperature = 230°C
  - dipping time = 5 seconds
  - the number of times = once
  - use of R-type flux

  (2) Use of Sn-3.0Ag-0.5Cu solder Bath
  - solder bath temperature = 245°C
  - dipping time = 5 seconds
  - the number of times = once
  - use of R-type flux

RESTRICTIONS ON PRODUCT USE

030619EBA

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