# 512Mb DDR2 SDRAM

## Features

### CAS Latency and Frequency

| Speed Sorts | -5A DDR2 -400 | -37B DDR2 -533 | -3C DDR2 -667 | Units |
|---|---|---|---|---|
| Bin (CL-tRCD-TRP) | 3-3-3 | 4-4-4 | 5-5-5 | tck |
| max. Clock Frequency | 200 | 266 | 333 | MHz |
| Data Rate | 400 | 533 | 667 | Mb/s/pin |
| $\overline{CAS}$ Latency | 3 | 4 | 5 | tck |
| $t_{RCD}$ | 15 | 15 | 15 | ns |
| $t_{RP}$ | 15 | 15 | 15 | ns |
| $t_{RC}$ | 55 | 60 | 60 | ns |

- 1.8V ± 0.1V Power Supply Voltage
- 4 internal memory banks
- Programmable CAS Latency: 3, 4 and 5
- Programmable Additive Latency: 0, 1, 2, 3 and 4
- Write Latency = Read Latency -1
- Programmable Burst Length: 4 and 8
- Programmable Sequential / Interleave Burst
- OCD (Off-Chip Driver Impedance Adjustment)
- ODT (On-Die Termination)
- 4 bit prefetch architecture
- 1KB page size for x 4 & x 8,
  2KB page size for x16
- Data-Strobes: Bidirectional, Differential
- Strong and Weak Strength Data-Output Driver
- Auto-Refresh and Self-Refresh
- Power Saving Power-Down modes
- 7.8 µs max. Average Periodic Refresh Interval
- Packages:
  60 pin BGA for x4/x8 components
  84 pin BGA for x8/x16 components

## Description

The 512Mb Double-Data-Rate-2 (DDR2) DRAMs is a high-speed CMOS Double Data Rate 2 SDRAM containing 536,870,912 bits. It is internally configured as a quad-bank DRAM.

The 512Mb chip is organized as either 32Mbit x 4 I/O x 4 bank, 16Mbit x 8 I/O x 4 bank or 8Mbit x 16 I/O x 4 bank device. These synchronous devices achieve high speed double-data-rate transfer rates of up to 533 Mb/sec/pin for general applications.

The chip is designed to comply with all key DDR2 DRAM key features: (1) posted CAS with additive latency, (2) write latency = read latency -1, (3) normal and weak strength data-output driver, (4) variable data-output impedance adjustment and (5) an ODT (On-Die Termination) function.

All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and $\overline{CK}$ falling). All I/Os are synchronized with a single ended DQS or differential DQS pair in a source synchronous fashion. A 16 bit address bus for x4 and x8 organised components and a 15 bit address bus for x16 components is used to convey row, column, and bank address devices.

These devices operate with a single 1.8V +/-0.1V power supply and are available in BGA packages.

An Auto-Refresh and Self-Refresh mode is provided along with various power-saving power-down modes.

## Pin Configuration - 60 balls 0.8mmx0.8mm Pitch BGA Package (x4/x8)

<Top View >

See the balls through the package.

x 4

| 1 | 2 | 3 | | 7 | 8 | 9 |
|---|---|---|---|---|---|---|
| VDD | NC | VSS | A | VSSQ | $\overline{DQS}$ | VDDQ |
| NC | VSSQ | DM | B | DQS | VSSQ | NC |
| VDDQ | DQ1 | VDDQ | C | VDDQ | DQ0 | VDDQ |
| NC | VSSQ | DQ3 | D | DQ2 | VSSQ | NC |
| VDDL | VREF | VSS | E | VSSDL | CK | VDD |
| | CKE | $\overline{WE}$ | F | $\overline{RAS}$ | $\overline{CK}$ | ODT |
| NC | BA0 | BA1 | G | $\overline{CAS}$ | $\overline{CS}$ | |
| | A10/AP | A1 | H | A2 | A0 | VDD |
| VSS | A3 | A5 | J | A6 | A4 | |
| | A7 | A9 | K | A11 | A8 | VSS |
| VDD | A12 | NC | L | NC | A13 | |

x 8

| 1 | 2 | 3 | | 7 | 8 | 9 |
|---|---|---|---|---|---|---|
| VDD | NU/$\overline{RDQS}$ | VSS | A | VSSQ | $\overline{DQS}$ | VDDQ |
| DQ6 | VSSQ | DM/RDQS | B | DQS | VSSQ | DQ7 |
| VDDQ | DQ1 | VDDQ | C | VDDQ | DQ0 | VDDQ |
| DQ4 | VSSQ | DQ3 | D | DQ2 | VSSQ | DQ5 |
| VDDL | VREF | VSS | E | VSSDL | CK | VDD |
| | CKE | $\overline{WE}$ | F | $\overline{RAS}$ | $\overline{CK}$ | ODT |
| BA2 | BA0 | BA1 | G | $\overline{CAS}$ | $\overline{CS}$ | |
| | A10/AP | A1 | H | A2 | A0 | VDD |
| VSS | A3 | A5 | J | A6 | A4 | |
| | A7 | A9 | K | A11 | A8 | VSS |
| VDD | A12 | NC | L | NC | A13 | |

## Pin Configuration - 84 balls 0.8mmx0.8mm Pitch BGA Package (x16)

<Top View >

See the balls through the package.

x 16

| 1 | 2 | 3 | | 7 | 8 | 9 |
|---|---|---|---|---|---|---|
| VDD | NC | VSS | A | VSSQ | $\overline{\text{UDQS}}$ | VDDQ |
| DQ14 | VSSQ | UDM | B | UDQS | VSSQ | DQ15 |
| VDDQ | DQ9 | VDDQ | C | VDDQ | DQ8 | VDDQ |
| DQ12 | VSSQ | DQ11 | D | DQ10 | VSSQ | DQ13 |
| VDD | NC | VSS | E | VSSQ | $\overline{\text{LDQS}}$ | VDDQ |
| DQ6 | VSSQ | LDM | F | LDQS | VSSQ | DQ7 |
| VDDQ | DQ1 | VDDQ | G | VDDQ | DQ 0 | VDDQ |
| DQ4 | VSSQ | DQ3 | H | DQ2 | VSSQ | DQ5 |
| VDDL | VREF | VSS | J | VSSDL | CK | VDD |
| | CKE | $\overline{\text{WE}}$ | K | $\overline{\text{RAS}}$ | $\overline{\text{CK}}$ | ODT |
| NC | BA0 | BA1 | L | $\overline{\text{CAS}}$ | $\overline{\text{CS}}$ | |
| | A10/AP | A1 | M | A2 | A0 | VDD |
| VSS | A3 | A5 | N | A6 | A4 | |
| | A7 | A9 | P | A11 | A8 | VSS |
| VDD | A12 | NC | R | NC | NC | |

## Input/Output Functional Description

| Symbol | Type | Function |
|---|---|---|
| CK, $\overline{CK}$ | Input | **Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing). |
| CKE | Input | **Clock Enable:** CKE high activates and CKE low deactivates internal clock signals and device input buffers and output drivers. Taking CKE low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit and for Self-Refresh entry. CKE is asynchronous for Self-Refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during Power Down. Input buffers, excluding CKE are disabled during Self-Refresh. |
| $\overline{CS}$ | Input | **Chip Select:** All command are masked when $\overline{CS}$ is registered high. $\overline{CS}$ provides for external rank selection on systems with multiple memory ranks. $\overline{CS}$ is considered part of the command code. |
| $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | Input | **Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered. |
| DM, LDM, UDM | Input | **Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled high coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. LDM and UDM are the input mask signals for x16 components and control the lower or upper bytes. For x8 components the data mask function is disabled, when RDQS / $\overline{RDQS}$ are enabled by EMRS(1) command. |
| BA0, BA1 | Input | **Bank Address Inputs:** BA0 and BA1 define to which bank an Active, Read, Write or Precharge command is being applied. BA0 and BA1 also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle. |
| A0 - A13 | Input | **Address Inputs:** Provides the row address for Activate commands and the column address and Auto-Precharge bit A10 (=AP) for Read/Write commands to select one location out of the memory array in the respective bank. A10 (=AP) is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10=low) or all banks (A10=high). If only one bank is to be precharged, the bank is selected by BA0 and BA1. The address inputs also provide the op-code during Mode Register Set commands.<br>Row address A13 is used on x4 and x8 components only. |
| DQ | Input/Output | **Data Inputs/Output:** Bi-directional data bus. |
| DQS, ($\overline{DQS}$)<br>LDQS, ($\overline{LDQS}$),<br>UDQS,($\overline{UDQS}$) | Input/Output | **Data Strobe:** output with read data, input with write data. Edge aligned with read data, centered with write data. For the x16, LDQS corresponds to the data on LDQ0 - LDQ7; UDQS corresponds to the data on UDQ0-UDQ7. The data strobes DQS, LDQS, UDQS may be used in single ended mode or paired with the optional complementary signals $\overline{DQS}$, $\overline{LDQS}$, $\overline{UDQS}$ to provide differential pair signaling to the system during both reads and writes. An EMRS(1) control bit enables or disables the complementary data strobe signals. |
| RDQS, ($\overline{RDQS}$) | Input/Output | **Read Data Strobe:** For the x8 components a RDQS, $\overline{RDQS}$ pair can be enabled via the EMRS(1) for read timing. RDQS, $\overline{RDQS}$ is not supported on x4 and x16 components. RDQS, $\overline{RDQS}$ are edge-aligned with read data. If RDQS, $\overline{RDQS}$ is enabled, the DM function is disabled on x8 components. |
| ODT | Input | **On Die Termination:** ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is applied to each DQ, DQS, $\overline{DQS}$ and DM signal for x4 and DQ, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$ and DM for x8 configurations. For x16 configuration ODT is applied to each DQ, UDQS, $\overline{UDQS}$, LDQS, $\overline{LDQS}$, UDM and LDM signal. The ODT pin will be ignored if the EMRS(1) is programmed to disable ODT. |
| NC | | **No Connect:** No internal electrical connection is present. |
| $V_{DDQ}$ | Supply | **DQ Power Supply:** 1.8V +/- 0.1V |
| $V_{SSQ}$ | Supply | **DQ Ground** |
| $V_{DDL}$ | Supply | **DLL Power Supply:** 1.8V +/- 0.1V |
| $V_{SSDL}$ | Supply | **DLL Ground** |
| $V_{DD}$ | Supply | **Power Supply:** 1.8V +/- 0.1V |
| $V_{SS}$ | Supply | **Ground** |
| $V_{REF}$ | Supply | **SSTL_1.8 reference voltage** |

## Ordering Information

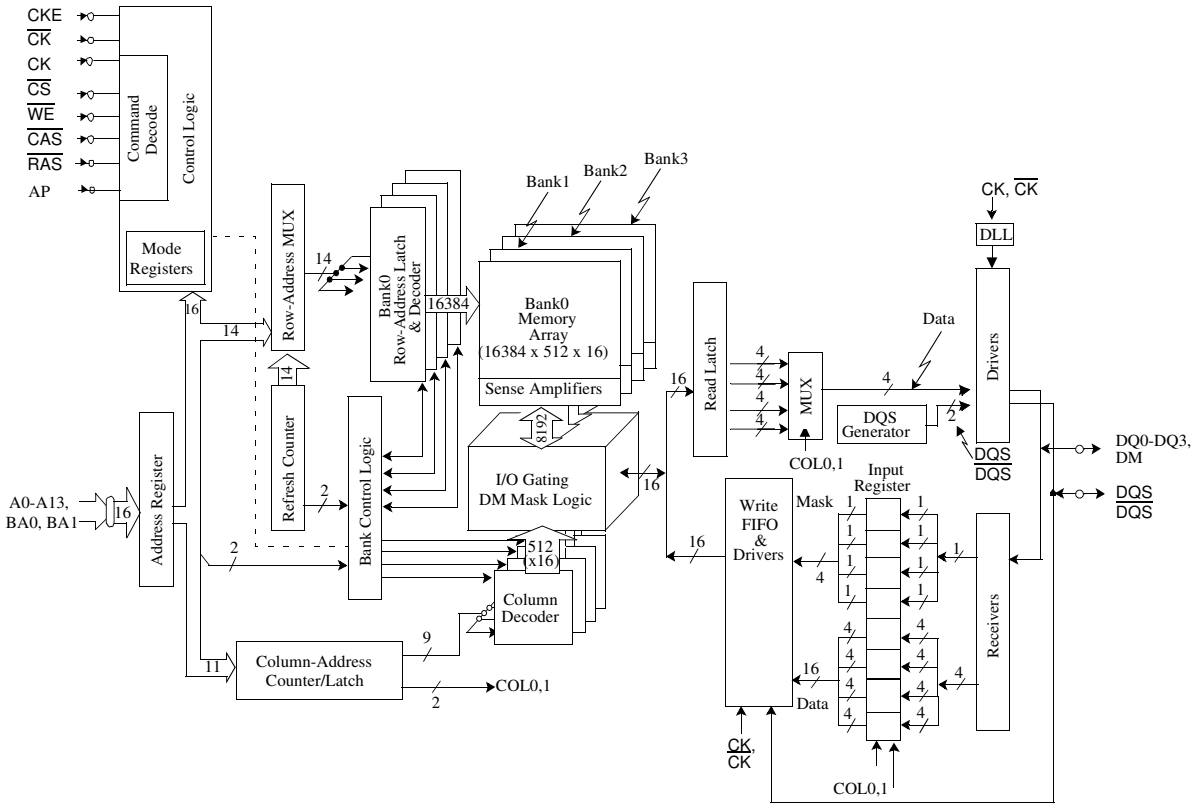
### Leaded

| Org. | Part Number | Package | Speed | |
|---|---|---|---|---|
| | | | Clock (MHz) | CL-$t_{RCD}$-$t_{RP}$ |
| 128M x 4 | NT5TU128M4AB-5A | 60ball BGA 0.8mmx0.8mm Pitch | 200 | 3-3-3 |
| | NT5TU128M4AB-37B | | 266 | 4-4-4 |
| | NT5TU128M4AB-3C | | 333 | 5-5-5 |
| 64M x 8 | NT5TU64M8AB-5A | 60ball BGA 0.8mmx0.8mm Pitch | 200 | 3-3-3 |
| | NT5TU64M8AB-37B | | 266 | 4-4-4 |
| | NT5TU64M8AB-3C | | 333 | 5-5-5 |
| | NT5TU64M8AF-5A | 84ball BGA 0.8mmx0.8mm Pitch | 200 | 3-3-3 |
| | NT5TU64M8AF-37B | | 266 | 4-4-4 |
| | NT5TU64M8AF-3C | | 333 | 5-5-5 |
| 32M x 16 | NT5TU32M16AF-5A | 84ball BGA 0.8mmx0.8mm Pitch | 200 | 3-3-3 |
| | NT5TU32M16AF-37B | | 266 | 4-4-4 |
| | NT5TU32M16AF-3C | | 333 | 5-5-5 |
| Note: | | | | |

### Green

| Org. | Part Number | Package | Speed | |
|---|---|---|---|---|
| | | | Clock (MHz) | CL-$t_{RCD}$-$t_{RP}$ |
| 128M x 4 | NT5TU128M4AE-5A | 60ball BGA 0.8mmx0.8mm Pitch | 200 | 3-3-3 |
| | NT5TU128M4AE-37B | | 266 | 4-4-4 |
| | NT5TU128M4AE-3C | | 333 | 5-5-5 |
| 64M x 8 | NT5TU64M8AE-5A | 60ball BGA 0.8mmx0.8mm Pitch | 200 | 3-3-3 |
| | NT5TU64M8AE-37B | | 266 | 4-4-4 |
| | NT5TU64M8AE-3C | | 333 | 5-5-5 |
| 32M x 16 | NT5TU32M16AG-5A | 84ball BGA 0.8mmx0.8mm Pitch | 200 | 3-3-3 |
| | NT5TU32M16AG-37B | | 266 | 4-4-4 |
| | NT5TU32M16AG-3C | | 333 | 5-5-5 |
| Note: | | | | |

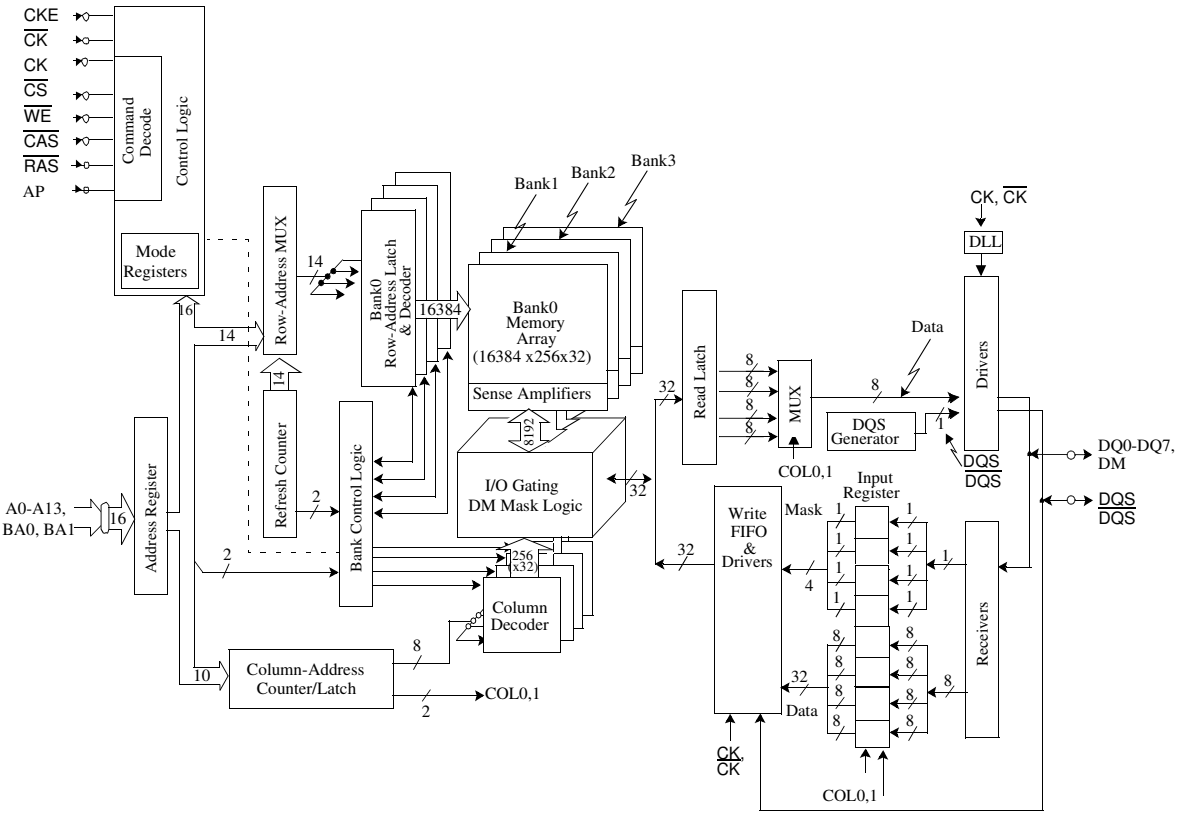
## Block Diagram (128Mb x 4)




**Note:** This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

**Note:** DM is a unidirectional signal (input only), but is internally loaded to match the load of the bidirectional DQ and DQS signals.

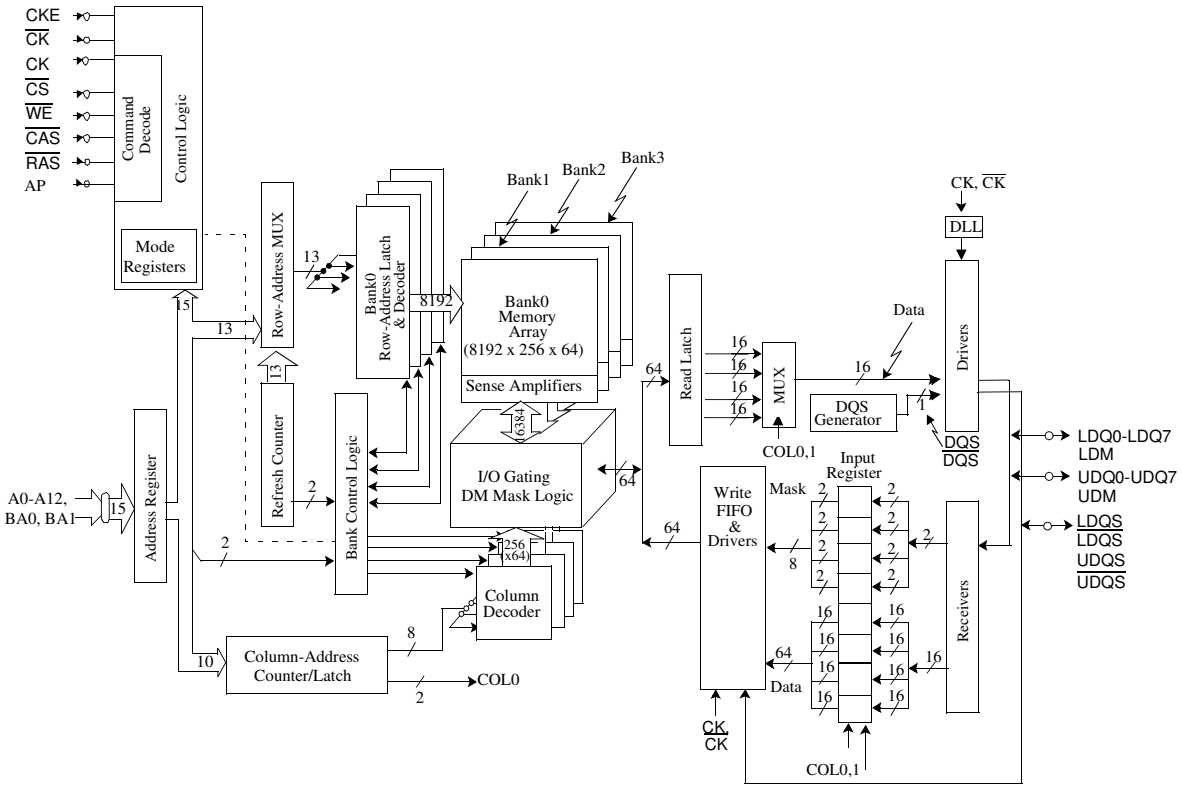
## Block Diagram (64Mb x 8)




**Note:** This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

**Note:** DM is a unidirectional signal (input only), but is internally loaded to match the load of the bidirectional DQ and DQS signals.

## Block Diagram (32Mb x 16)




**Note:** This Functional Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

**Note:** DM is a unidirectional signal (input only), but is internally loaded to match the load of the bidirectional DQ and DQS signals.

## Functional Description

The 512Mb DDR2 SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. The 512Mb DDR SDRAM is internally configured as a quad-bank DRAM.

The 512Mb DDR2 SDRAM uses a double-data-rate architecture to achieve high-speed operation. The double-data-rate architecture is essentially a *4n* prefetch architecture, with an interface designed to transfer four data words per clock cycle at the I/O pins. A single read or write access for the 512Mb DDR SDRAM consists of a single *4n*-bit wide, one clock cycle data transfer at the internal DRAM core and four corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write accesses to the DDR2 SDRAM are burst oriented; accesses start at a selected location and continue for the burst length of four or eight in a programmed sequence. Accesses begin with the registration of an Activate command, which is followed by a Read or Write command. The address bits registered coincident with the activate command are used to select the bank and row to be accesses (BA0 & BA1 select the banks, A0-A13 select the row for x4 and x8 components, A0~A12 select the row for x16 components). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst access and to determine if the Auto-Precharge command is to be issued.

Prior to normal operation, the DDR2 SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command description and device operation.

## Initialization

DDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

The following sequence is required for POWER UP and Initialization.

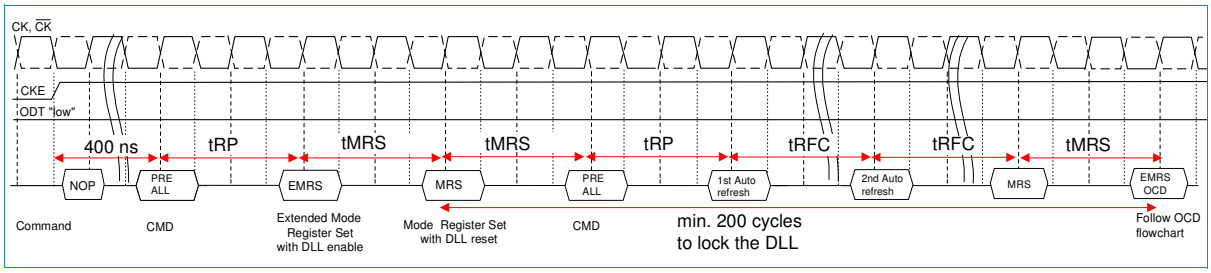
1. Apply power and attempt to maintain CKE below 0.2 * VDDQ and ODT* at a low state (all other inputs may be undefined). The power voltage ramp time must be no greater than 20mS; and during the ramp, VDD>VDDL>VDDQ and VDD-VDDQ<0.3 volts.

   - VDD,VDDL and VDDQ are driven from a signle power converter output, AND
   - VTT is limited to 0.95 V max, AND
   - VREF tracks VDDQ/2
     or
   - Apply VDD without any slope reversal before or at the same time as VDDL.
   - Apply VDDL without any slope reversal before or at the same time as VDDQ.
   - Apply VDDQ without any slope reversal before or at the same time as VTT & VREF.
     at least one of these two sets of conditions must be met.

2. Start clock (CK, $\overline{CK}$) and maintain stable condition.
3. For the minimum of 200uS after stable power and clock, then apply NOP or deselect & take CKE high.
4. Wait minimum of 400ns, then issue a Precharge-all command. NOP or deselect applied during 400ns period.
5. Issue EMRS(2) command. (To issue EMRS(2) command, provide “low” to BA0 and BA2 and “high” to BA1)
6. Issue EMRS(3) command. (To issue EMRS(3) command, provide “low” to BA2 and “high” to BA0 and BA1)
7. Issue EMRS command to enable DLL. (To issue “DLL Enable” command, provide “low” to A0 and “high” to BA0 and “low” to BA1 ~ BA2 and A13)
8. Issue MRS command (Mode Register Set) for "DLL reset". (To issue DLL reset command, provide “high” to A8 and “low” to BA0 ~ BA2 and A13)
9. Issue Precharge-All command.
10. Issue 2 or more Auto-Refresh commands.
11. Issue a MRS command with low on A8 to initialize device operation. (i.e. to programm operating paramters without resetting the DLL.)
12. At least 200 clocks after step 8, execute OCD Calibration (Off Chip Driver impedance adjustment). If OCD calibration is not used, EMRS OCD Default command (A9=A8=A7=1) followed by EMRS OCD Calibration Mode Exit command (A9=A8=A7=0) must be issued with other parameters of EMRS.
13. The DDR2 SDRAM is now read for normal operation.

* To guarantee ODT off, VREF must be valid and a low level must be applied to the ODT pin 13.

## Example




## Register Definition

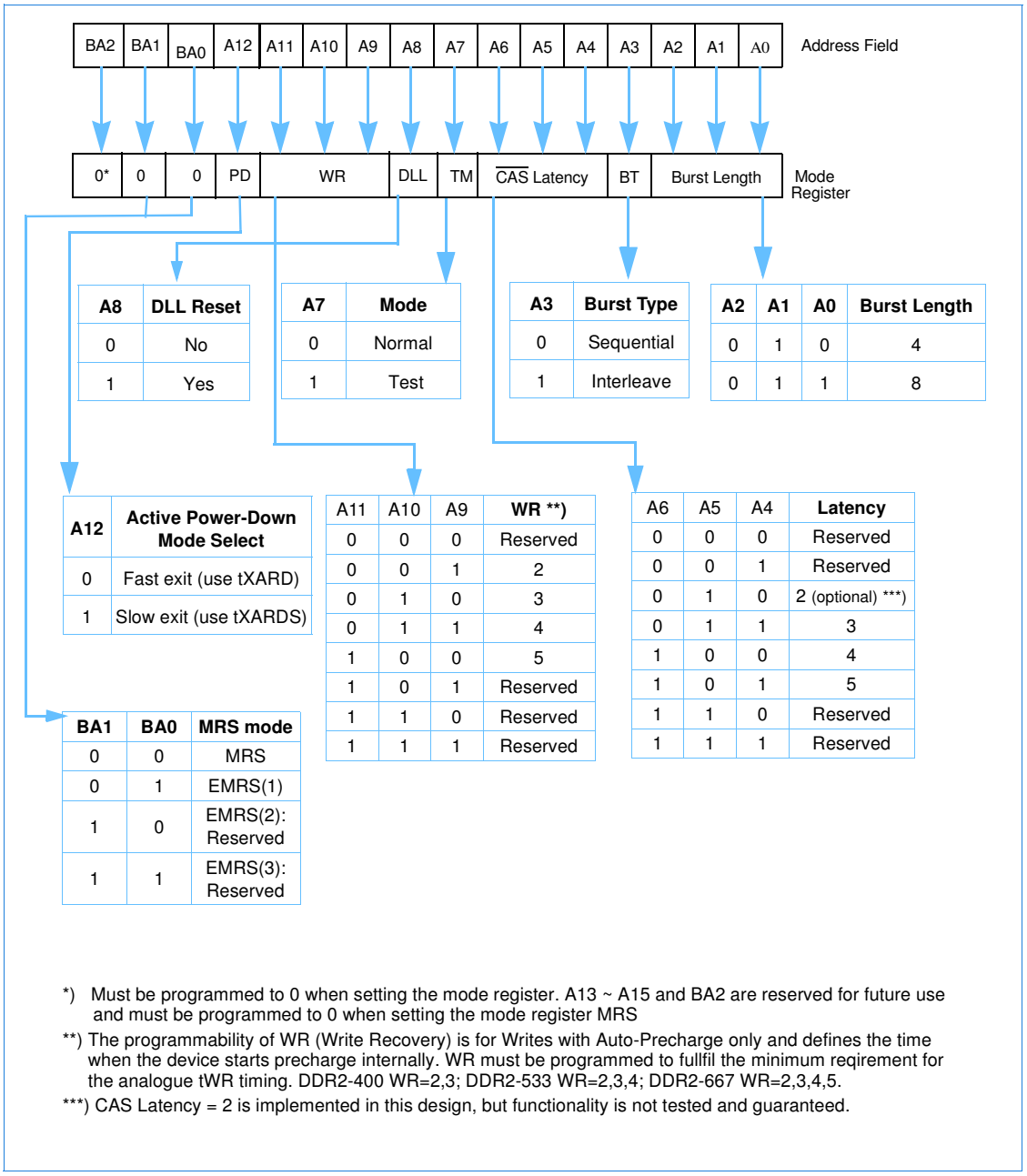
### Programming the Mode Register and Extended Mode Registers

For application flexibility, burst length, burst type, $\overline{CAS}$ latency, DLL reset function, write recovery time (tWR) are user defined variables and must be programmed with a Mode Register Set (MRS) command. Additionally, DLL disable function, additive $\overline{CAS}$ latency, driver impedance, ODT (On Die Termination), single-ended strobe and OCD (off chip driver impedance adjustment) are also user defined variables and must be programmed with an Extended Mode Register Set (EMRS) command. Contents of the Mode Register (MR) and Extended Node Registers (EMRS(#)) can be altered by re-executing the MRS and EMRS Commands. If the user chooses to modify only a subset of the MRS or EMRS variables, all variables must be redefined when the MRS or EMRS commands are issued. MRS, EMRS and DLL Reset do not affect array contents, which means reinitialization including those can be executed any time after power-up without affecting array contents.

### Mode Register Set (MRS)

The mode register stores the data for controlling the various operating modes of DDR2 SDRAM. It programs $\overline{CAS}$ latency, burst length, burst sequence, test mode, DLL reset, tWR (write recovery) and various vendor specific options to make DDR2 SDRAM useful for various applications. The default value of the mode register is not defined, therefore the mode register must be written after power-up for proper operation. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA0 and BA1, while controlling the state of address pins A0 ~ A13. The DDR2 SDRAM should be in all bank precharged with CKE already high prior to writing into the mode register. The mode register set command cycle time ($t_{MRD}$) is required to complete the write operation to the mode register. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharged state. The mode register is divided into various fields depending on functionality. Burst length is defined by A0 ~ A2 with options of 4 and 8 bit burst length. Burst address sequence type is defined by A3 and $\overline{CAS}$ latency is defined by A4 ~ A6. A7 is used for test mode and must be set to low for normal MRS operation. A8 is used for DLL reset. A9 ~ A11 are used for write recovery time (tWR) definition for Auto-Precharge mode. With address bit A12 two Power-Down modes can be selected, a “standard mode” and a “low-power” Power-Down mode, where the DLL is disabled. Addess bit A13 and all “higher” address bits (including BA2) have to be set to “low” for compatibility with other DDR2 memory products with higher memory densities.

## MRS Mode Register Operation Table (Address Input For Mode Set)




| A8 | DLL Reset |
|---|---|
| 0 | No |
| 1 | Yes |

| A7 | Mode |
|---|---|
| 0 | Normal |
| 1 | Test |

| A3 | Burst Type |
|---|---|
| 0 | Sequential |
| 1 | Interleave |

| A2 | A1 | A0 | Burst Length |
|---|---|---|---|
| 0 | 1 | 0 | 4 |
| 0 | 1 | 1 | 8 |

| A12 | Active Power-Down Mode Select |
|---|---|
| 0 | Fast exit (use tXARD) |
| 1 | Slow exit (use tXARDS) |

| A11 | A10 | A9 | WR **) |
|---|---|---|---|
| 0 | 0 | 0 | Reserved |
| 0 | 0 | 1 | 2 |
| 0 | 1 | 0 | 3 |
| 0 | 1 | 1 | 4 |
| 1 | 0 | 0 | 5 |
| 1 | 0 | 1 | Reserved |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |

| A6 | A5 | A4 | Latency |
|---|---|---|---|
| 0 | 0 | 0 | Reserved |
| 0 | 0 | 1 | Reserved |
| 0 | 1 | 0 | 2 (optional) ***) |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 5 |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |

| BA1 | BA0 | MRS mode |
|---|---|---|
| 0 | 0 | MRS |
| 0 | 1 | EMRS(1) |
| 1 | 0 | EMRS(2): Reserved |
| 1 | 1 | EMRS(3): Reserved |

*) Must be programmed to 0 when setting the mode register. A13 ~ A15 and BA2 are reserved for future use and must be programmed to 0 when setting the mode register MRS

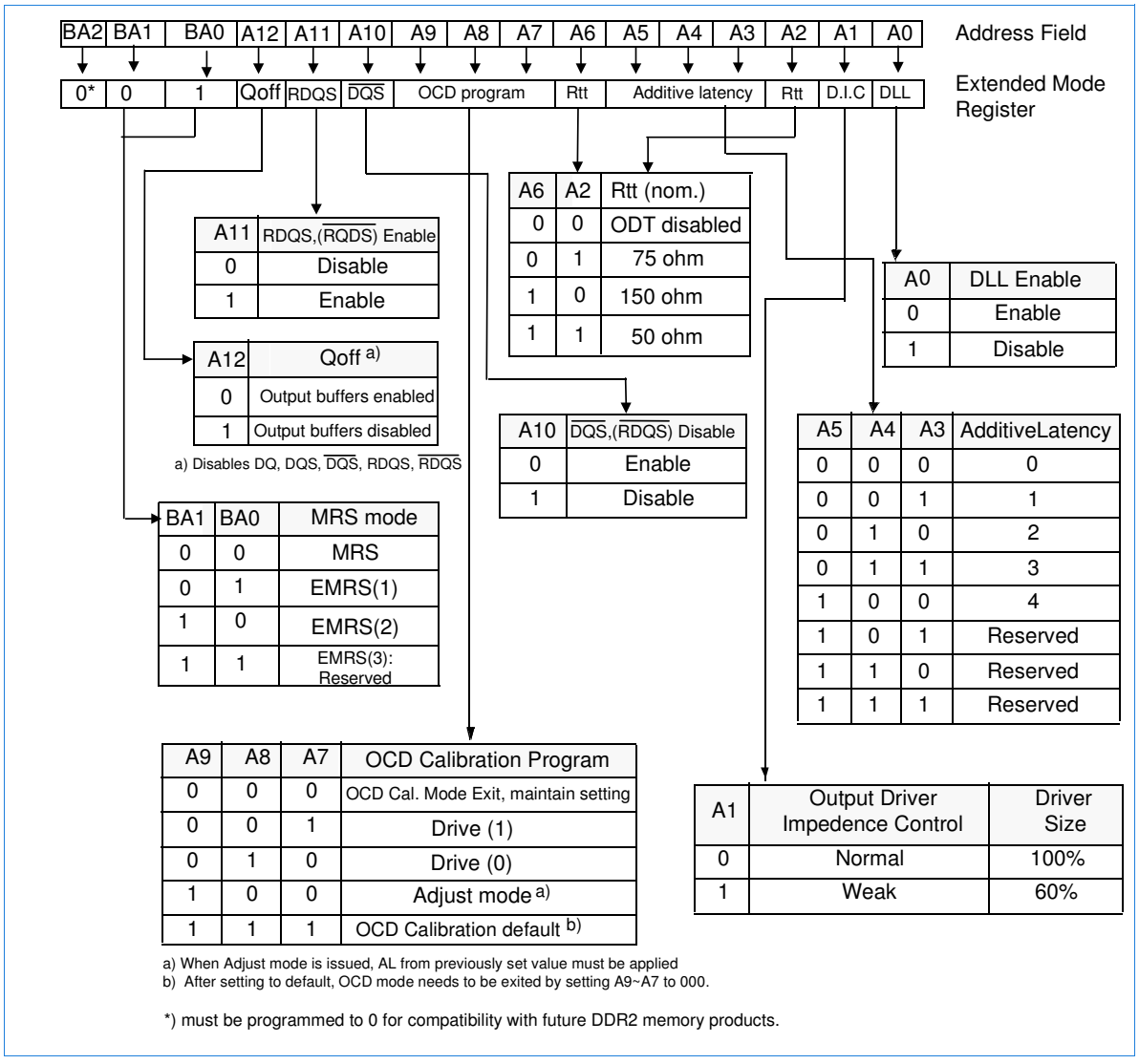
**) The programmability of WR (Write Recovery) is for Writes with Auto-Precharge only and defines the time when the device starts precharge internally. WR must be programmed to fullfil the minimum reqirement for the analogue tWR timing. DDR2-400 WR=2,3; DDR2-533 WR=2,3,4; DDR2-667 WR=2,3,4,5.

***) CAS Latency = 2 is implemented in this design, but functionality is not tested and guaranteed.

## Extended Mode Register Set (EMRS(1))

The extended mode register EMRS(1) stores the data for enabling or disabling the DLL, output driver strength, additive latency, OCD program, ODT, $\overline{DQS}$ disable, RQDS and $\overline{RDQS}$ enable. The default value of the extended mode register EMRS(1) is not defined, therefore the extended mode register must be written after power-up for proper operation. The extended mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA1 and high on BA0, while controlling the state of the address pins. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register(1). The mode register set command cycle time (tMRD) must be satisfied to complete the write operation to the EMRS(1). Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in precharge state.

### EMRS(1) Extended Mode Register Operation Table (Address Input For Mode Set)




| A11 | RDQS,(RDQS) Enable |
|---|---|
| 0 | Disable |
| 1 | Enable |

| A12 | Qoff a) |
|---|---|
| 0 | Output buffers enabled |
| 1 | Output buffers disabled |

a) Disables DQ, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$

| A6 | A2 | Rtt (nom.) |
|---|---|---|
| 0 | 0 | ODT disabled |
| 0 | 1 | 75 ohm |
| 1 | 0 | 150 ohm |
| 1 | 1 | 50 ohm |

| A10 | DQS,(RDQS) Disable |
|---|---|
| 0 | Enable |
| 1 | Disable |

| A0 | DLL Enable |
|---|---|
| 0 | Enable |
| 1 | Disable |

| A5 | A4 | A3 | AdditiveLatency |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | Reserved |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |

| BA1 | BA0 | MRS mode |
|---|---|---|
| 0 | 0 | MRS |
| 0 | 1 | EMRS(1) |
| 1 | 0 | EMRS(2) |
| 1 | 1 | EMRS(3): Reserved |

| A9 | A8 | A7 | OCD Calibration Program |
|---|---|---|---|
| 0 | 0 | 0 | OCD Cal. Mode Exit, maintain setting |
| 0 | 0 | 1 | Drive (1) |
| 0 | 1 | 0 | Drive (0) |
| 1 | 0 | 0 | Adjust mode a) |
| 1 | 1 | 1 | OCD Calibration default b) |

| A1 | Output Driver Impedence Control | Driver Size |
|---|---|---|
| 0 | Normal | 100% |
| 1 | Weak | 60% |

a) When Adjust mode is issued, AL from previously set value must be applied
b) After setting to default, OCD mode needs to be exited by setting A9~A7 to 000.

*) must be programmed to 0 for compatibility with future DDR2 memory products.

A0 is used for DLL enable or disable. A1 is used for enabling half-strength data-output driver. A2 and A6 enables ODT (On-Die termination) and sets the Rtt value. A3~A5 are used for additive latency settings and A7 ~ A9 enables the OCD impedance adjustment mode. A10 enables or disables the differential $\overline{DQS}$ and $\overline{RDQS}$ signals, A11 disables or enables RDQS. Address bit A12 have to be set to "low" for normal operation. With A12 set to "high" the SDRAM outputs are disabled and in Hi-Z. "High" on BA0 and "low" for BA1 have to be set to access the EMRS(1). A13 and all "higher" address bits (including BA2) have to be set to "low" for compatibility with other DDR2 memory products with higher memory densities. Refer to the table for specific codes on the previous page.

### Single-ended and Differential Data Strobe Signals

The following table lists all possible combinations for DQS, $\overline{DQS}$, RDQS, $\overline{RQDS}$ which can be programmed by A10 & A11 address bits in EMRS. RDQS and $\overline{RDQS}$ are available in x8 components only. If RDQS is enabled in x8 components, the DM function is disabled. RDQS is active for reads and don't care for writes :

| EMRS | | Stobe Function Matrix | | | | Signaling |
|---|---|---|---|---|---|---|
| A11 (RDQS Enable) | A10 ($\overline{DQS}$ Enable) | RDQS/DM | $\overline{RDQS}$ | DQS | $\overline{DQS}$ | |
| 0 (Disable) | 0 (Enable) | DM | Hi-Z | DQS | $\overline{DQS}$ | differential DQS signals |
| 0 (Disable) | 1 (Disable) | DM | Hi-Z | DQS | Hi-Z | single-ended DQS signals |
| 1 (Enable) | 0 (Enable) | RDQS | $\overline{RDQS}$ | DQS | $\overline{DQS}$ | differential DQS signals |
| 1 (Enable) | 1 (Disable) | RDQS | Hi-Z | DQS | Hi-Z | single-ended DQS signals |

### DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. The DLL is automatically disabled when entering Self-Refresh operation and is automatically re-enabled and reset upon exit of Self-Refresh operation. Any time the DLL is reset, 200 clock cycles must occur before a Read command can be issued to allow time for the internal clock to be synchronized with the external clock. Less clock cycles may result in a violation of the tAC or tDQSCK parameters.

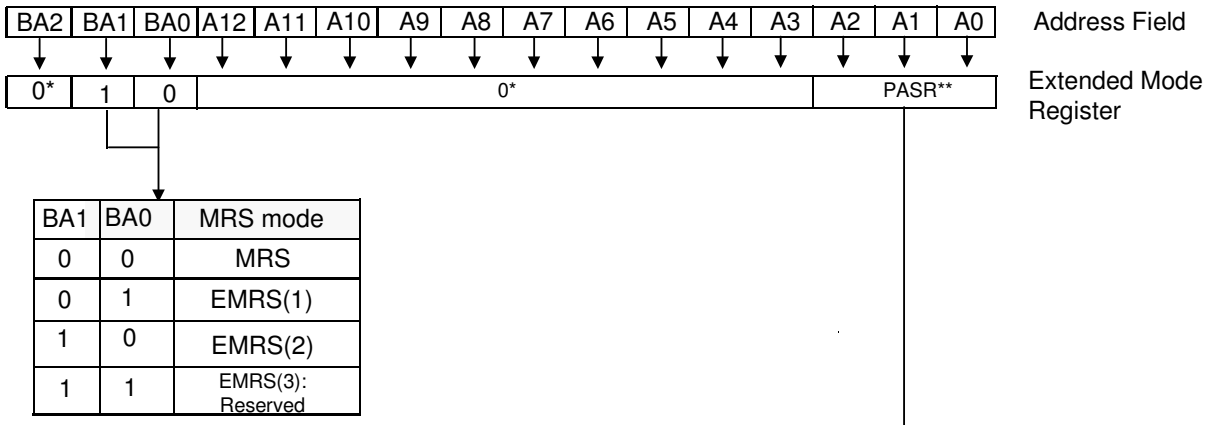
### Output Disable (Qoff)

Under normal operation, the DRAM outputs are enabled during Read operation for driving data (Qoff bit in the EMRS(1) is set to 0). When the Qoff bit is set to 1, the DRAM outputs will be disabled. Disabling the DRAM outputs allows users to measure IDD currents during Read operations, without including the output buffer current.

## EMRS(2) and EMRS(3) Extended Mode Registers

The Extended Mode Registers EMRS(2) and EMRS(3) are reserved for future use and all bits except BA0 and BA1 must be programmed to 0 when setting the mode register during initialization.

## Extended Mode Register Set (EMRS(2))



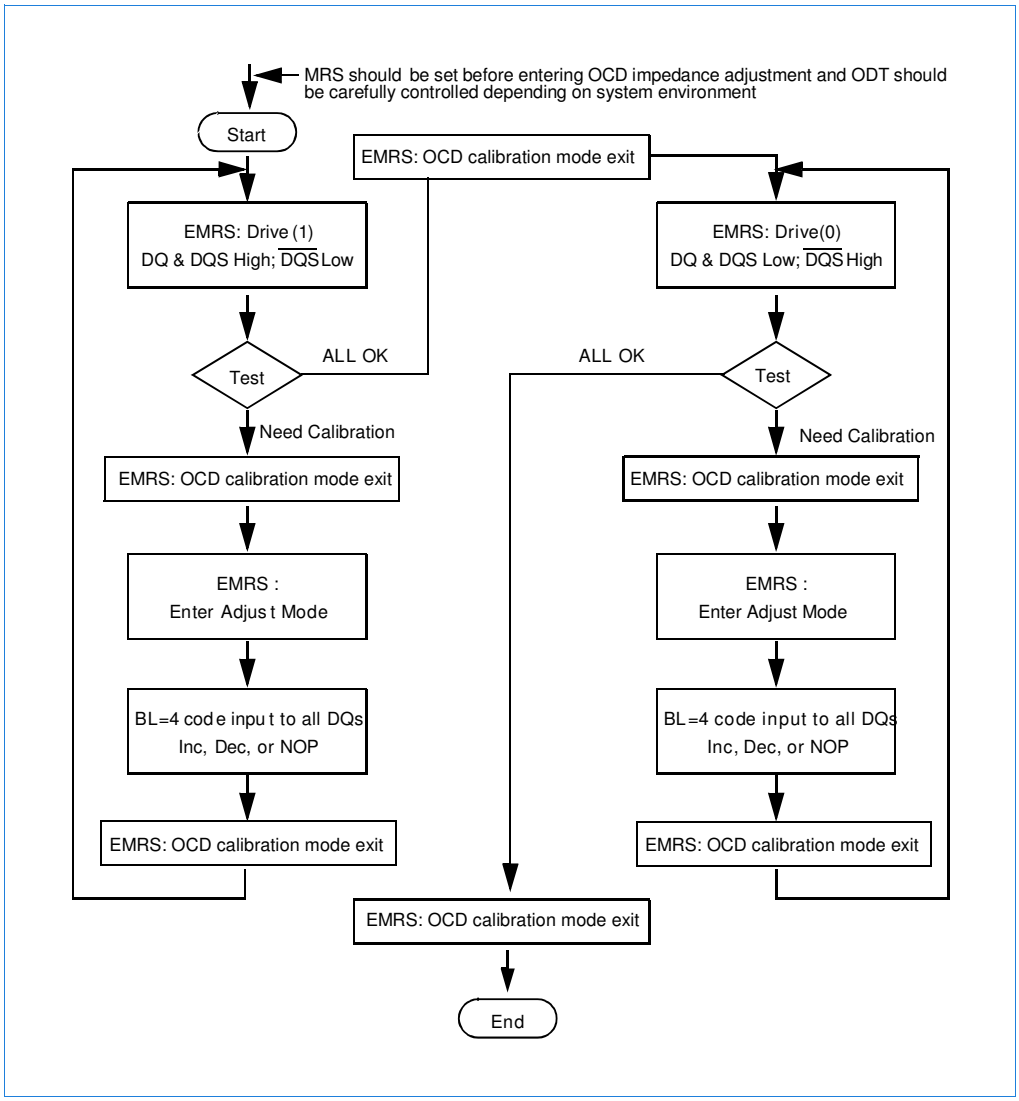

| BA1 | BA0 | MRS mode |
|---|---|---|
| 0 | 0 | MRS |
| 0 | 1 | EMRS(1) |
| 1 | 0 | EMRS(2) |
| 1 | 1 | EMRS(3): Reserved |

| A2 | A1 | A0 | Partial Array Self Refresh |
|---|---|---|---|
| 0 | 0 | 0 | Full array |
| 0 | 0 | 1 | Half Array (BA[1:0]=00&01) |
| 0 | 1 | 0 | Quarter Array (BA[1:0]=00) |
| 0 | 1 | 1 | Not defined |
| 1 | 0 | 0 | 3 / 4 array (BA[1:0]=01,10,&11) |
| 1 | 0 | 1 | Half array (BA[1:0]=10&11) |
| 1 | 1 | 0 | Quarter array (BA[1:0]=11) |
| 1 | 1 | 1 | Not defined |

* The rest bits in EMRS(2) is reserved for future use and all bits in EMRS(2) except A0-A2,BA0, and BA1 must be programmed to 0 when setting EMRS(2) during initialization.
** Optional. If PASR(Partial Array Self Refresh) is enabled, data located in areas of the array beyond the spec. location will be lost if self refresh is entered.

## Off-Chip Driver (OCD) Impedance Adjustment

DDR2 SDRAM supports driver calibration feature and the flow chart below is an example of the sequence. Every calibration mode command should be followed by “OCD calibration mode exit” before any other command being issued. MRS should be set before entering OCD impedance adjustment and ODT (On Die Termination) should be carefully controlled depending on system environment.



## Extended Mode Register Set for OCD impedance adjustment

OCD impedance adjustment can be done using the following EMRS(1) mode. In drive mode all outputs are driven out by DDR2 SDRAM and drive of RDQS is dependent on EMRS(1) bit enabling RDQS operation. In Drive(1) mode, all DQ, DQS (and RDQS) signals are driven high and all $\overline{DQS}$ (and $\overline{RDQS}$) signals are driven low. In Drive(0) mode, all DQ, DQS (and RDQS) signals are driven low and all $\overline{DQS}$ (and $\overline{RDQS}$) signals are driven high. In adjust mode, BL = 4 of operation code data must be used. In case of OCD calibration default, output driver characteristics have a nominal impedance value of 18 Ohms during nominal temperature and voltage conditions. Output driver characteristics for OCD calibration default are specified in the following table. OCD applies only to normal full strength output drive setting defined by EMRS(1) and if half strength is set, OCD default driver characteristics are not applicable. When OCD calibration adjust mode is used, OCD default output driver characteristics are not applicable. After OCD calibration is completed or driver strength is set to default, subsequent EMRS(1) commands not intended to adjust OCD characteristics must specify A7~A9 as '000' in order to maintain the default or calibrated value.

### Off- Chip-Driver program

| A9 | A8 | A7 | Operation |
|---|---|---|---|
| 0 | 0 | 0 | OCD calibration mode exit |
| 0 | 0 | 1 | Drive(1) DQ, DQS, (RDQS) high and $\overline{DQS}$, ($\overline{RDQS}$) low |
| 0 | 1 | 0 | Drive(0) DQ, DQS, (RDQS) low and $\overline{DQS}$, ($\overline{RDQS}$) high |
| 1 | 0 | 0 | Adjust mode |
| 1 | 1 | 1 | OCD calibration default |

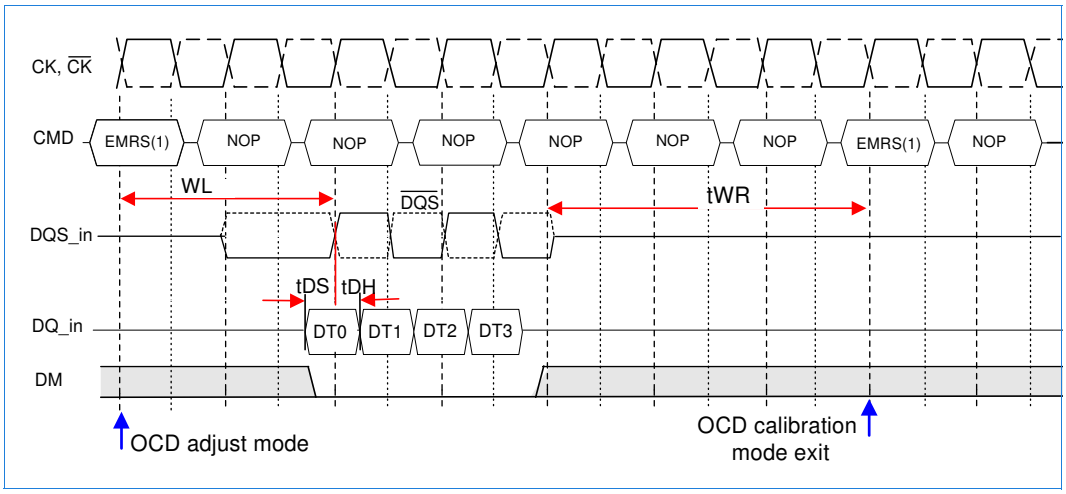
## OCD impedance adjust

To adjust output driver impedance, controllers must issue the ADJUST EMRS(1) command along with a 4 bit burst code to DDR2 SDRAM as in the following table. For this operation, Burst Length has to be set to BL = 4 via MRS command before activating OCD and controllers must drive the burst code to all DQs at the same time. DT0 is the table means all DQ bits at bit time 0, DT1 at bit time 1, and so forth. The driver output impedance is adjusted for all DDR2 SDRAM DQs simultaneously and after OCD calibration, all DQs of a given DDR2 SDRAM will be adjusted to the same driver strength setting. The maximum step count for adjustment can be up to 16 and when the limit is reached, further increment or decrement code has no effect. The default setting may be any step within the maximum step count range. When Adjust mode command is issued, AL from previously set value must be applied.

### Off- Chip-Driver Adjust Program

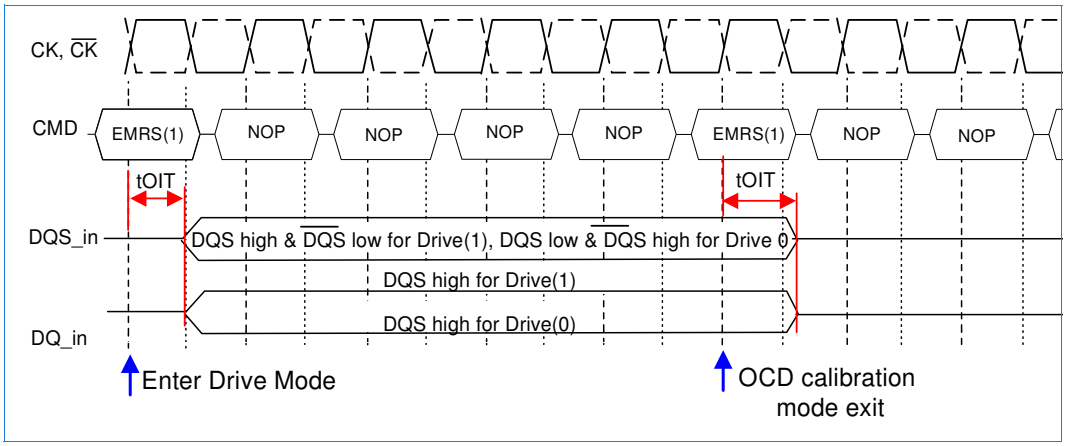
| 4 bit burst code inputs to all DQs | | | | Operation | |
|---|---|---|---|---|---|
| $D_{T0}$ | $D_{T1}$ | $D_{T2}$ | $D_{T3}$ | Pull-up driver strength | Pull-down driver strength |
| 0 | 0 | 0 | 0 | NOP (no operation) | NOP (no operation) |
| 0 | 0 | 0 | 1 | Increase by 1 step | NOP |
| 0 | 0 | 1 | 0 | Decrease by 1 step | NOP |
| 0 | 1 | 0 | 0 | NOP | Increase by 1 step |
| 1 | 0 | 0 | 0 | NOP | Decrease by 1 step |
| 0 | 1 | 0 | 1 | Increase by 1 step | Increase by 1 step |
| 0 | 1 | 1 | 0 | Decrease by 1 step | Increase by 1 step |
| 1 | 0 | 0 | 1 | Increase by 1 step | Decrease by 1 step |
| 1 | 0 | 1 | 0 | Decrease by 1 step | Decrease by 1 step |
| Other Combinations | | | | Reserved | Reserved |

For proper operation of adjust mode, WL = RL - 1 = AL + CL -1 clocks and tDS / tDH should be met as the following timing diagram. Input data pattern for adjustment, DT0 - DT3 is fixed and not affected by MRS addressing mode (i.e. sequential or interleave). Burst length of 4 have to be programmed in the MRS for OCD impedance adjustment.




## Drive Mode

Drive mode, both Drive(1) and Drive(0), is used for controllers to measure DDR2 SDRAM Driver impedance before OCD impedance adjustment. In this mode, all outputs are driven out tOIT after “enter drive mode” command and all output drivers are turned-off tOIT after “OCD calibration mode exit” command as the following timing diagram.



## On-Die Termination (ODT)

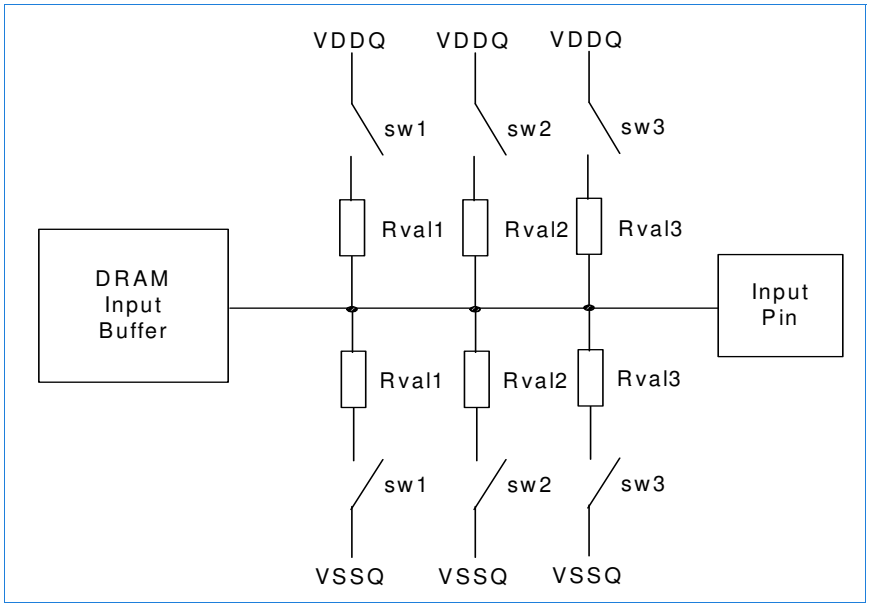
ODT (On-Die Termination) is a new feature on DDR2 components that allows a DRAM to turn on/off termination resistance for each DQ, DQS, $\overline{\text{DQS}}$ and DM for x4 and DQ, DQS, $\overline{\text{DQS}}$, DM, RDQS (DM and RDQS share the same pin), and $\overline{\text{RDQS}}$ for x8 configuration via the ODT control pin, where $\overline{\text{DQS}}$ is terminated only when enabled in the EMRS(1) by address bit A10 = 0. For x8 configuration $\overline{\text{RDQS}}$ is only terminated, when enabled in the EMRS(1) by address bits A10 = 0 and A11 = 1.

For x16 configuration ODT is applied to each DQ, DQ, UDQS, $\overline{\text{UDQS}}$, LDQS, $\overline{\text{LDQS}}$, UDM and LDM signal via the ODT control pin, where $\overline{\text{UDQS}}$ and $\overline{\text{LDQS}}$ are terminated only when enabled in the EMRS(1) by address bit A10 = 0.

The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

The ODT function can be used for all active and standby modes. ODT is turned off and not supported in Self-Refresh mode.

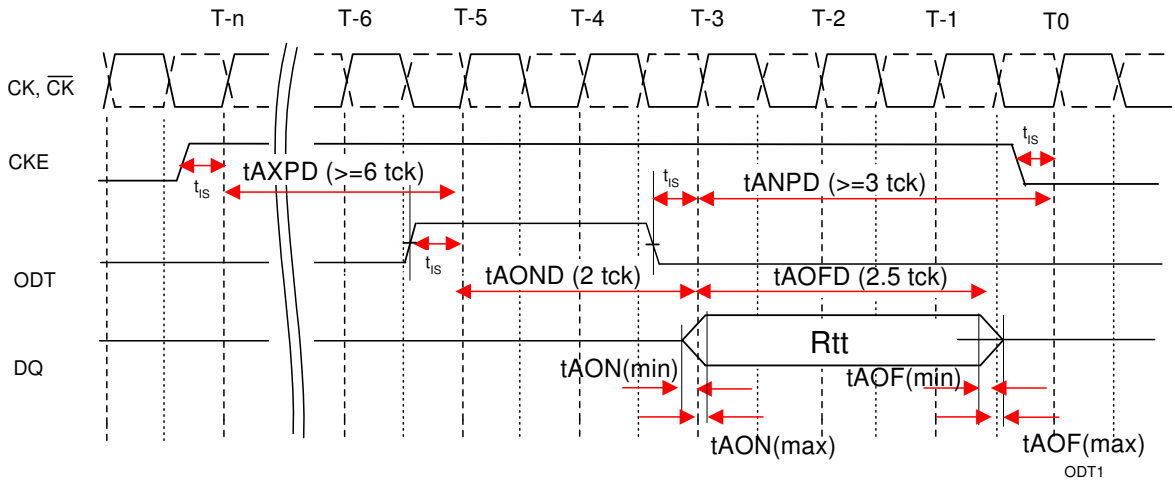
**Funtional Prepresentation of ODT**




Switch sw1, sw2 and sw3 are enabled by the ODT pin. Selection between sw1, sw2 and sw3 are determined by "Rtt (nominal)" in EMRS(1) address bits A6 & A2. Target *Rtt = 0.5 * Rval1* or *0.5 * Rval2* or *0.5 * Rval3*.

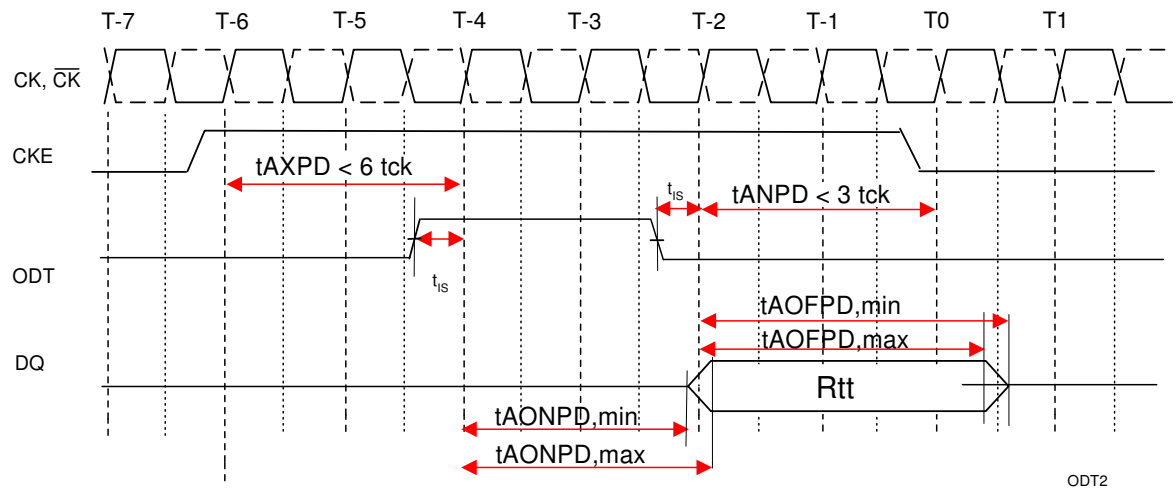
The ODT pin will be ignored if the Extended Mode Register (EMRS(1)) is programmed to disable ODT.

## ODT Timing for Active / Standby (Idle) Mode and Standard Active Power-Down Mode




1) Both ODT to Power Down Entry and Exit Latency timing parameter tANPD and tAXPD are met, therefore Non-Power Down Mode timings have to be applied.
2) ODT turn-on time ($t_{AON,min}$) is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max. ($t_{AON,max}$) is when the ODT resistance is fully on. Both are measured from $t_{AOND}$.
3) ODT turn off time min. ( $t_{AOF,min}$) is when the device starts to turn off the ODT resistance.ODT turn off time max. ($t_{AOF,max}$) is when the bus is in high impedance. Both are measured from $t_{AOFD}$.

## ODT Timing for Precharge Power-Down and Low Power Power-Down Mode

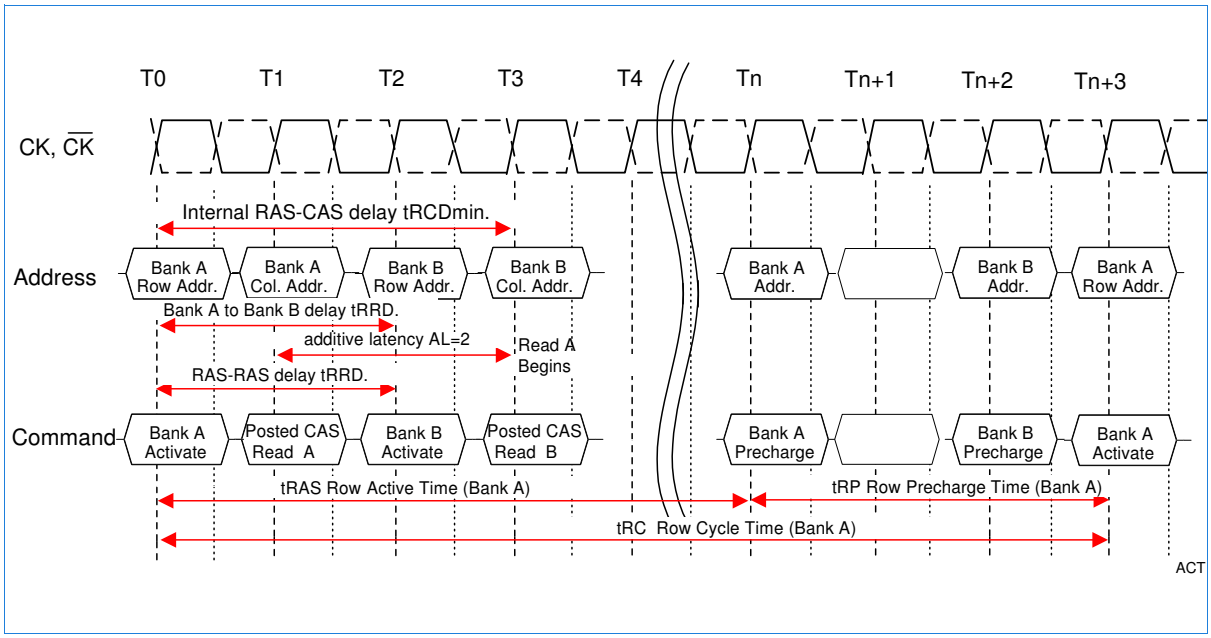



1) Both ODT to Power Down Entry and Exit Latencies tANPD and tAXPD are not met, therefore Power-Down Mode timings have to be applied.

## Bank Activate Command

The Bank Activate command is issued by holding $\overline{CAS}$ and $\overline{WE}$ high with $\overline{CS}$ and $\overline{RAS}$ low at the rising edge of the clock. The bank addresses BA0 and BA1 are used to select the desired bank. The row addresses A0 through A13 are used to determine which row to activate in the selected bank for x4 and x8 organised components. For x16 components row addresses A0 through A12 have to be applied. The Bank Activate command must be applied before any Read or Write operation can be executed. Immediately after the bank active command, the DDR2 SDRAM can accept a read or write command (with or without Auto-Precharge) on the following clock cycle. If a R/W command is issued to a bank that has not satisfied the tRCDmin specification, then additive latency must be programmed into the device to delay the R/W command which is internally issued to the device. The additive latency value must be chosen to assure tRCDmin is satisfied. Additive latencies of 0, 1, 2, 3 and 4 are supported. Once a bank has been activated it must be precharged before another Bank Activate command can be applied to the same bank. The bank active and precharge times are defined as tRAS and tRP, respectively. The minimum time interval between successive Bank Activate commands to the same bank is determined (tRC). The minimum time interval between Bank Active commands, to any other bank, is the Bank A to Bank B delay time (tRRD).

**Bank Activate Command Cycle: tRCD = 3, AL = 2, tRP = 3, tRRD = 2**



## Read and Write Commands and Access Modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting $\overline{RAS}$ high, $\overline{CS}$ and $\overline{CAS}$ low at the clock's rising edge. $\overline{WE}$ must also be defined at this time to determine whether the access cycle is a read operation ($\overline{WE}$ high) or a write operation ($\overline{WE}$ low). The DDR2 SDRAM provides a wide variety of fast access modes. A single Read or Write Command will initiate a serial read or write operation on successive clock cycles at data rates of up to 667Mb/sec/pin for main memory. The boundary of the burst cycle is restricted to specific segments of the page length.

For example, the 32Mbit x 4 I/O x 4 Bank chip has a page length of 1 kByte (defined by CA0-CA9 & CA11).
In case of a 4-bit burst operation (burst length = 4) the page length of 1 kByte is divided into 512 uniquely addressable segments (4-bits x 4 I/O each). The 4-bit burst operation will occur entirely within one of the 512 segments (defined by CA0-CA8) beginning with the column address supplied to the device during the Read or Write Command (CA0-CA9 & A11). The second, third and fourth access will also occur within this segment, however, the burst order is a function of the starting address, and the burst sequence.

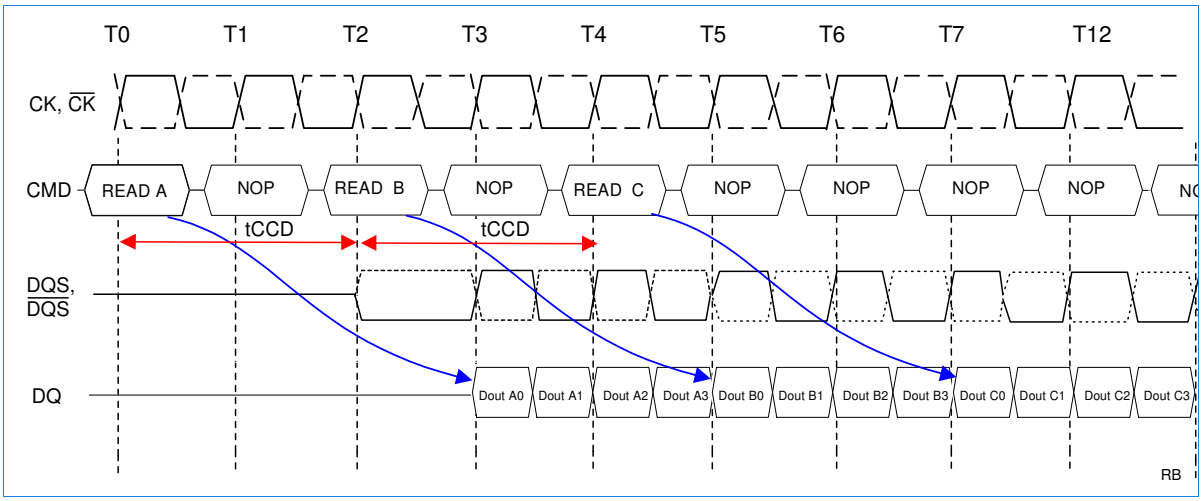
In case of a 8-bit burst operation (burst length = 8) the page length of 1 kByte is divided into 256 uniquely addressable double segments (8-bits x 4 I/O each). The 8-bit burst operation will occur entirely within one of the 256 double segments (defined by CA0-CA7) beginning with the column address supplied to the deivce during the Read or Write Command ( CA0-CA9 & CA11).

A new burst access must not interrupt the previous 4 bit burst operation in case of BL = 4 setting. Therefore the minimum $\overline{CAS}$ to $\overline{CAS}$ delay (tCCD) is a minimum of 2 clocks for read or write cycles.

For 8 bit burst operation (BL = 8 ) the minimum $\overline{CAS}$ to $\overline{CAS}$ delay (tCCD) is 4 clocks for read or write cycles.
Burst interruption is allowed with 8 bit burst operation. For details see the "Burst Interrupt" - Section of this datasheet.

**Example:**

**Read Burst Timing Example : (CL = 3, AL = 0, RL = 3, BL = 4)**

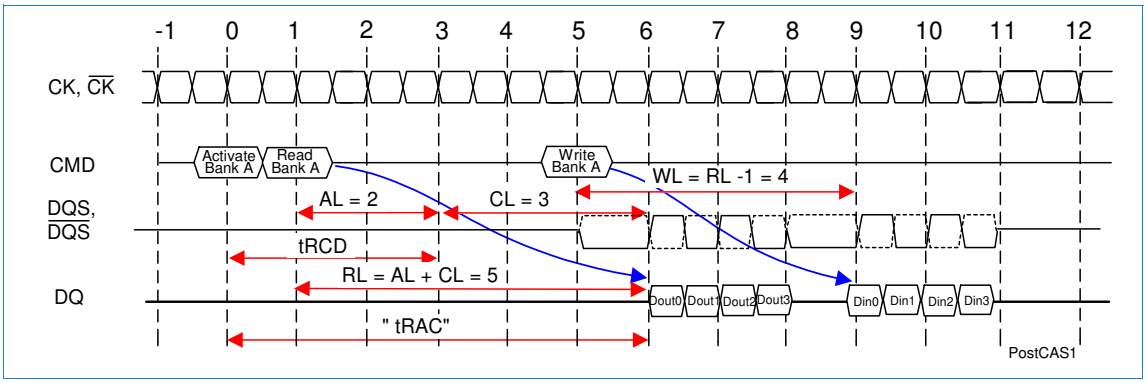


## Posted $\overline{CAS}$

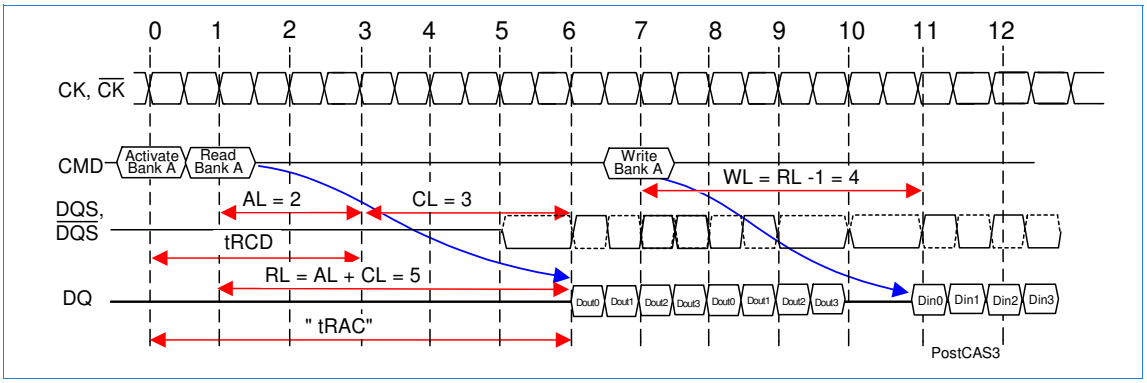
Posted $\overline{CAS}$ operation is supported to make command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. In this operation, the DDR2 SDRAM allows a Read or Write command to be issued immediately after the $\overline{RAS}$ bank activate command (or any time during the $\overline{RAS}$ to $\overline{CAS}$ delay time, tRCD, period). The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is the sum of AL and the $\overline{CAS}$ latency (CL). Therefore if a user chooses to issue a Read/Write command before the tRCDmin, then AL greater than 0 must be written into the EMRS(1). The Write Latency (WL) is always defined as RL - 1 (Read Latency -1) where Read Latency is defined as the sum of Additive Latency plus $\overline{CAS}$ latency (RL=AL+CL). If a user chooses to issue a Read command after the tRCDmin period, the Read Latency is also defined as RL = AL + CL.

**Examples:**

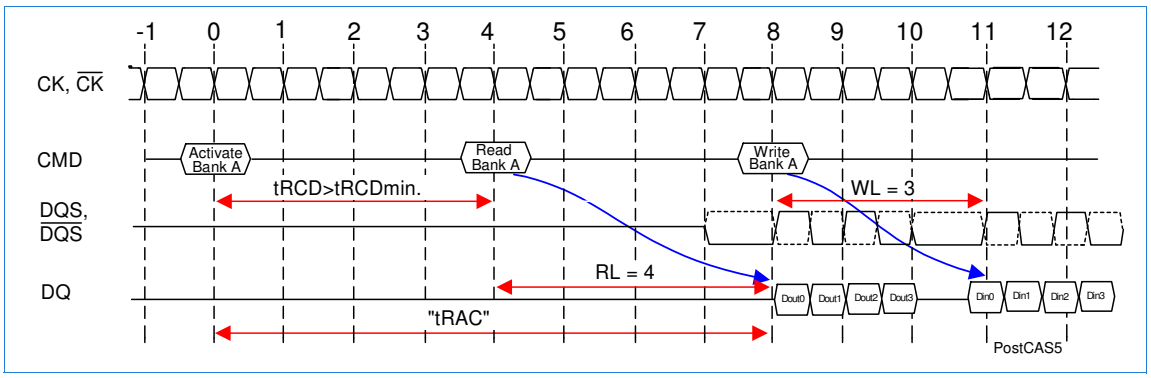
**Read followed by a write to the same bank, Activate to Read delay < tRCDmin:**
**AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL -1) = 4, BL = 4**



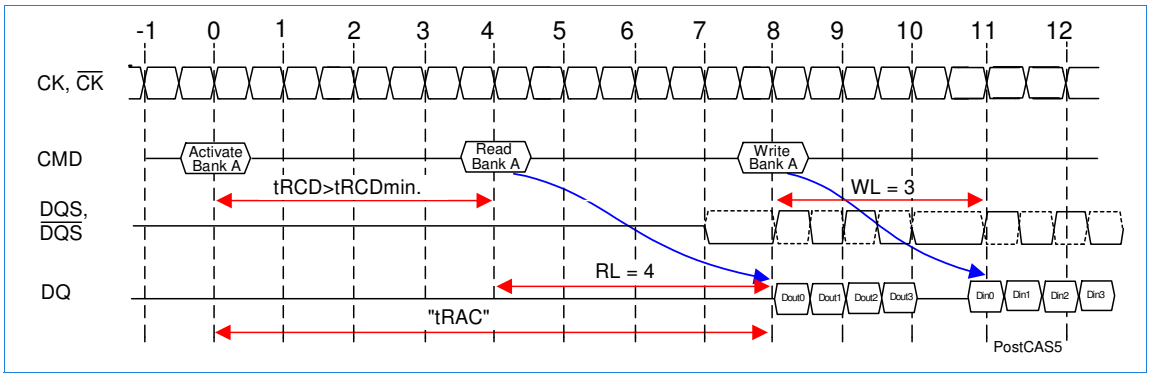

**Read followed by a write to the same bank, Activate to Read delay < tRCDmin:**
**AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL -1) = 4, BL = 8**



**Read followed by a write to the same bank, Activate to Read delay = tRCDmin:**
**AL = 0, CL = 3, RL = (AL + CL) = 3, WL = (RL -1) = 2, BL = 4**




**Read followed by a write to the same bank, Activate to Read delay > tRCDmin:**
**AL = 1, CL = 3, RL = 4, WL = 3, BL = 4**



## Burst Mode Operation

Burst mode operation is used to provide a constant flow of data to memory locations (write cycle), or from memory locations (read cycle). The parameters that define how the burst mode will operate are burst sequence and burst length. The DDR2 SDRAM supports 4 bit and 8 bit burst modes only. For 8 bit burst mode, full interleave address ordering is supported, however, sequential address ordering is nibble based for ease of implementation. The burst length is programmable and defined by the addresses A0 ~ A2 of the MRS. The burst type, either sequential or interleaved, is programmable and defined by the address bit 3 (A3) of the MRS. Seamless burst read or write operations are supported. Interruption of a burst read or write operation is prohibited, when burst length = 4 is programmed. For burst interruption of a read or write burst when burst length = 8 is used, see the “Burst Interruption “ section of this datasheet. A Burst Stop command is not supported on DDR2 SDRAM devices.

### Burst Length and Sequence

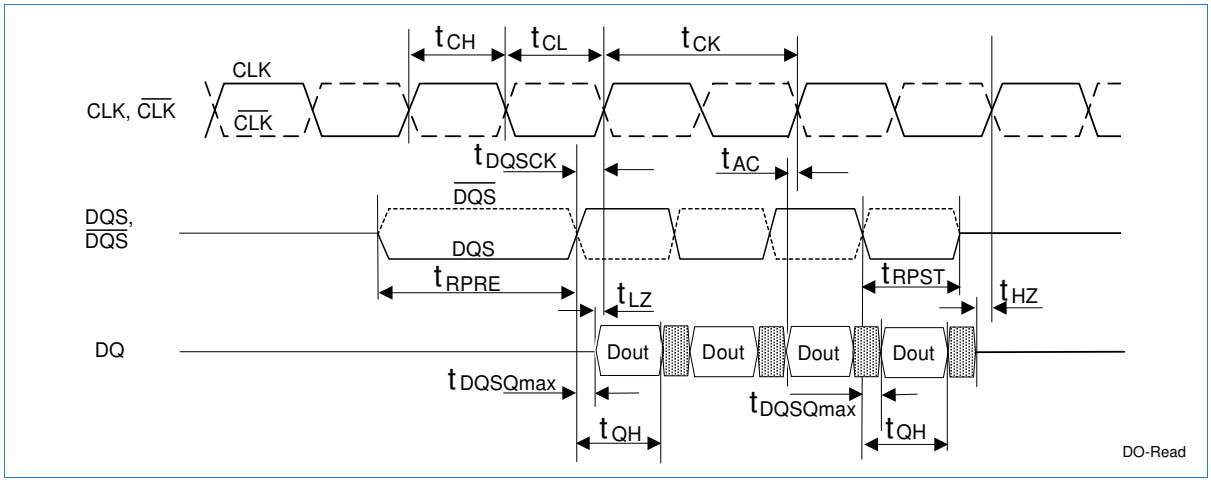
| Burst Length | Starting Address (A2 A1 A0) | Sequential Addressing (decimal) | Interleave Addressing (decimal) |
|---|---|---|---|
| 4 | x 0 0 | 0, 1, 2, 3 | 0, 1, 2, 3 |
| | x 0 1 | 1, 2, 3, 0 | 1, 0, 3, 2 |
| | x 1 0 | 2, 3, 0, 1 | 2, 3, 0, 1 |
| | x 1 1 | 3, 0, 1, 2 | 3, 2, 1, 0 |
| 8 | 0 0 0 | 0, 1, 2, 3, 4, 5, 6, 7 | 0, 1, 2, 3, 4, 5, 6, 7 |
| | 0 0 1 | 1, 2, 3, 0, 5, 6, 7, 4 | 1, 0, 3, 2, 5, 4, 7, 6 |
| | 0 1 0 | 2, 3, 0, 1, 6, 7, 4, 5 | 2, 3, 0, 1, 6, 7, 4, 5 |
| | 0 1 1 | 3, 0, 1, 2, 7, 4, 5, 6 | 3, 2, 1, 0, 7, 6, 5, 4 |
| | 1 0 0 | 4, 5, 6, 7, 0, 1, 2, 3 | 4, 5, 6, 7, 0, 1, 2, 3 |
| | 1 0 1 | 5, 6, 7, 4, 1, 2, 3, 0 | 5, 4, 7, 6, 1, 0, 3, 2 |
| | 1 1 0 | 6, 7, 4, 5, 2, 3, 0, 1 | 6, 7, 4, 5, 2, 3, 0, 1 |
| | 1 1 1 | 7, 4, 5, 6, 3, 0, 1, 2 | 7, 6, 5, 4, 3, 2, 1, 0 |

Note: 1) Page length is a function of I/O organization
128Mb X 4 organization (CA0-CA9, CA11); Page Length = 1 kByte
64Mb X 8 organization (CA0-CA9 ); Page Length = 1 kByte
32Mb X 16 organization (CA0-CA9); Page Length = 2 kByte
2) Order of burst access for sequential addressing is “nibble-based” and therefore different from SDR or DDR components

## Burst Read Command

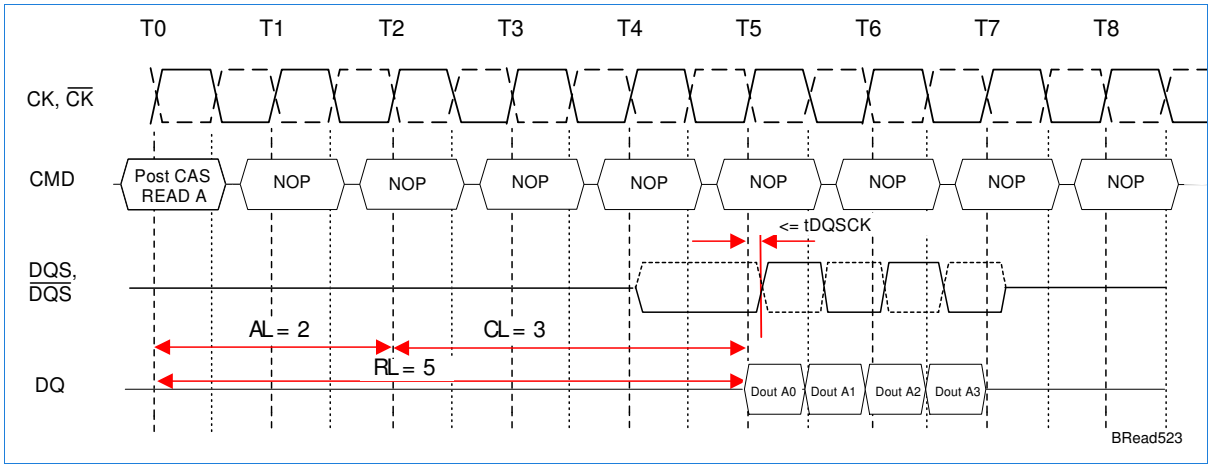
The Burst Read command is initiated by having $\overline{CS}$ and $\overline{CAS}$ low while holding $\overline{RAS}$ and $\overline{WE}$ high at the rising edge of the clock. The address inputs determine the starting column address for the burst. The delay from the start of the command until the data from the first cell appears on the outputs is equal to the value of the read latency (RL). The data strobe output (DQS) is driven low one clock cycle before valid data (DQ) is driven onto the data bus. The first bit of the burst is synchronized with the rising edge of the data strobe (DQS). Each subsequent data-out appears on the DQ pin in phase with the DQS signal in a source synchronous manner. The RL is equal to an additive latency (AL) plus $\overline{CAS}$ latency (CL). The CL is defined by the Mode Register Set (MRS). The AL is defined by the Extended Mode Register Set (EMRS(1))

### Basic Burst Read Timing

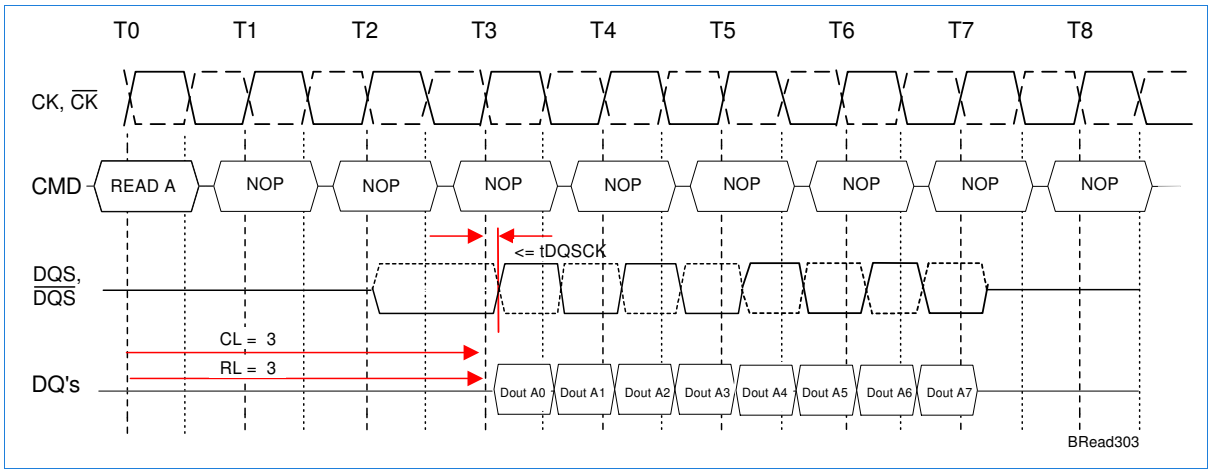



### Examples:

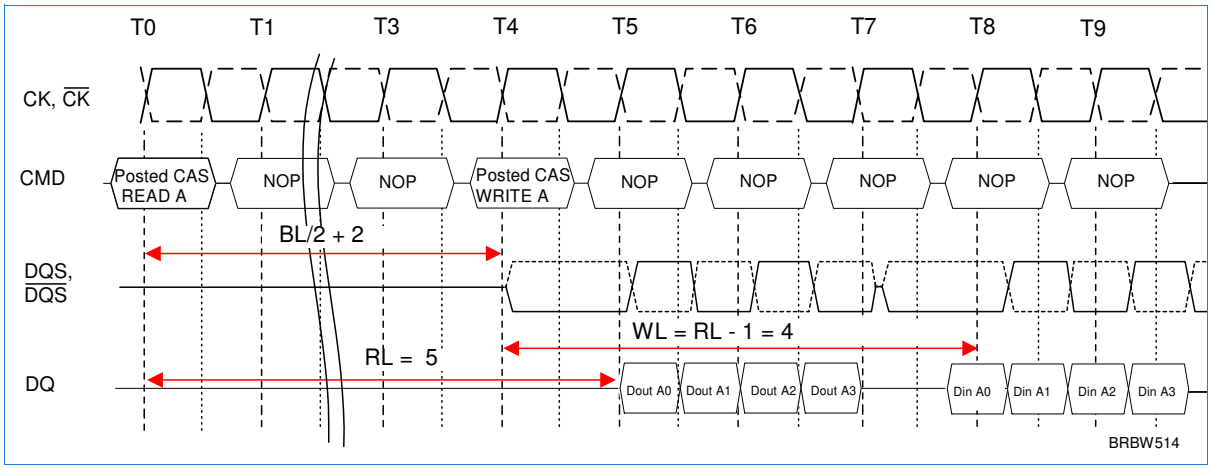
#### Burst Read Operation: RL = 5 (AL = 2, CL = 3, BL = 4)



### Burst Read Operation: RL = 3 (AL = 0, CL = 3, BL = 8)

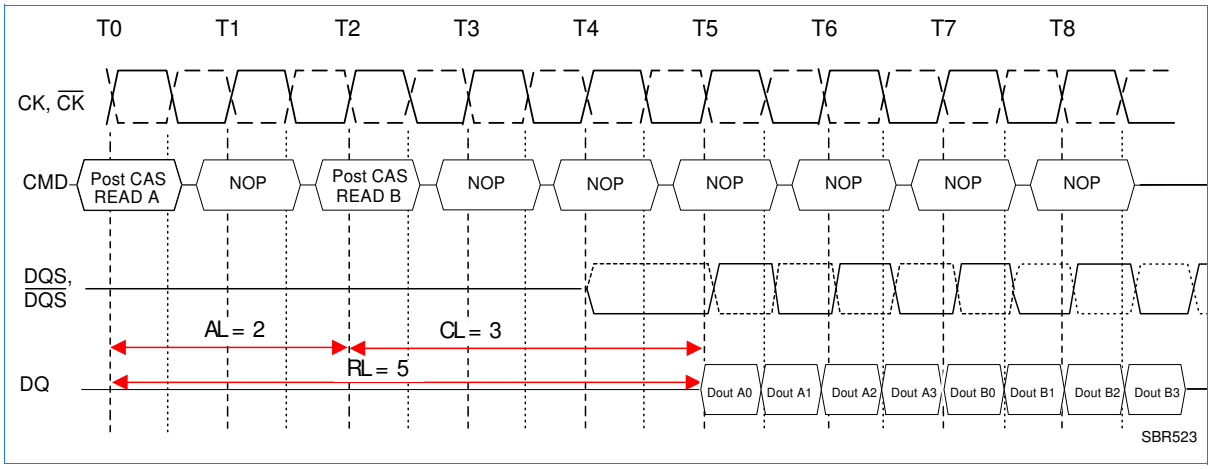



### Burst Read followed by Burst Write : RL = 5, WL = (RL-1) = 4, BL = 4



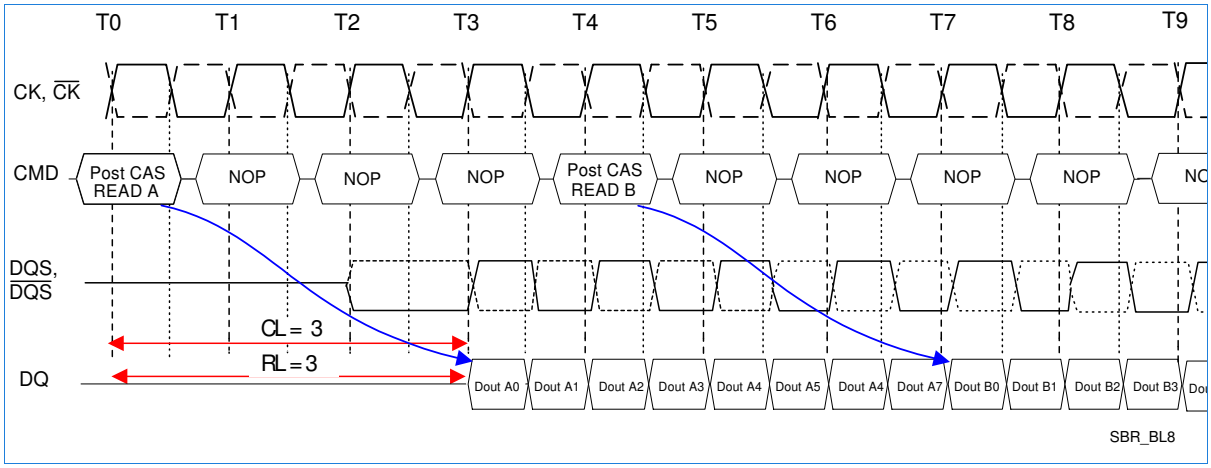

The minimum time from the burst read command to the burst write command is defined by a read-to-write turn-around time, which is BL/2 + 2 clocks.

**Seamless Burst Read Operation : RL = 5, AL = 2, CL = 3, BL = 4**




The seamless burst read operation is supported by enabling a read command at every BL / 2 number of clocks. This operation is allowed regardless of same or different banks as long as the banks are activated.

**Seamless Burst Read Operation : RL = 3, AL = 0, CL = 3, BL = 8 (non interrupting)**

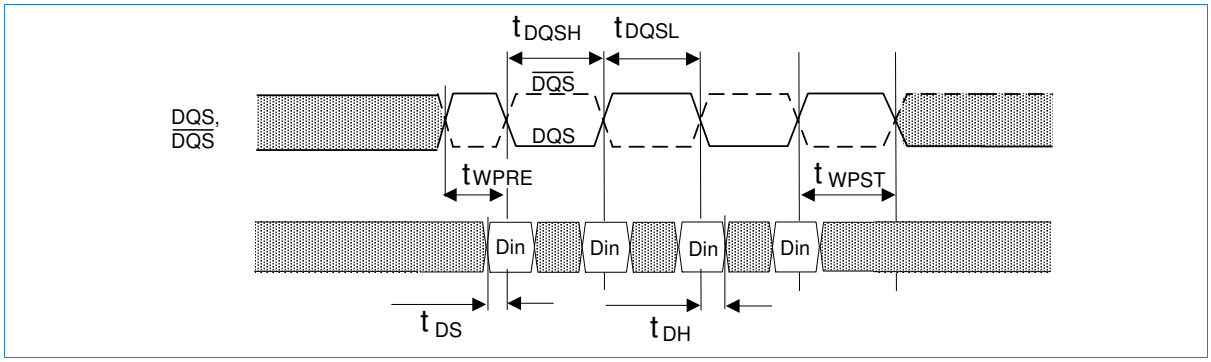



The seamless, non interrupting 8-bit burst read operation is supported by enabling a read command at every BL / 2 number of clocks. This operation is allowed regardless of same or different banks as long as the banks are activated.

## Burst Write Command

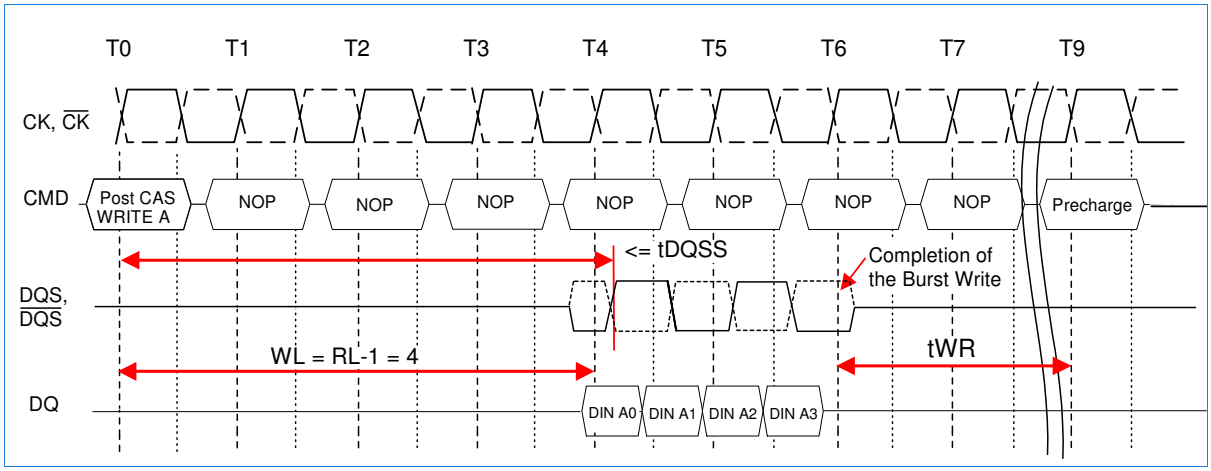
The Burst Write command is initiated by having $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ low while holding $\overline{RAS}$ high at the rising edge of the clock. The address inputs determine the starting column address. Write latency (WL) is defined by a read latency (RL) minus one and is equal to (AL + CL -1). A data strobe signal (DQS) has to be driven low (preamble) a time tWPRE prior to the WL. The first data bit of the burst cycle must be applied to the DQ pins at the first rising edge of the DQS following the preamble. The tDQSS specification must be satisfied for write cycles. The subsequent burst bit data are issued on successive edges of the DQS until the burst length is completed. When the burst has finished, any additional data supplied to the DQ pins will be ignored. The DQ signal is ignored after the burst write operation is complete. The time from the completion of the burst write to bank precharge is named “write recovery time” (tWR) and is the time needed to store the write data into the memory array. tWR is an analog timing parameter (see the AC table in this specification) and is not the programmed value for WR in the MRS.

### Basic Burst Write Timing

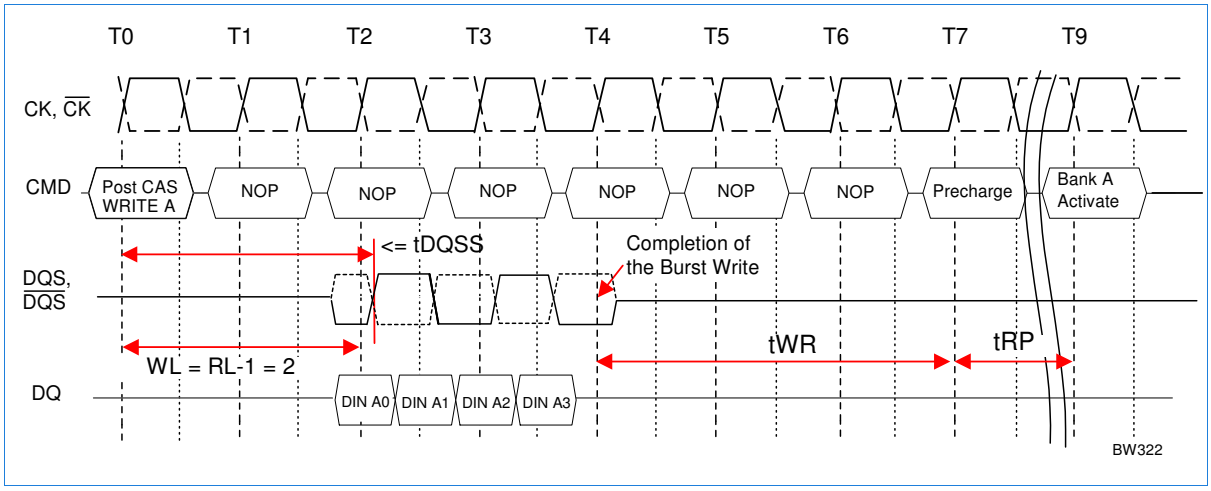



**Example:**.

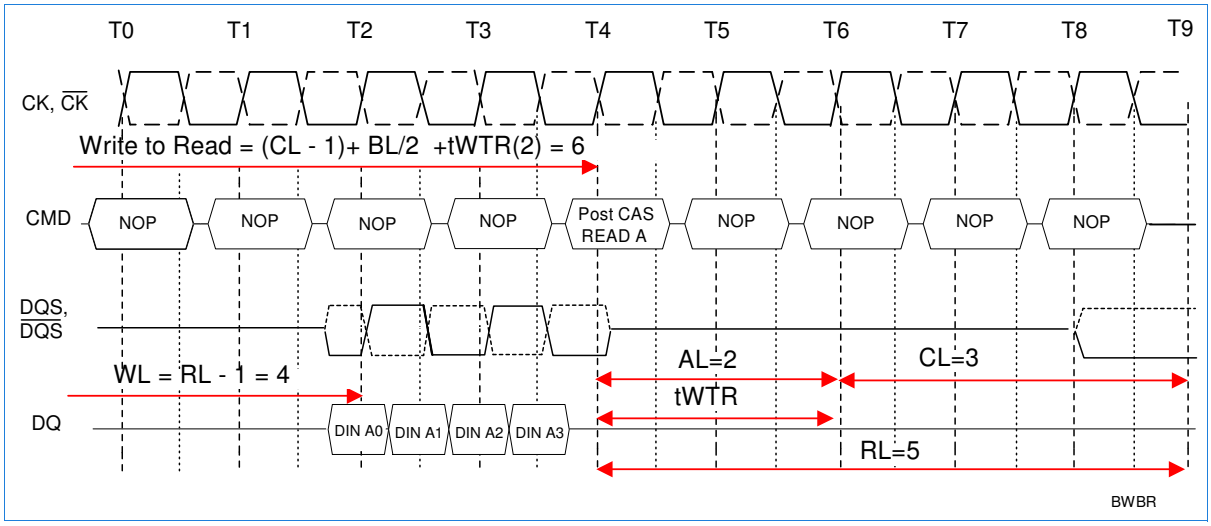
**Burst Write Operation : RL = 5 (AL = 2, CL = 3), WL = 4, BL = 4**



**Burst Write Operation : RL = 3 (AL = 0, CL = 3), WL = 2, BL = 4**

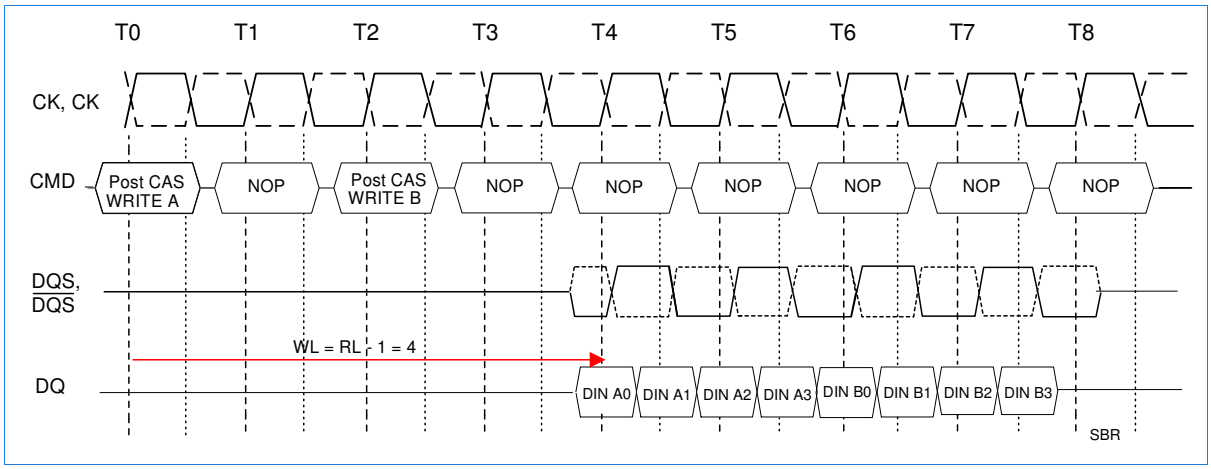



**Burst Write followed by Burst Read : RL = 5 (AL = 2, CL = 3), WL = 4, tWTR = 2, BL = 4**



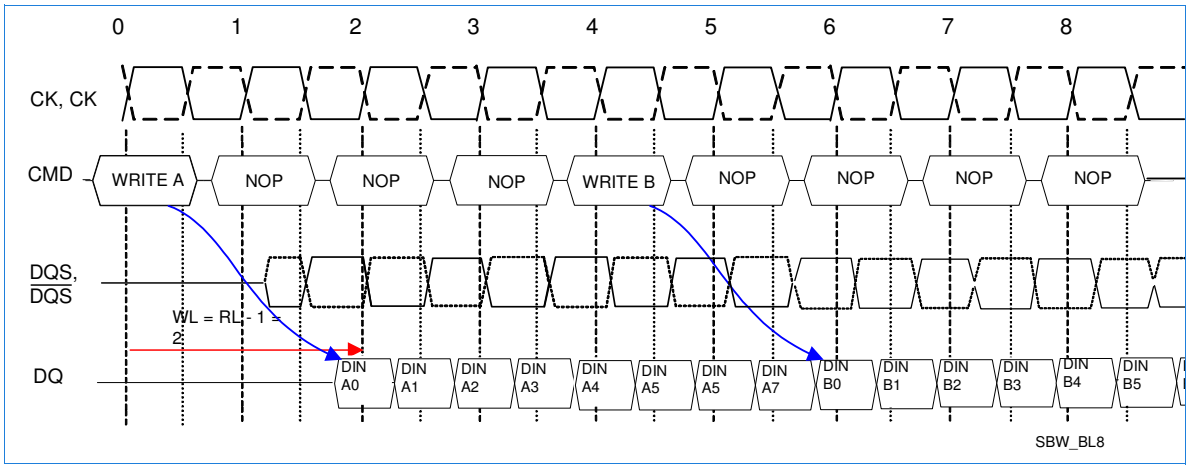

The minimum number of clocks from the burst write command to the burst read command is (CL - 1) +BL/2 + tWTR where tWTR is the write-to-read turn-around time tWTR expressed in clock cycles. The tWTR is not a write recovery time (tWR) but the time required to transfer 4 bit write data from the input buffer into sense amplifiers in the array.

### Seamless Burst Write Operation : RL = 5, WL = 4, BL = 4




The seamless burst write operation is supported by enabling a write command every BL / 2 number of clocks. This operation is allowed regardless of same or different banks as long as the banks are activated.

### Seamless Burst Write Operation : RL = 3, WL = 2, BL = 8, non interrupting

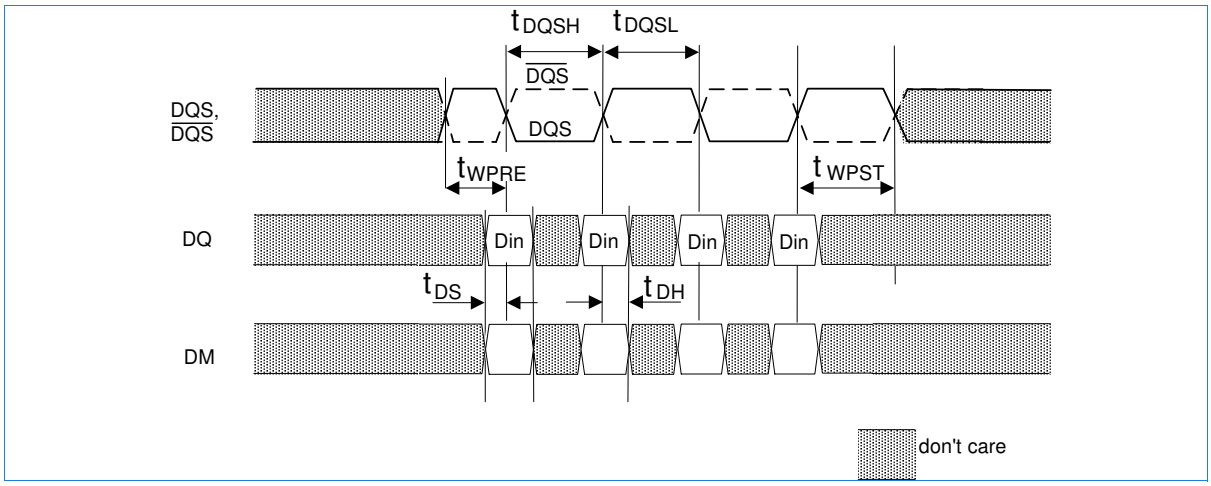



The seamless, non interrupting 8-bit burst write operation is supported by enabling a write command at every BL / 2 number of clocks. This operation is allowed regardless of same or different banks as long as the banks are activated.

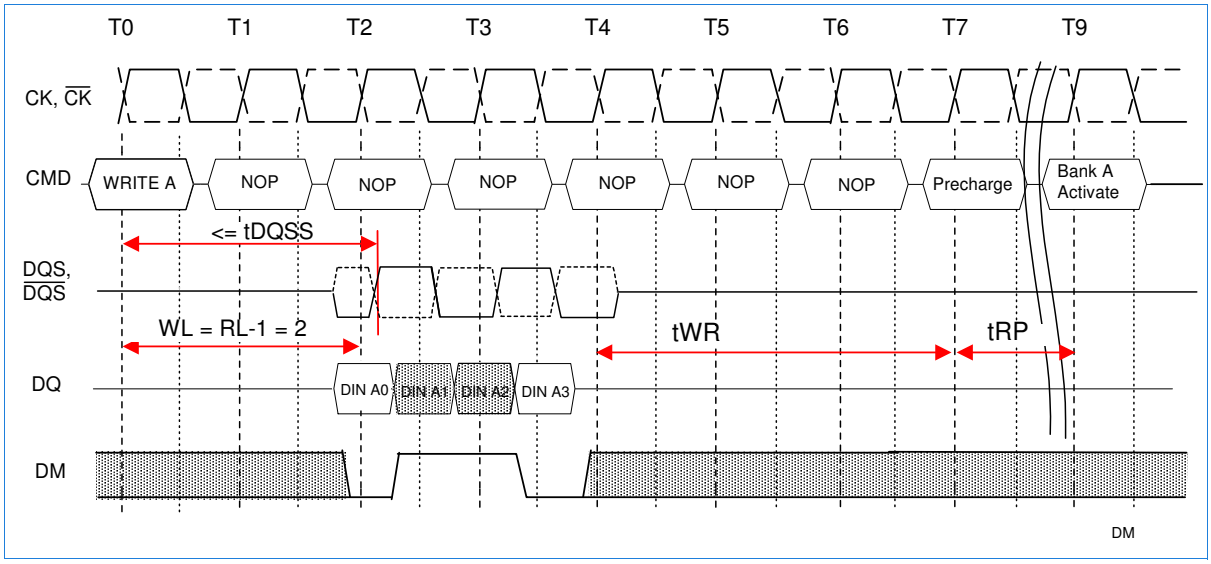
## Write Data Mask

One write data mask input (DM) for x4 and x8 components and two write data mask inputs (LDM, UDM) for x16 components are supported on DDR2 SDRAMs, consistent with the implementation on DDR SDRAMs. It has identical timings on write operations as the data bits, and though used in a uni-directional manner, is internally loaded identically to data bits to insure matched system timing. Data mask is not used during read cycles. If DM is high during a write burst coincident with the write data, the write data bit is not written to the memory. For x8 components the DM function is disabled, when RDQS / $\overline{RDQS}$ are enabled by EMRS(1).

### Write Data Mask Timing




### Burst Write Operation with Data Mask : RL = 3 (AL = 0, CL = 3), WL = 2, tWR = 3 , BL = 4



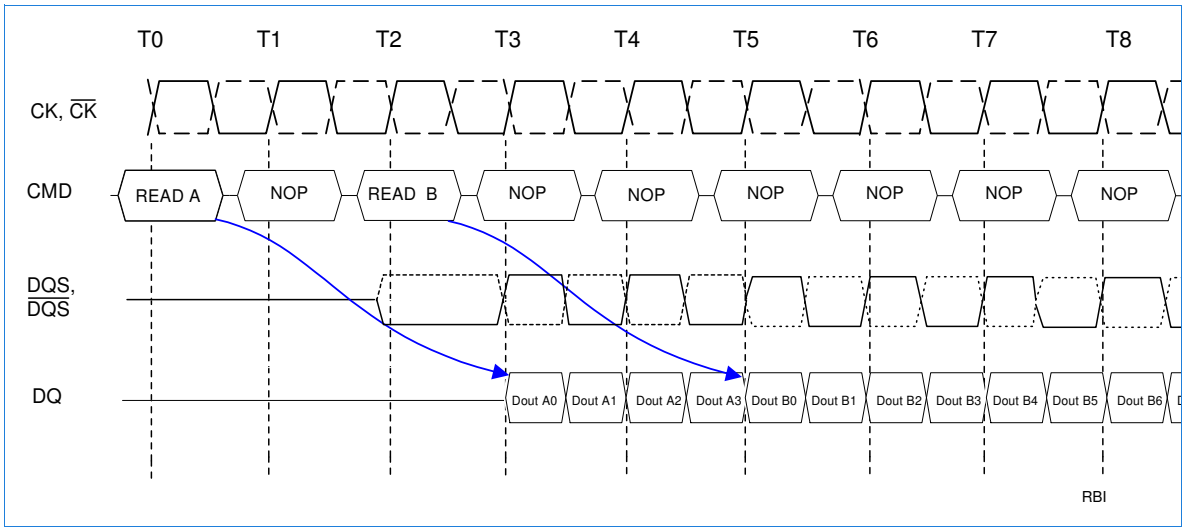
## Burst Interruption

Interruption of a read or write burst is prohibited for burst length of 4 and only allowed for burst length of 8 under the following conditions:

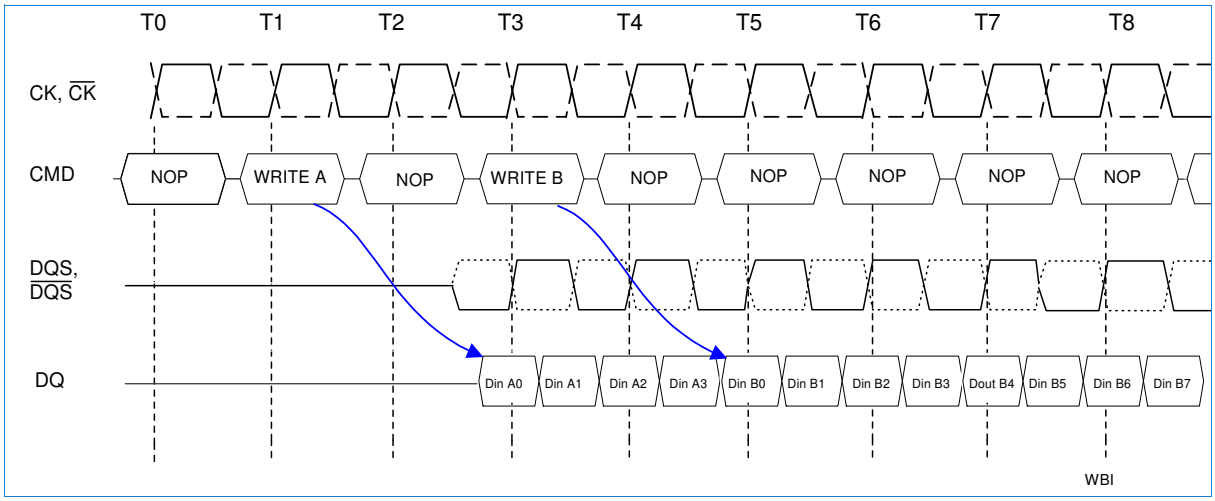
1. A Read Burst of 8 can only be interrupted by another Read command. Read burst interruption by a Write or Precharge Command is prohibited.
2. A Write Burst of 8 can only be interrupted by another Write command. Write burst interruption by a Read or Precharge Command is prohibited.
3. Read burst interrupt must occur exactly two clocks after the previous Read command. Any other Read burst interrupt timings are prohibited.
4. Write burst interrupt must occur exactly two clocks after the previous Write command. Any other Read burst interrupt timings are prohibited.
5. Read or Write burst interruption is allowed to any bank inside the DDR2 SDRAM.
6. Read or Write burst with Auto-Precharge enabled is not allowed to be interrupted.
7. Read burst interruption is allowed by a Read with Auto-Precharge command.
8. Write burst interruption is allowed by a Write with Auto-Precharge command.
9. All command timings are referenced to burst length set in the mode register. They are not referenced to the actual burst. For example, Minimum Read to Precharge timing is AL + BL/2 where BL is the burst length set in the mode register and not the actual burst (which is shorter because of interrupt). Minimum Write to Precharge timing is WL + BL/ 2 + tWR, where tWR starts with the rising clock after the un-interrupted burst end and not form the end of the actual burst end.

**Examples:**

**Read Burst Interrupt Timing Example : (CL = 3, AL = 0, RL = 3, BL = 8)**



## Write Burst Interrupt Timing Example : ( CL = 3, AL = 0, WL = 2, BL = 8)



## Precharge Command

The Precharge Command is used to precharge or close a bank that has been activated. The Precharge Command is triggered when $\overline{CS}$, $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at the rising edge of the clock. The Pre-charge Command can be used to precharge each bank independently or all banks simultaneously. Three address bits A10, BA0 and BA1 are used to define which bank to precharge when the command is issued

**Bank Selection for Precharge by Address Bit**

| A10 | BA0 | BA1 | Precharge Bank(s) |
|---|---|---|---|
| LOW | LOW | LOW | Bank 0 only |
| LOW | LOW | HIGH | Bank 1 only |
| LOW | HIGH | LOW | Bank 2 only |
| LOW | HIGH | HIGH | Bank 3 only |
| HIGH | Don't Care | Don't Care | all banks |

**Burst Read Operation Followed by a Precharge**

The following rules apply as long as the tRTP timing parameter - Internal Read to Precharge Command delay time - is less or equal two clocks, which is the case for operating frequencies less or equal 266 Mhz (DDR2 400 and 533 speed sorts):

Minimum Read to Precharge command spacing to the same bank = AL + BL/2 clocks. For the earliest possible precharge, the Precharge command may be issued on the rising edge which is "Additive Latency (AL) + BL/2 clocks" after a Read Command, as long as the minimum tRAS timing is satisfied.

A new bank active command may be issued to the same bank if the following two conditions are satisfied simultaneously:

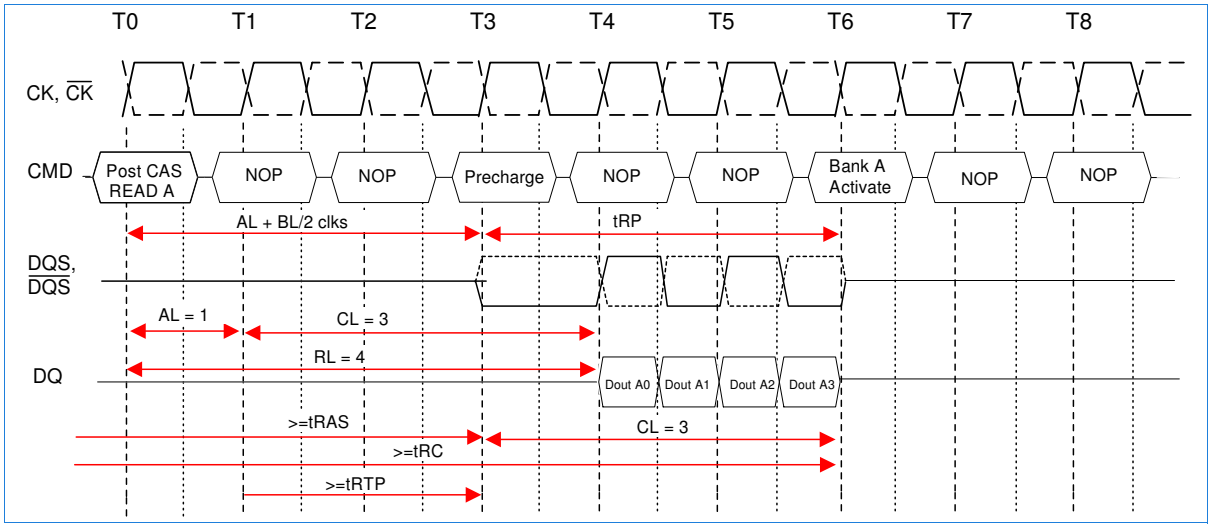
(1) The RAS precharge time (tRP) has been satisfied from the clock at which the precharge begins.

(2) The RAS cycle time (tRCmin) from the previous bank activation has been satisfied.

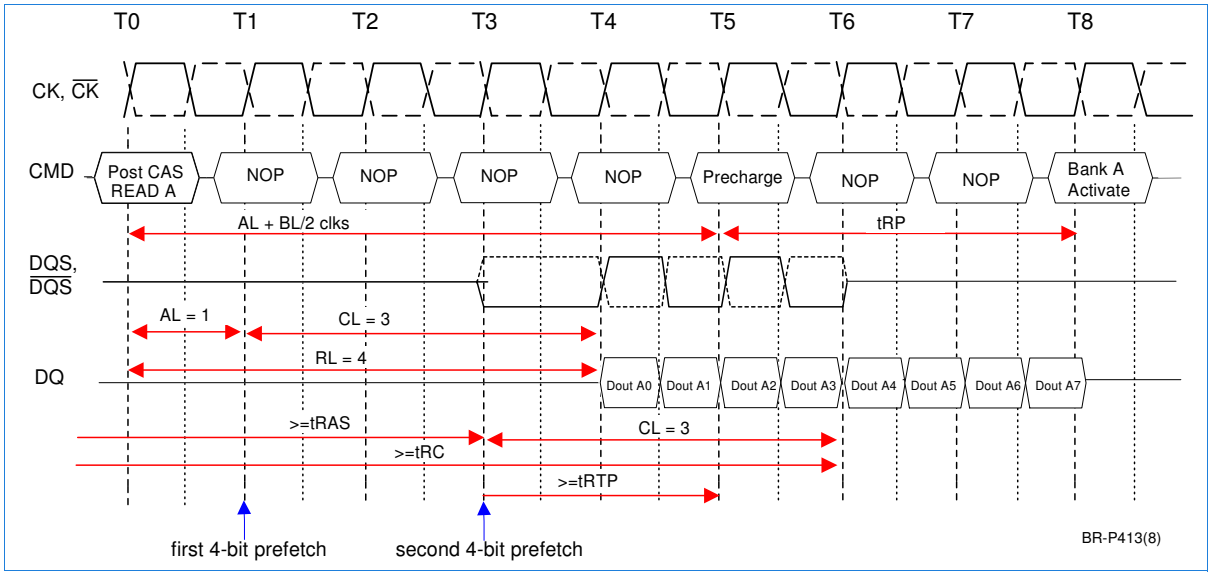
For operating frequencies higher than 266 MHz, tRTP becomes > 2 clocks and one additional clock cycle has to be added for the minimum Read to Precharge command spacing, which now becomes AL + BL/2 + 1 clocks.

**Examples:**

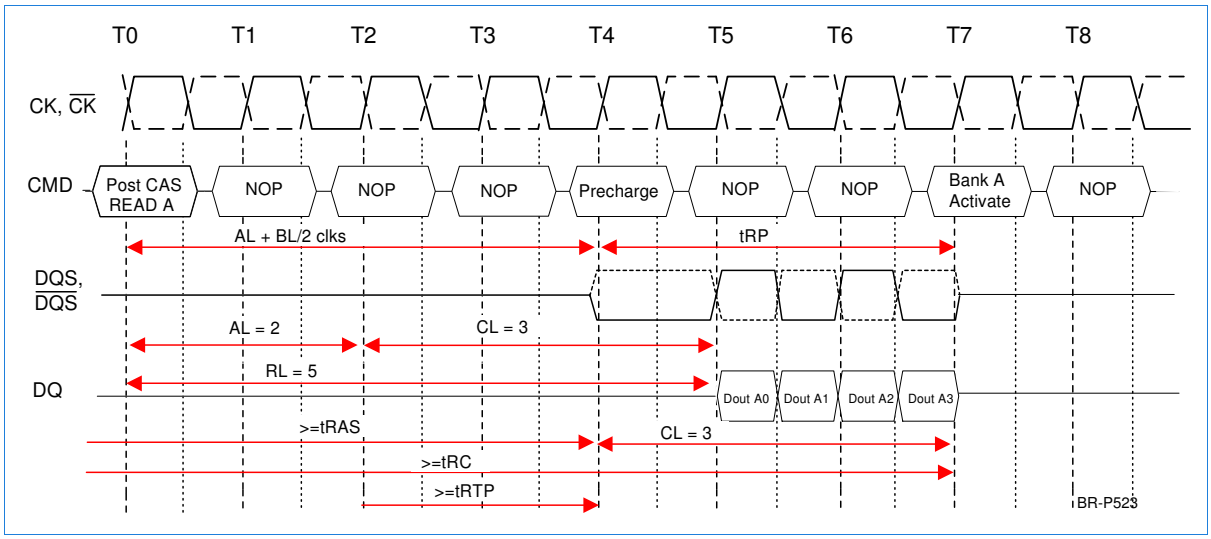
**Burst Read Operation Followed by Precharge: RL = 4 (AL = 1, CL = 3), BL = 4, tRTP <= 2 clocks**



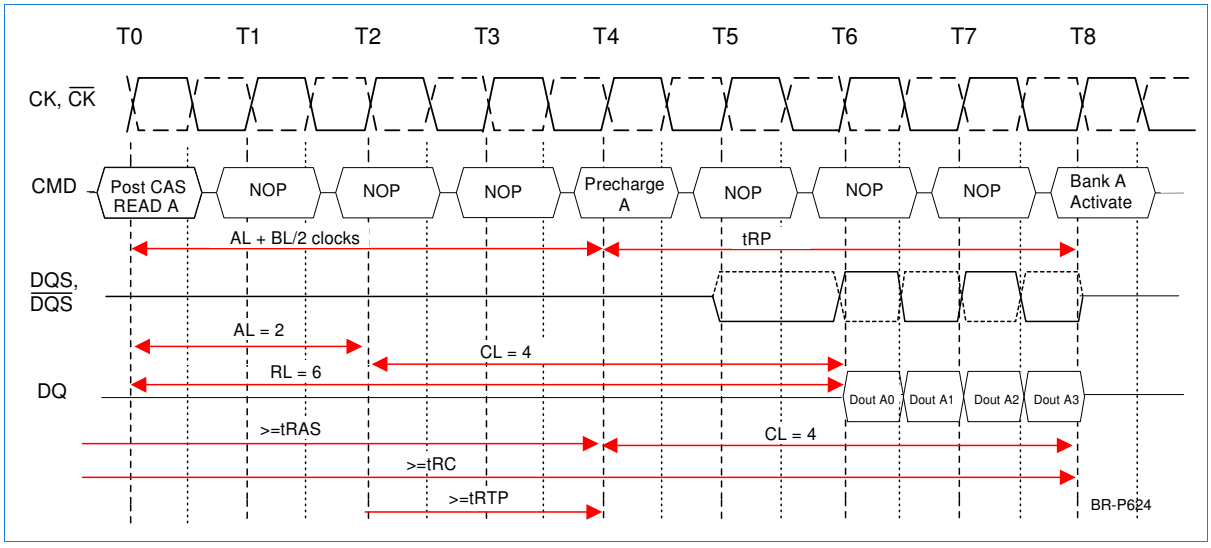

**Burst Read Operation Followed by Precharge: RL = 4 (AL = 1, CL = 3), BL = 8, tRTP <= 2 clocks**



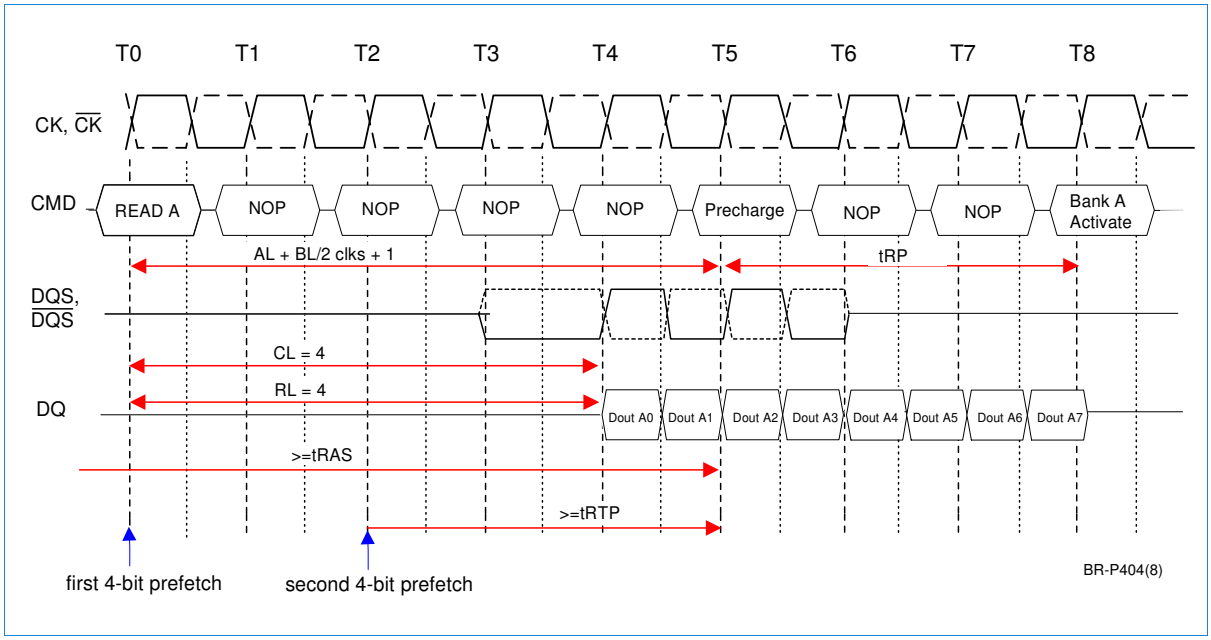
### Burst Read Operation Followed by Precharge: RL = 5 (AL = 2, CL = 3), BL = 4, tRTP <= 2 clocks




### Burst Read Operation Followed by Precharge: RL = 6, (AL = 2, CL = 4), BL = 4, tRTP <= 2 clocks



## Burst Read Operation Followed by Precharge: RL = 4, (AL = 0, CL = 4), BL = 8, tRTP > 2 clocks

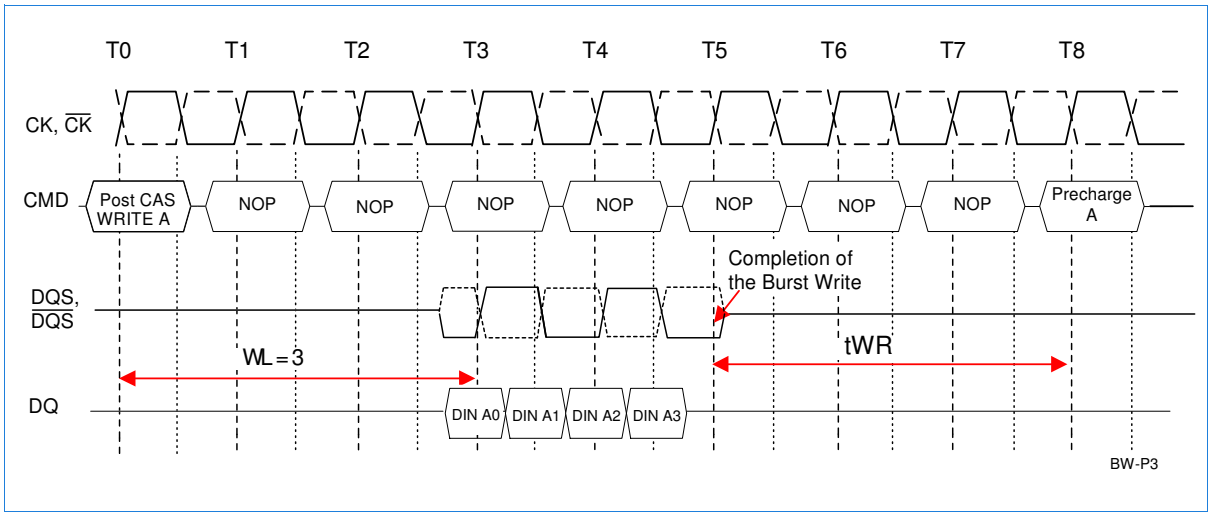


## Burst Write followed by Precharge

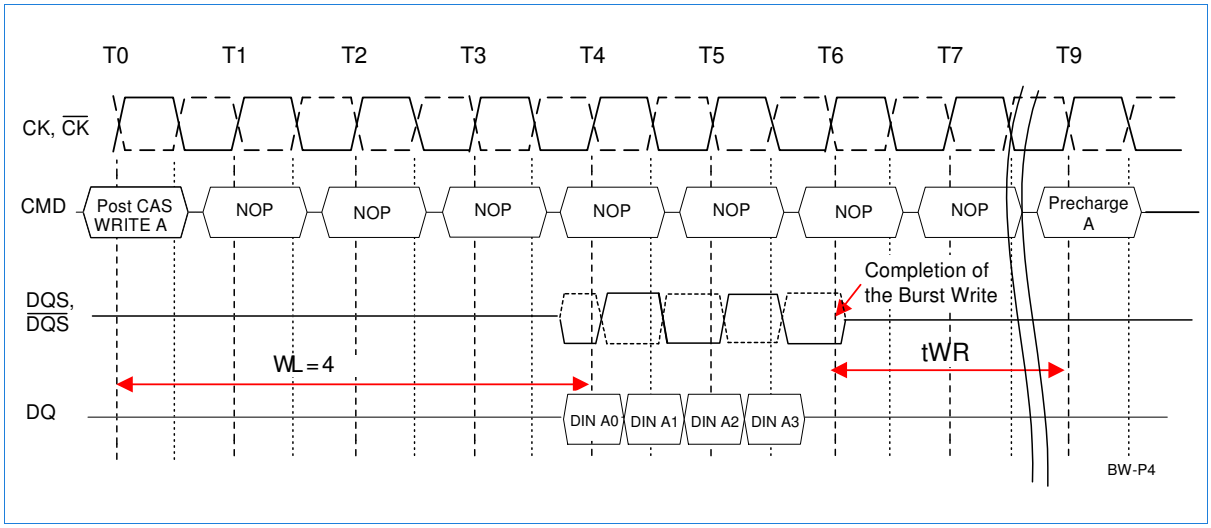
Minimum Write to Precharge command spacing to the same bank = **WL + BL/2 + tWR**. For write cycles, a delay must be satisfied from the completion of the last burst write cycle until the Precharge command can be issued. This delay is known as a write recovery time (t WR ) referenced from the completion of the burst write to the Precharge command. No Precharge command should be issued prior to the tWR delay, as DDR2 SDRAM does not support any burst interrupt by a Precharge command. tWR is an analog timing parameter (see the AC table in this datasheet) and is not the programmed value for tWR in the MRS.

**Examples:**

**Burst Write followed by Precharge : WL = (RL - 1) = 3, BL = 4, tWR = 3**




**Burst Write followed by Precharge : WL = (RL - 1) = 4, BL = 4, tWR = 3**



## Auto-Precharge Operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the Precharge Command or the Auto-Precharge function. When a Read or a Write Command is given to the DDR2 SDRAM, the $\overline{CAS}$ timing accepts one extra address, column address A10, to allow the active bank to auto-matically begin precharge at the earliest possible moment during the burst read or write cycle. If A10 is low when the Read or Write Command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst sequence. If A10 is high when the Read or Write Com-mand is issued, then the Auto-Precharge function is enabled. During Auto-Precharge, a Read Command will execute as normal with the exception that the active bank will begin to precharge internally on the rising edge which is CAS Latency (CL) clock cycles before the end of the read burst. Auto-Precharge is also implemented for Write Commands.The precharge operation engaged by the Auto-Precharge command will not begin until the last data of the write burst sequence is properly stored in the memory array. This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon CAS Latency) thus improving system performance for random data access. The RAS lockout circuit internally delays thepprecharge operation until the array restore operation has been completed so that the Auto-Precharge command may be issued with any read or write command.

### Burst Read with Auto-Precharge

If A10 is high when a Read Command is issued, the Read with Auto-Precharge function is engaged. The DDR2 SDRAM starts an Auto-Precharge operation on the rising edge which is (AL + BL/2) cycles later from the Read with AP command if tRAS(min) and tRTP are satisfied. If tRAS(min) is not satisfied at the edge, the start point of Auto-Precharge operation will be delayed until tRAS(min) is satisfied. If tRTP(min) is not satisfied at the edge, the start point of Auto-Precharge operation will be delayed until tRTP(min) is satisfied.
In case the internal precharge is pushed out by tRTP, tRP starts at the point where the internal precharge happens (not at the next rising clock edge after this event). So for BL = 4 the minimum time from Read with Auto-Precharge to the next Activate command becomes AL + tRTP + tRP. For BL = 8 the time from Read with Auto-Precharge to the next Activate command is AL + 2 + tRTP + tRP. Note that both parameters tRTP and tRP have to be rounded up to the next integer value. In any event internal precharge does not start earlier than two clocks after the last 4-bit prefetch.

A new bank active (command) may be issued to the same bank if the following two conditions are satisfied simultaneously:

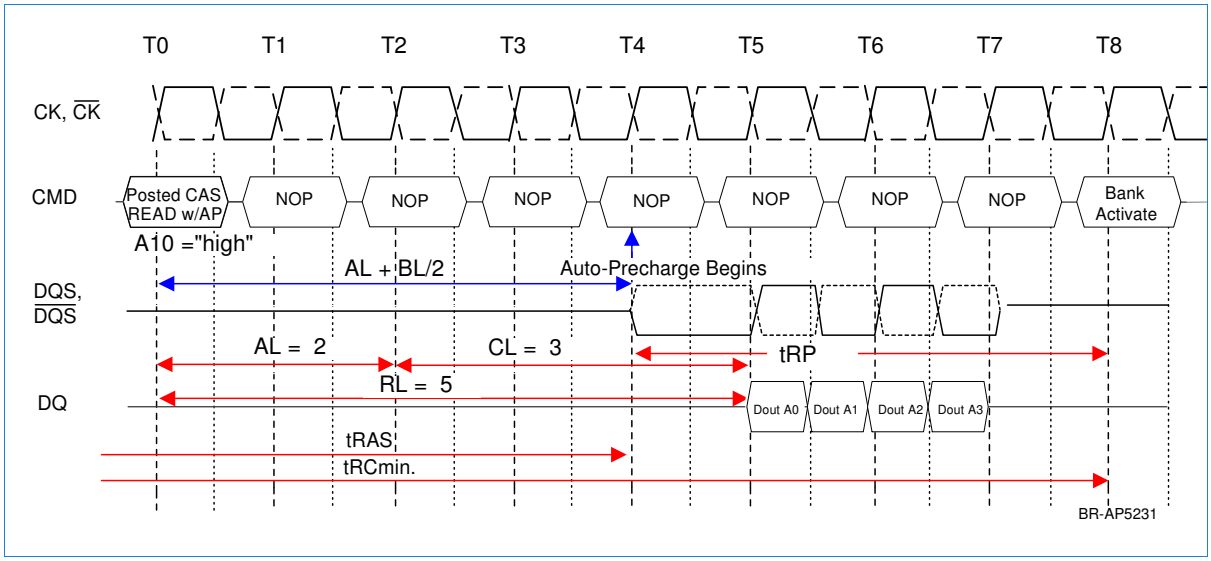
(1) The $\overline{RAS}$ precharge time (tRP) has been satisfied from the clock at which the Auto-Precharge begins.

(2) The $\overline{RAS}$ cycle time (tRC) from the previous bank activation has been satisfied.

**Examples:**

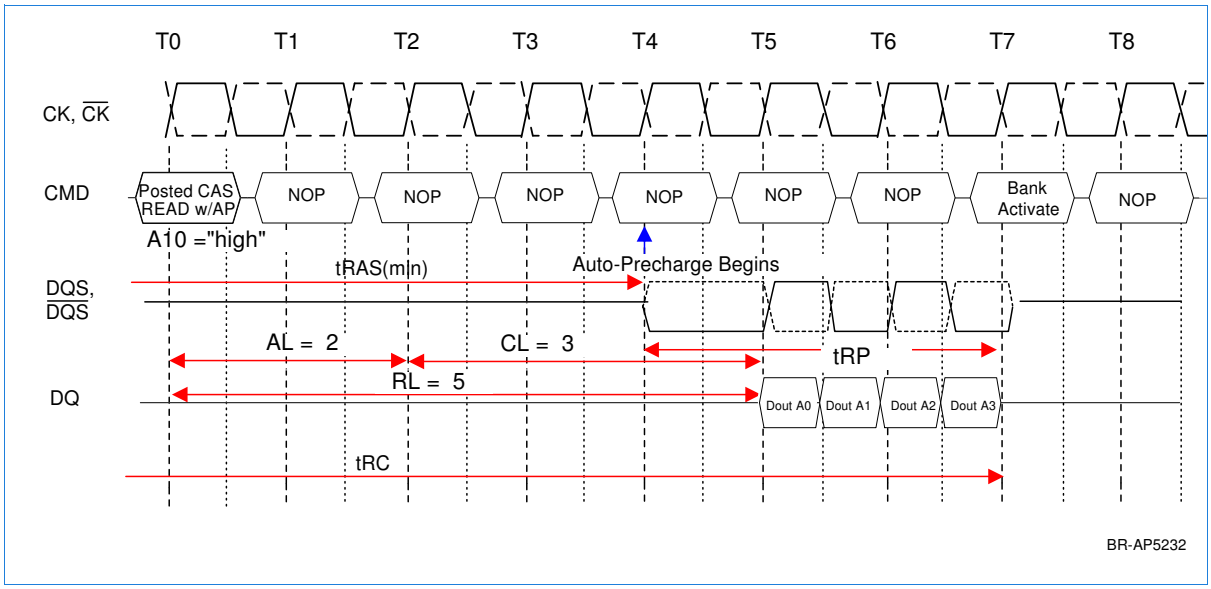
**Burst Read with Auto-Precharge followed by an activation to the Same Bank (tRC Limit)**

**RL = 5 (AL = 2, CL = 3), BL = 4, tRTP <= 2 clocks**



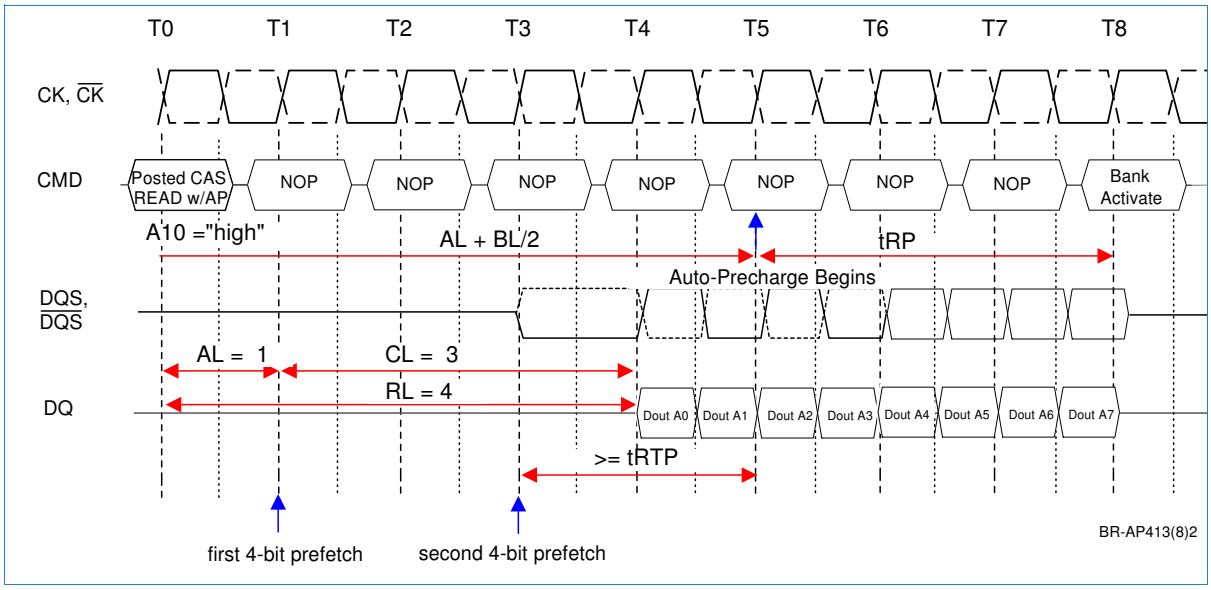

**Burst Read with Auto-Precharge followed by an Activation to the Same Bank (tRAS Limit):**

**RL = 5 ( AL = 2, CL = 3), BL = 4, tRTP <= 2 clocks**



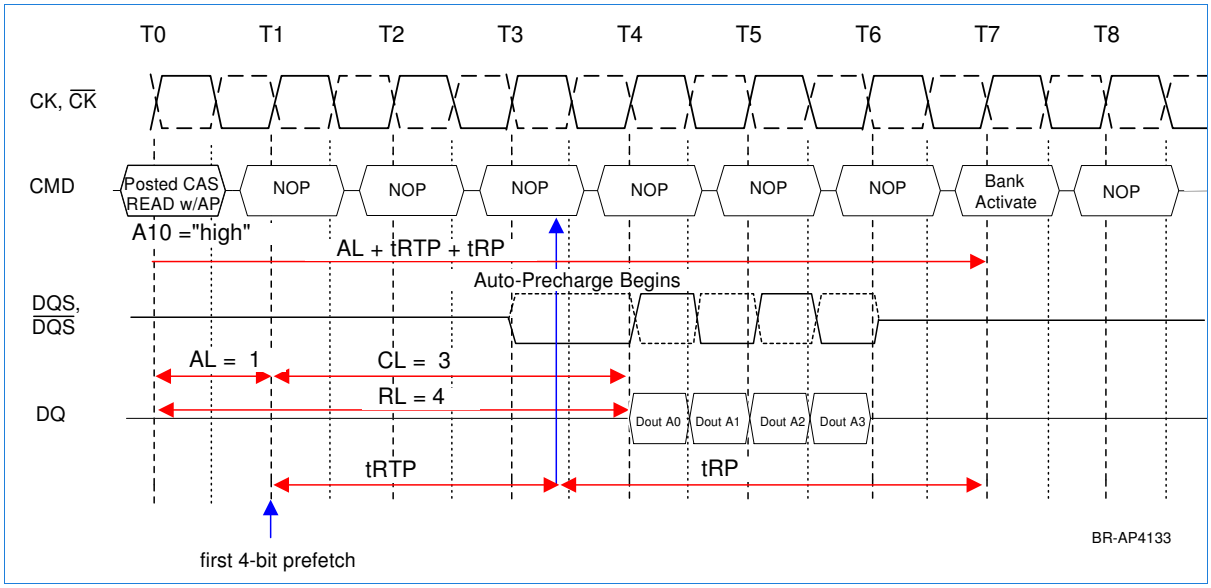
**Burst Read with Auto-Precharge followed by an Activation to the Same Bank:**

**RL = 4 ( AL = 1, CL = 3), BL = 8, tRTP <= 2 clocks**




**Burst Read with Auto-Precharge followed by an Activation to the Same Bank:**

**RL = 4 ( AL = 1, CL = 3), BL = 4, tRTP > 2 clocks**



## Burst Write with Auto-Precharge

If A10 is high when a Write Command is issued, the Write with Auto-Precharge function is engaged. The DDR2 SDRAM automatically begins precharge operation after the completion of the write burst plus the write recovery time delay (WR), programmed in the MRS register, as long as tRAS is satisfied. The bank undergoing Auto-Precharge from the completion of the write burst may be reactivated if the following two conditions are satisfied.

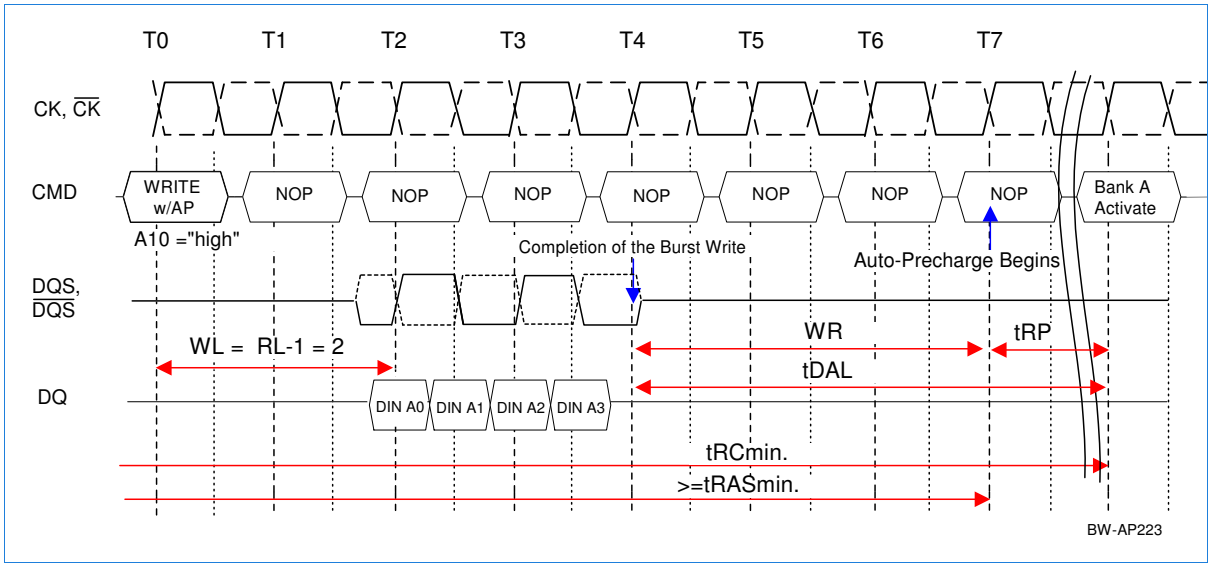
(1) The last data-in to bank activate delay time (tDAL = WR + tRP) has been satisfied.

(2) The RAS cycle time (tRC) from the previous bank activation has been satisfied.

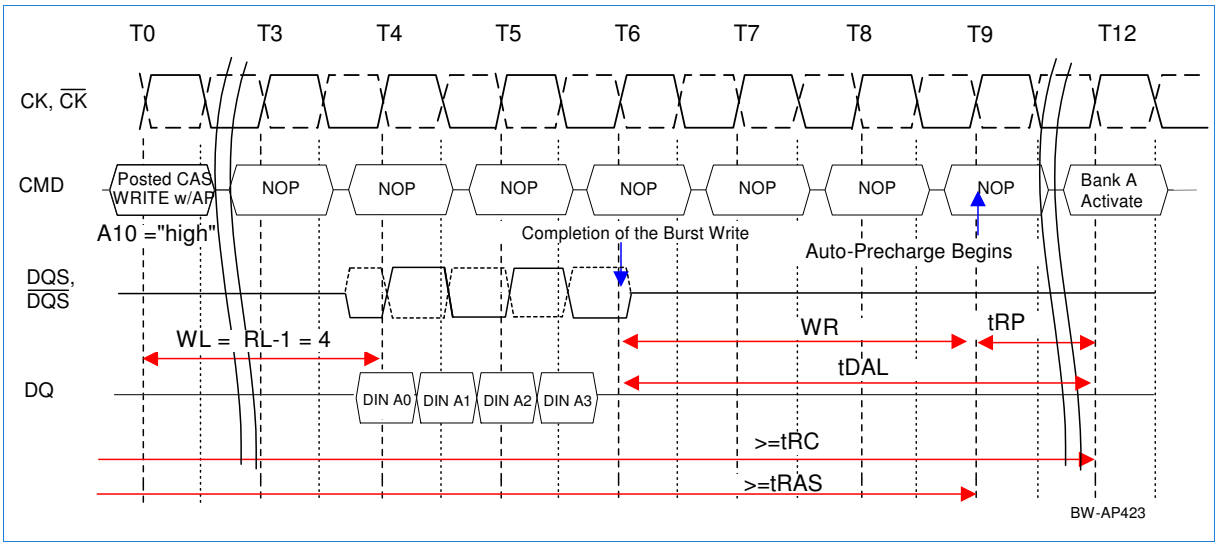
In DDR2 SDRAMs the write recovery time delay (WR ) has to be programmed into the MRS mode register. As long as the analog twr timing parameter is not violated, WR can be programmed between 2 and 6 clock cycles. Minimum Write to Activate command spacing to the same bank = **WL + BL/2 + tDAL.**

**Examples:**

**Burst Write with Auto-Precharge (tRC Limit) : WL = 2, tDAL = 6 (WR = 3, tRP = 3) , BL = 4**



**Burst Write with Auto-Precharge (WR + tRP Limit) : WL = 4, tDAL = 6 (WR = 3, tRP = 3), BL = 4**




## Concurrent Auto-Precharge

DDR2 devices support the “Concurrent Auto-Precharge” feature. A Read with Auto-Precharge enabled, or a Write with Auto-Precharge enabled, may be followed by any command to the other bank, as long as that command does not interrupt the read or write data transfer, and all other related limitations (e.g. contention between Read data and Write data must be avoided externally and on the internal data bus.

The minimum delay from a Read or Write command with Auto-Precharge enabled, to a command to a different bank, is summarized in the table below. As defined, the WL = RL - 1 for DDR2 devices which allows the command gap and corresponding data gaps to be minimized.

| From Command | To Command (different bank, non-interrupting command) | Minimum Delay with Concurrent Auto-Pre-charge Support | Units | Note |
|---|---|---|---|---|
| WRITE w/AP | Read or Read w/AP | (CL -1) + (BL/2) + tWTR | tCK | |
| | Write ot Write w/AP | BL/2 | tCK | |
| | Precharge or Activate | 1 | tCK | 1) |
| Read w/AP | Read or Read w/AP | BL/2 | tCK | |
| | Write or Write w/AP | BL/2 + 2 | tCK | |
| | Precharge or Activate | 1 | tCK | 1) |

Note:
1) This rule only applies to a selective Precharge command to another banks, a Precharge-All command is illegal

## Refresh

SDRAMs require a refresh of all rows in any rolling 64 ms interval. Each refresh is generated in one of two ways : by an explicit Auto-Refresh command, or by an internally timed event in Self-Refresh mode. Dividing the number of device rows into the rolling 64 ms interval defined the average refresh interval tREFI, which is a guideline to controlles for distributed refresh timing. For example, a 512Mbit DDR2 SDRAM has 8192 rows resulting in a tREFI of 7,8 µs.

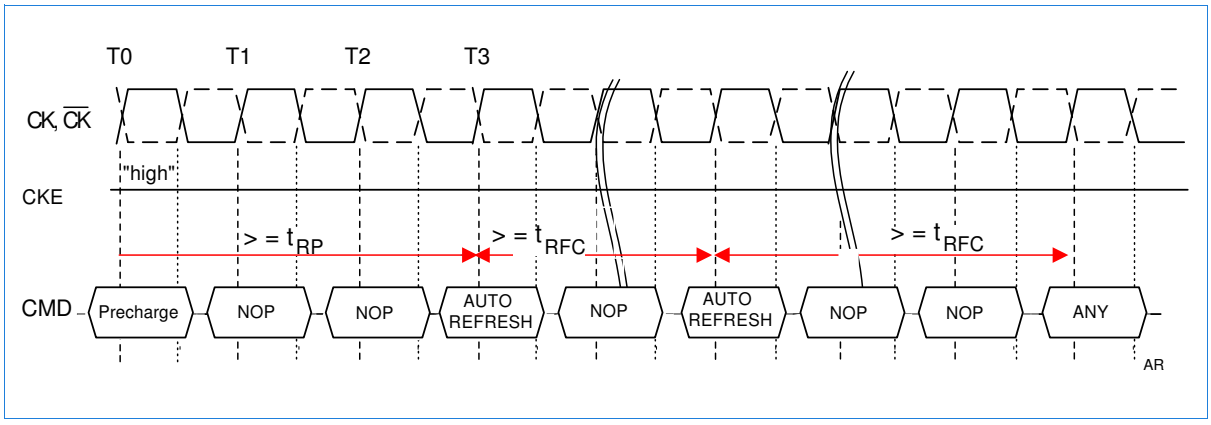
## Auto-Refresh Command

Auto-Refresh is used during normal operation of the DDR2 SDRAMs. This command is nonpersistent, so it must be issued each time a refresh is required. The refresh addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an Auto-Refresh command. The DDR2 SDRAM requires Auto-Refresh cycles at an average periodic interval of tREFI (maximum).

When $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ are held low and $\overline{WE}$ high at the rising edge of the clock, the chip enters the Auto-Refresh mode. All banks of the SDRAM must be precharged and idle for a minimum of the precharge time ($t_{RP}$) before the Auto-Refresh Command can be applied. An internal address counter supplies the addresses during the refresh cycle. No control of the external address bus is required once this cycle has started.

When the refresh cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the Auto-Refresh Command and the next Activate Command or subsequent Auto-Refresh Command must be greater than or equal to the Auto-Refresh cycle time ($t_{RFC}$).

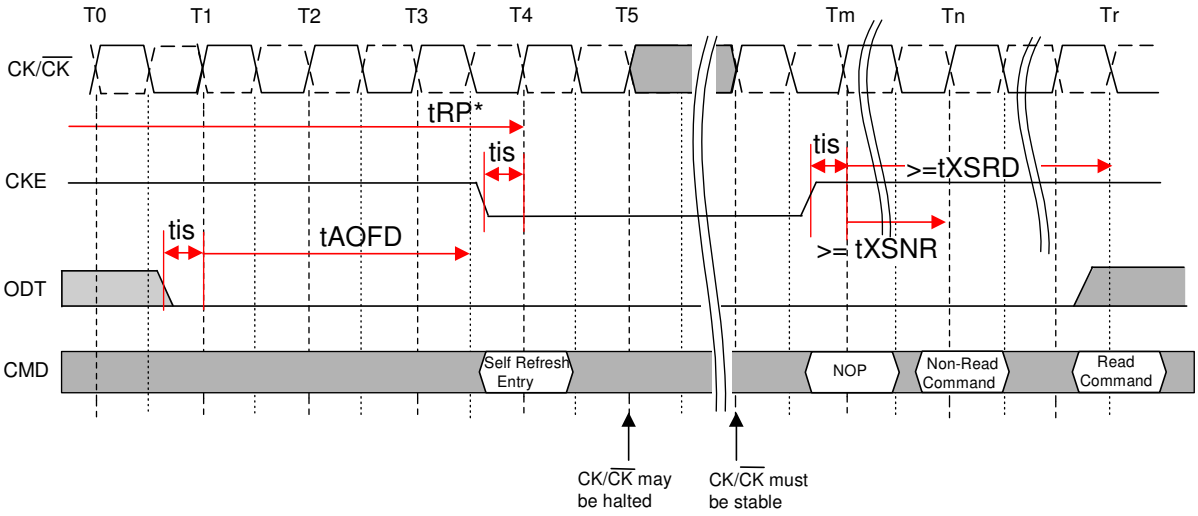
To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM, meaning that the maximum absolute interval between any Auto-Refresh command and the next Auto-Refresh command is 9 * tREFI.



## Self-Refresh Command

The Self-Refresh command can be used to retain data, even if the rest of the system is powered down. When in the Self-Refresh mode, the DDR2 SDRAM retains data without external clocking.

The DDR2 SDRAM device has a built-in timer to accommodate Self-Refresh operation. The Self-Refresh Command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE held low with $\overline{WE}$ high at the rising edge of the clock. ODT must be turned off before issuing Self Refresh command, by either driving ODT pin low or using EMRS(1) command. Once the command is registered, CKE must be held low to keep the device in Self-Refresh mode. When the DDR2 SDRAM has entered Self-Refresh mode all of the external control signals, except CKE, are disabled. The clock is internally disabled during Self-Refresh Operation to save power. The user may change the external clock frequency or halt the external clock one clock after Self-Refresh entry is registered, however, the clock must be restarted and stable before the device can exit Self-Refresh operation. Once Self-Refresh Exit command is registered, a delay equal or longer than the tXSNR or tXSRD must be satisfied before a valid command can be issued to the device. CKE must remain high for the entire Self-Refresh exit period (tXSNR or tXSRD) for proper operation. NOP or DESELECT commands must be registered on each positive clock edge during the Self-Refresh exit interval. Since the ODT function is not supported during Self-Refresh operation, ODT has to be turned off tAOFD before entering Self-Refresh Mode and can be turned on again when the tXSRD timing is satisfied.




* = Device must be in the "All banks idle" state to entering Self Refresh mode.
ODT must be turned off prior to entering Self Refresh mode.
tXSRD (>=200 tCK) has to be satisfied for a Read or a Read with Auto-Precharge command.
tXSNR has to be satisfied for any command except a Read or a Read with Auto-Precharge command, where tXSNR is defined as tRFC + 10ns.
The miminum CKE low time is defined by the $tCKE_{min.}$ timing parameter.
Since CKE is an SSTL input, VREF must be maintained during Self Refresh.

## Power-Down

Power-down is synchronously entered when CKE is registered low, along with NOP or Deselect command. CKE is not allowed to go low while mode register or extended mode register command time, or read or write operation is in progress. CKE is allowed to go low while any other operation such as row activation, Precharge, Auto-Precharge or Auto-Refresh is in progress, but power-down IDD specification will not be applied until finishing those operations.

The DLL should be in a locked state when power-down is entered. Otherwise DLL should be reset after exiting power-down mode for proper read operation.

If power-down occurs when all banks are precharged, this mode is referred to as *Precharge Power-down*; if power-down occurs when there is a row active in any bank, this mode is referred to as *Active Power-down*. For *Active Power-down* two different power saving modes can be selected within the MRS register, address bit A12. When A12 is set to "low" this mode is referred as "standard active power-down mode" and a fast power-down exit timing defined by the tXARD timing parameter can be used. When A12 is set to "high" this mode is referred as a power saving "low power active power-down mode". This mode takes longer to exit from the power-down mode and the tXARDS timing parameter has to be satisfied.
Entering power-down deactivates the input and output buffers, excluding CK, $\overline{CK}$, ODT and CKE. Also the DLL is disabled upon entering Precharge Power-down or slow exit active power-down, but the DLL is kept enabled during fast exit active power-down. In power-down mode, CKE low and a stable clock signal must be maintained at the inputs of the DDR2 SDRAM, and all other input signals are "Don't Care". Power-down duration is limited by 9 times tREFI of the device.

The power-down state is synchronously exited when CKE is registered high (along with a NOP or Deselect command). A valid, executable command can be applied with power-down exit latency, tXP, tXARD or tXARDS, after CKE goes high. Power-down exit latencies are defined in the AC spec table of this data sheet.

**Power-Down Entry**

*Active Power-down mode* can be entered after an activate command. *Precharge Power-down* mode can be entered after a precharge, Precharge-All or internal precharge command. It is also allowed to enter power-mode after an Auto-Refresh command or MRS / EMRS(1) command when tMRD is satisfied.

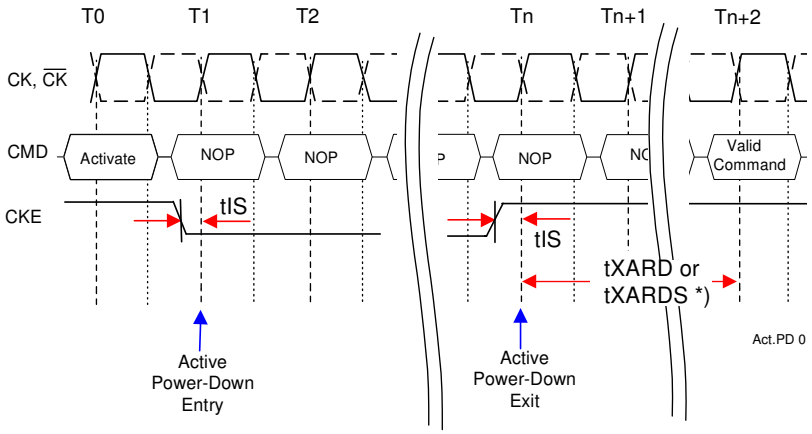
*Active Power-down mode* entry is prohibited as long as a Read Burst is in progress, meaning CKE should be kept high until the burst operation is finished. Therefore Active Power-Down mode entry after a Read or Read with Auto-Precharge command is allowed after RL + BL/2 is satisfied.

*Active Power-down mode* entry is prohibited as long as a Write Burst and the internal write recovery is in progress. In case of a write command, active power-down mode entry is allowed when WL + BL/2 + tWTR is satisfied.

In case of a write command with Auto-Precharge, Power-down mode entry is allowed after the internal precharge command has been executed, which is WL + BL/2 + WR starting from the write with Auto-Precharge command. In case the DDR2 SDRAM enters the *Precharge Power-down* mode.

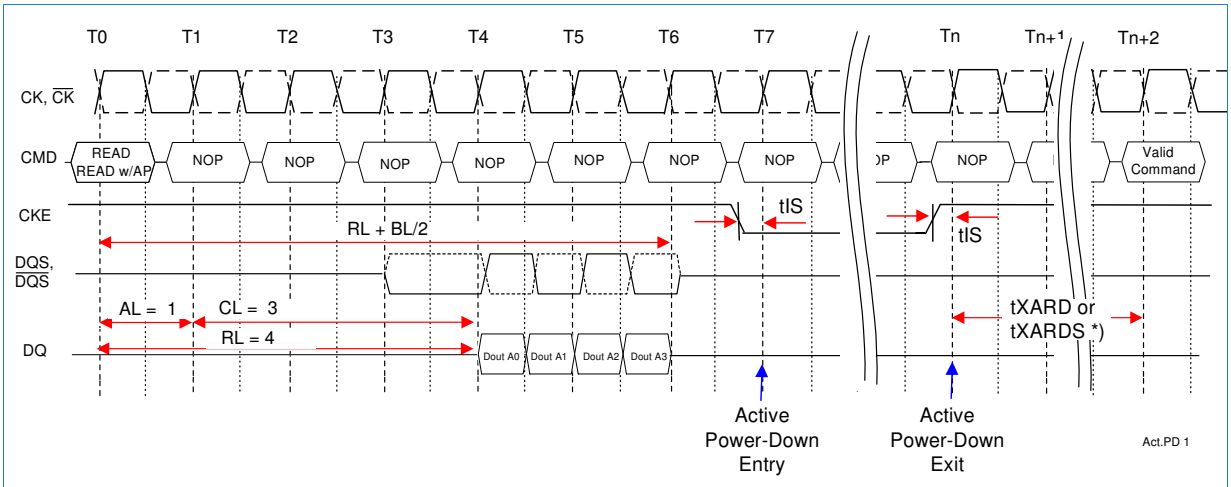
**Examples:**

**Active Power-Down Mode Entry and Exit after an Activate Command**



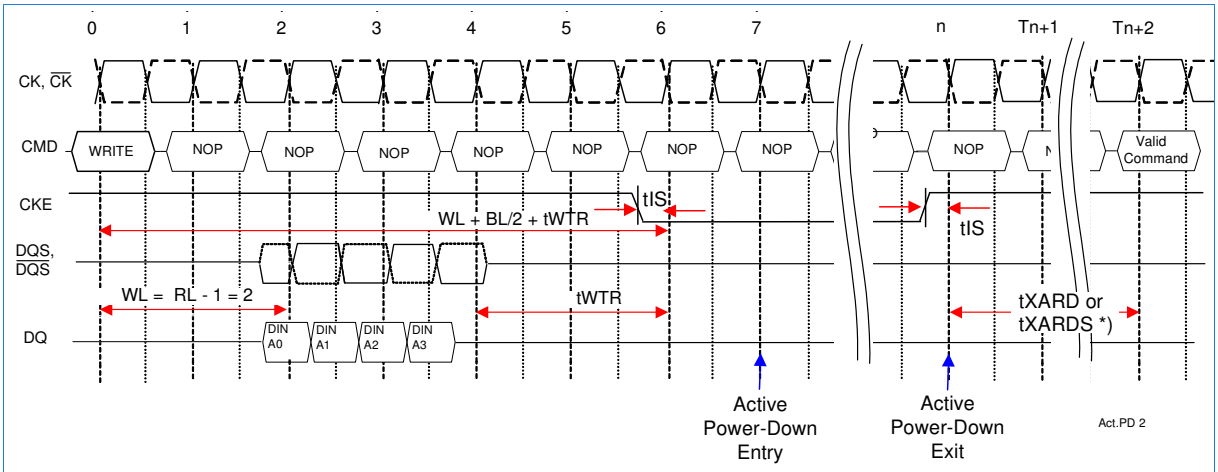

note: Active Power-Down mode exit timing tXARD ("fast exit") or tXARDS ("slow exit") depends on the programmed state in the MRS, address bit A12.

**Active Power-Down Mode Entry and Exit after a Read Burst: RL = 4 (AL = 1, CL =3), BL = 4**



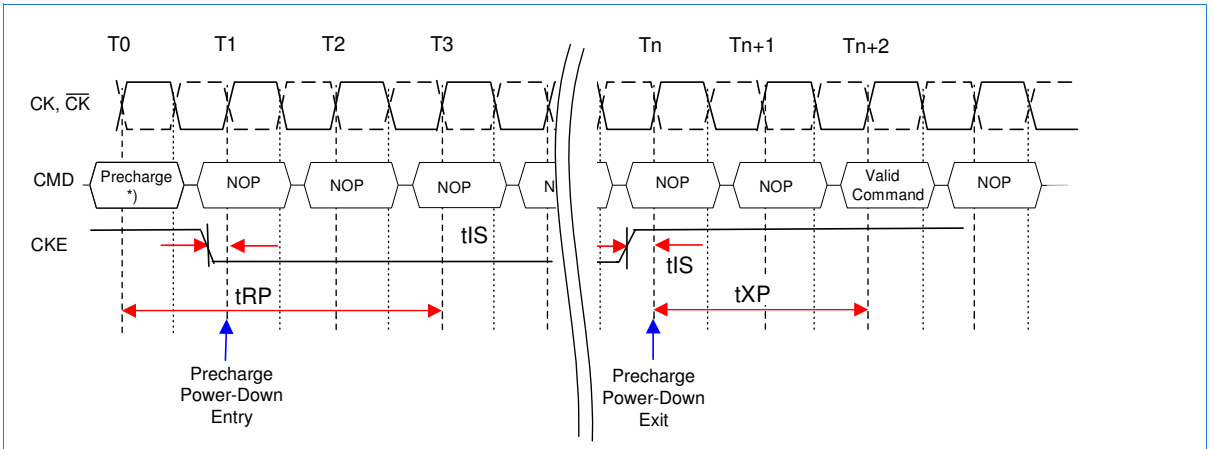

Note: Active Power-Down mode exit timing tXARD ("fast exit") or tXARDS ("slow exit") depends on the programmed state in the MRS, address bit A12.

### Active Power-Down Mode Entry and Exit after a Write Burst: WL = 2, tWTR = 2, BL = 4




Note: Active Power-Down mode exit timing tXARD ("fast exit") or tXARDS ("slow exit") depends on the programmed state in the MRS, address bit A12.

### Precharge Power Down Mode Entry and Exit




*) "Precharge" may be an external command or an internal precharge following Write with AP.

## No Operation Command

The No Operation Command should be used in cases when the SDRAM is in a idle or a wait state. The purpose of the No Operation Command is to prevent the SDRAM from registering any unwanted commands between operations. A No Operation Command is registered when $\overline{CS}$ is low with $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ held high at the rising edge of the clock. A No Operation Command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

## Deselect Command

The Deselect Command performs the same function as a No Operation Command. Deselect Command occurs when $\overline{CS}$ is brought high, the $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ signals become don't care.

## Input Clock Frequency Change

During operation the DRAM input clock frequency can be changed under the following conditions:

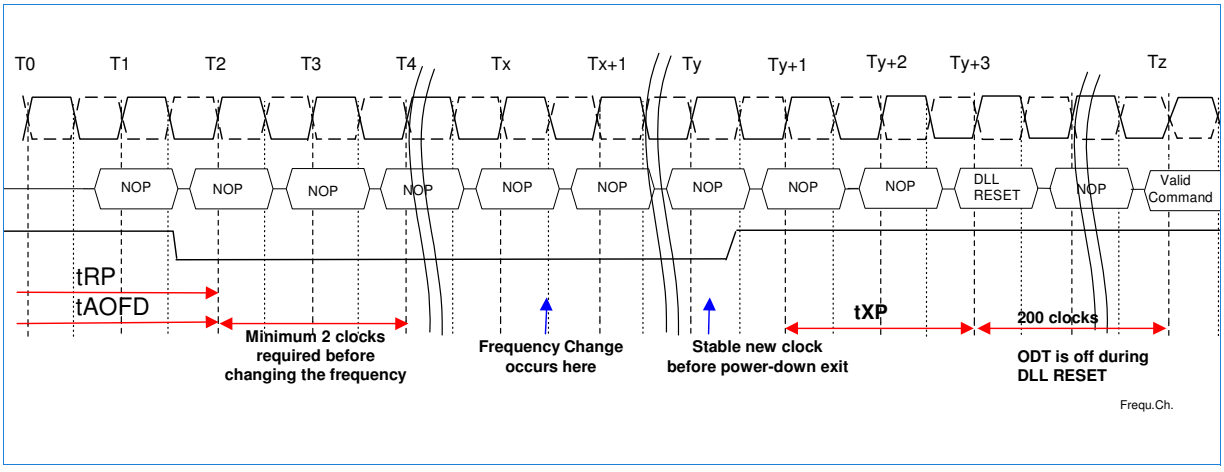
a) During Self-Refresh operation

b) DRAM is in Precharge Power-down mode and ODT is completely turned off.

The DDR2-SDRAM has to be in Precharged Power-down mode and idle. ODT must be allready turned off and CKE must be at a logic "low" state. After a minimum of two clock cycles after tRP and tAOFD have been satisfied the input clock frequency can be changed. A stable new clock frequency has to be provided, before CKE can be changed to a "high" logic level again. After tXP has been satisfied a DLL RESET command via EMRS(1) has to be issued. During the following DLL re-lock period of 200 clock cycles, ODT must remain off. After the DLL-re-lock period the DRAM is ready to operate with the new clock frequency.

**Example:**

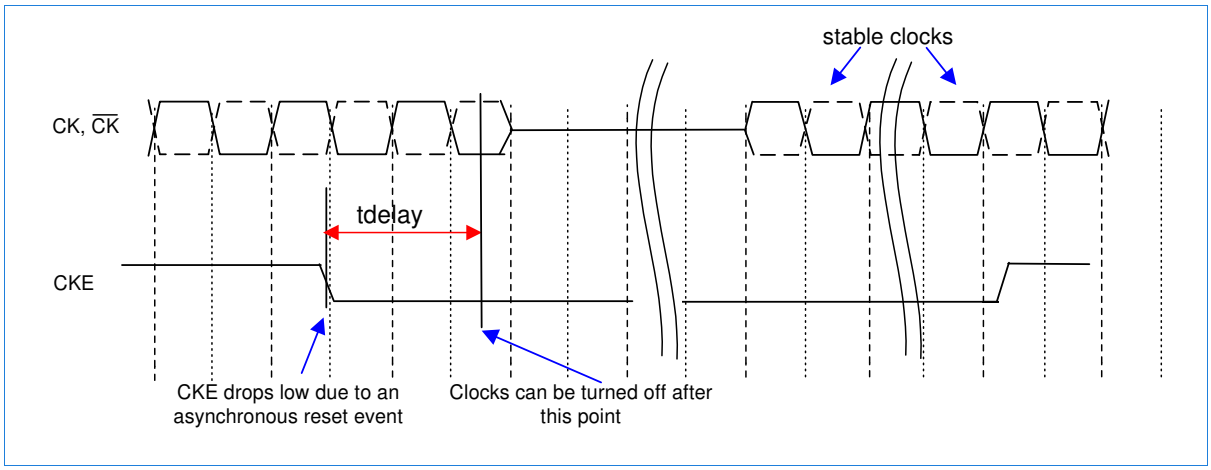
**Input frequency change during Precharge Power-Down mode**



## Asynchronous CKE Low Event

DRAM requires CKE to be maintained “high” for all valid operations as defined in this data sheet. If CKE asynchronously drops “low” during any valid operation DRAM is not guaranteed to preserve the contents of the memory array. If this event occurs, the memory controller must satisfy a time delay ( $t_{delay}$ ) before turning off the clocks. Stable clocks must exist at the input of DRAM before CKE is raised “high” again. The DRAM must be fully re-initialized as described the the initialization sequence (section 2.2.1, step 4 thru 13). DRAM is ready for normal operation after the initialization sequence. See AC timing parametric table for $t_{delay}$ specification.

### Asynchronous CKE Low Event



## Truth Table

## Command Truth Table

| Function | CKE | | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | BA0 BA1 | A13-A11 | A10 | A9 - A0 | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Previous Cycle | Current Cycle | | | | | | | | | |
| (Extended) Mode Register Set | H | H | L | L | L | L | BA | OP Code | | | 1, 2 |
| Auto-Refresh | H | H | L | L | L | H | X | X | X | X | 1 |
| Self-Refresh Entry | H | L | L | L | L | H | X | X | X | X | 1 |
| Self-Refresh Exit | L | H | H | X | X | X | X | X | X | X | 1 |
| Single Bank Precharge | H | H | L | L | H | L | BA | X | L | X | 1,2 |
| Precharge all Banks | H | H | L | L | H | L | X | X | H | X | 1 |
| Bank Activate | H | H | L | L | H | H | BA | Row Address | | | 1, 2 |
| Write | H | H | L | H | L | L | BA | Column | L | Column | 1,2,3 |
| Write with Auto-Precharge | H | H | L | H | L | L | BA | Column | H | Column | 1,2,3 |
| Read | H | H | L | H | L | H | BA | Column | L | Column | 1,2,3 |
| Read with Auto-Precharge | H | H | L | H | L | H | BA | Column | H | Column | 1,2,3 |
| No Operation | H | X | L | H | H | H | X | X | X | X | 1 |
| Device Deselect | H | X | H | X | X | X | X | X | X | X | 1 |
| Power Down Entry | H | L | H | X | X | X | X | X | X | X | 1,4 |
| | | | L | H | H | H | | | | | |
| Power Down Exit | L | H | H | X | X | X | X | X | X | X | 1,4 |
| | | | L | H | H | H | | | | | |

1. All DDR2 SDRAM commands are defined by states of $\overline{CS}$, $\overline{WE}$, $\overline{RAS}$, $\overline{CAS}$, and CKE at the rising edge of the clock.
2. Bank addresses (BAx) determine which bank is to be operated upon. For (E)MRS BxA selects an (Extended) Mode Register.
3. Burst reads or writes at BL = 4 cannot be terminated. See sections “Reads interrupted by a Read” and “Writes interrupted by a Write” insection 2.4.6 for details.
4. The Power Down Mode does not perform any refresh operations. The duration of Power Down is therefore limited by the refresh requirements outlined in section 2.7.
5. The state of ODT does not affect the states decribed in this table. The ODT function is not available during Self Refresh.
6. “X” means “H or L (but a defined logic level)”.
7. Operation that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restartet through the specified initialization sequence before normal operation can continue.

## Clock Enable (CKE) Truth Table for Synchronous Transistions

| Current State[2] | CKE | | Command (N) [3,12] | Action (N) [3] | Notes |
|---|---|---|---|---|---|
| | Previous Cycle [1] (N-1) | Current Cycle [1] (N) | $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$ | | |
| Power-Down | L | L | X | Maintain Power-Down | 11, 13, 15 |
| | L | H | DESELECT or NOP | Power-Down Exit | 4, 8, 11, 13 |
| Self Refresh | L | L | X | Maintain Self Refresh | 11, 15 |
| | L | H | DESELECT or NOP | Self Refresh Exit | 4, 5, 9 |
| Bank(s) Active | H | L | DESELECT or NOP | Active Power-Down Entry | 4,8,10,11, 13 |
| All Banks Idle | H | L | DESELECT or NOP | Precharge Power-Down Entry | 4,8,10,11 |
| | H | L | AUTOREFRESH | Self Refresh Entry | 6, 9, 11, 13 |
| Any State other than listed above | H | H | Refer to the Command Truth Table | | 7 |

1. CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR2 SDRAM immediately prior to clock edge N.
3. Command (N) is the command registered at clock edge N, and Action (N) is a result of Command (N).
4. All states and sequences not shown are illegal or reserved unless explicitely described elsewhere in this document.
5. On Self Refresh Exit DESELECT or NOP commands must be issued on every clock edge occuring during the tXSNR period.
   Read commands may be issued only after tXSRD (200 clocks) is satisfied.
6. Self Refresh mode can only be entered from the All Banks Idle state.
7. Must be a legal command as defined in the Command Truth Table.
8. Valid commands for Power-Down Entry and Exit are NOP and DESELECT only.
9. Valid commands for Self Refresh Exit are NOP and DESELCT only.
10. Power-Down and Self Refresh can not be entered while Read or Write operations, (Extended) mode Register operations, Precharge or Refresh operations are in progress. See section 2.8 “Power Down” and section 2.7.2 “Self Refresh Command” for a detailed list of restrictions.
11. Minimum CKE high time is 3 clocks, minimum CKE low time is 3 clocks.
12. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
13. The Power-Down Mode does not perform any refresh operations. The duration of Power-Down Mode is therefor limited by the refresh requirements.
14. CKE must be maintained high while the device is in OCD calibration mode.
15. “X” means “don’t care (including floating around VREF)” in Self Refresh and Power Down. However ODT must be driven high or low in Power Down if the ODT function is enabled (Bit A2 or A6 set to “1” in EMRS(1)).
16. Operation that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restartet through the specified initialization sequence before normal operation can continue.

## Data Mask (DM) Truth Table

| Name (Function) | DM | DQs | Notes |
|---|---|---|---|
| Write Enable | L | Valid | 1 |
| Write Inhibit | H | X | 1 |

1. Used to mask write data; provided coincident with the corresponding data.

## Operating Conditions

### Absolute Maximum Ratings

| Symbol | Parameter | Rating | Units | Notes |
|---|---|---|---|---|
| VDD | Voltage on VDD pin relative to VSS | -1.0 to + 2.3 | V | 1 |
| VDDQ | Voltage on VDDQ pin relative to VSS | -0.5 to + 2.3 | V | 1 |
| VDDL | Voltage on VDDL pin relative to VSS | -0.5 to + 2.3 | V | 1 |
| $V_{IN}$, $V_{OUT}$ | Voltage on any pin relative to VSS | -0.5 to + 2.3 | V | 1 |
| $T_{STG}$ | Storage Temperature | -55 to + 100 | °C | 1, 2 |

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

### DRAM Component Operating Temperature Range

| Symbol | Parameter | Rating | Units | Notes |
|---|---|---|---|---|
| $T_{OPER}$ | Operating Temperature | 0 to 85 | °C | 1, 2 |

1. Operating Temperature is the case surface temperature on the center / top side of the DRAM.
2. The operating temperature range are the temperatures where all DRAM specification will be supported. During operation, the DRAM case temperature must be maintained between 0 - 85°C under all other specifcation parameters.
3. Outside of this temperature range, even it is still within the limit of stress condition, some deviation on portion of operation specification may be required.
4. Some application may require to operate the DRAM up to 95°C case temperature. In this case above 85°C case temperature the Auto-Refresh command frequency has to be reduced to tREFI = 3.9 µs and some AC timing parameter will reach or exceed their specified limit values.
5. Self-Refresh period is hard-coded in the chip and therefore it is imperative that the system ensures the DRAM is below 85°C case temperature before initiating self-refresh operation.

# AC & DC Operating Conditions

## DC Operating Conditions

### Recommended DC Operating Conditions (SSTL_18)

| Symbol | Parameter | Rating | | | Units | Notes |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| VDD | Supply Voltage | 1.7 | 1.8 | 1.9 | V | 1 |
| VDDDL | Supply Voltage for DLL | 1.7 | 1.8 | 1.9 | V | 1 |
| VDDQ | Supply Voltage for Output | 1.7 | 1.8 | 1.9 | V | 1 |
| VREF | Input Reference Voltage | 0.49 * VDDQ | 0.5 * VDDQ | 0.51 * VDDQ | V | 2, 3 |
| VTT | Termination Voltage | VREF - 0.04 | VREF | VREF + 0.04 | V | 4 |

1. VDDQ tracks with VDD, VDDDL tracks with VDD. AC parameters are measured with VDD, VDDQ and VDDDL tied together.
2. The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.
3. Peak to peak ac noise on VREF may not exceed +/- 2% VREF (dc).
4. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF and must track variations in die dc level of VREF.

### ODT DC Electrical Characteristics:

| Parameter / Condition | Symbol | min. | nom. | max. | Units | Notes |
|---|---|---|---|---|---|---|
| Rtt eff. impedance value for EMRS(1)(A6,A2)=0,1; 75 ohm | Rtt1(eff) | 60 | 75 | 90 | ohm | 1 |
| Rtt eff. impedance value for EMRS(1)(A6,A2)=1,0; 150 ohm | Rtt2(eff) | 120 | 150 | 180 | ohm | 1 |
| Rtt eff. impedance value for EMRS(1)(A6,A2)=1,1; 50 ohm | Rtt3(eff) | 40 | 50 | 60 | ohm | 1 |
| Deviation of VM with respect to VDDQ / 2 | delta VM | - 6 | | + 6 | % | 2 |

1) Measurement Definition for Rtt(eff):
Apply VIHac and VILac to test pin seperately, then measure current I(VIHac) and I(VILac) respectively.

$$Rtt(eff) = (VIHac - VILac) / ( I(VIHac) - I(VILac))$$

2) Measurement Defintion for VM:
Measure voltage (VM) at test pin (midpoint) with no load:

$$delta\ VM = (( 2* VM / VDDQ) - 1 ) \times 100\%$$

## DC & AC Logic Input Levels

DDR2 SDRAM pin timing are specified for either single ended or differential mode depending on the setting of the EMRS(1) "Enable $\overline{DQS}$" mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timing are measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at VREF. In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, $\overline{DQS}$. This distinction in timing methods is guaranteed by design and characterisation. In single ended mode, the $\overline{DQS}$ (and $\overline{RDQS}$) signals are internally disabled and don't care.

### Single-ended DC & AC Logic Input Levels

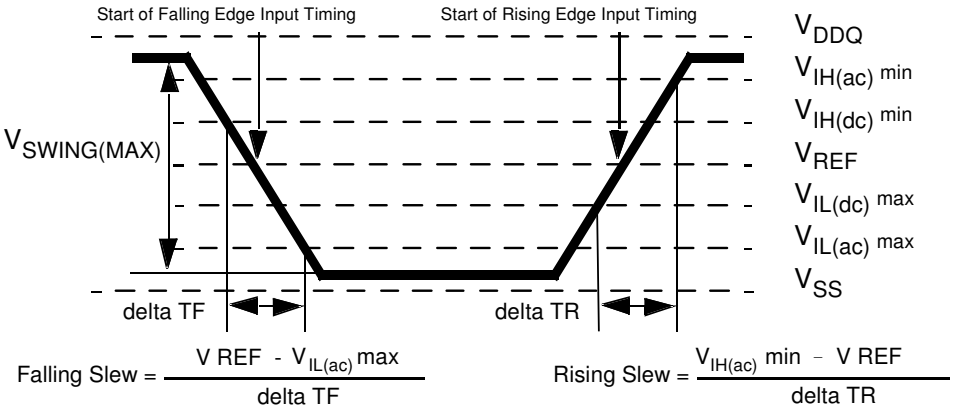
| Symbol | Parameter | Min. | Max. | Units | Note |
|---|---|---|---|---|---|
| VIH (dc) | DC input logic high | VREF + 0.125 | VDDQ + 0.3 | V | |
| VIL (dc) | DC input logic low | - 0.3 | VREF - 0.125 | V | |
| VIH (ac) | AC input logic high | VREF + 0.250 | - | V | 1 |
| VIL (ac) | AC input logic low | - | VREF - 0.250 | V | 2 |

Note1: DDR2-400/533 Min: VREF + 0.250V; DDR2-667 Min: VREF + 0.200V
Note2: DDR2-400/533 Max: VREF - 0.250V; DDR2-667 Max: VREF - 0.200V

### Single-ended AC Input Test Conditions

| Symbol | Condition | Value | Units | Notes |
|---|---|---|---|---|
| VREF | Input reference voltage | 0.5 * VDDQ | V | 1, 2 |
| VSWING(max) | Input signal maximum peak to peak swing | 1.0 | V | 1, 2 |
| SLEW | Input signal minimum slew rate | 1.0 | V / ns | 3, 4 |

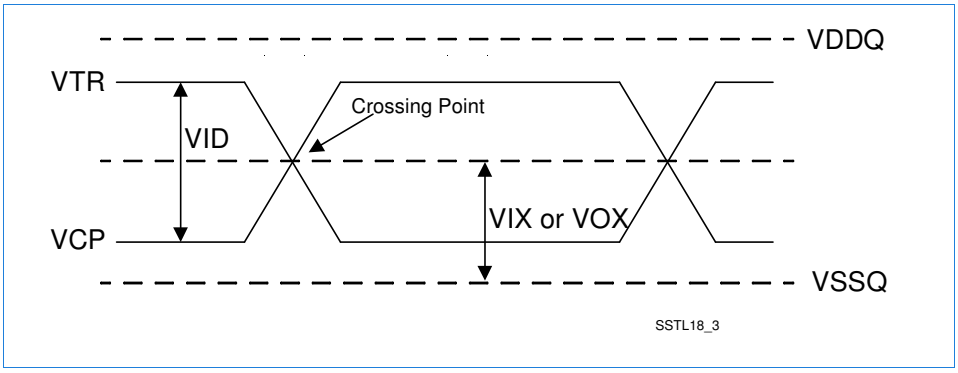
1. This timing and slew rate definition is valid for all single-ended signls execpt tis, tih, tds, tdh.
2. Input waveform timing is referenced to the input signal crossing through the VREF level applied to the device under test.
3. The input signal minimum slew rate is to be maintained over the range from VIL(dc)max to VIH(ac)min for rising edges and the range from VIH(dc)min to VIL(ac)max for falling edges as shown in the below figure.
4. AC timings are referenced with input waveforms switching from VIL(ac) to VIH(ac) on the positive transitions and VIH(ac) to VIL(ac) on the negative transitions.



## Differential DC and AC Input and Output Logic Levels

| Symbol | Parameter | min. | max. | Units | Notes |
|---|---|---|---|---|---|
| VID(ac) | AC differential input voltage | 0.5 | VDDQ + 0.6 | V | 3 |
| VIX(ac) | AC differential cross point input voltage | 0.5 * VDDQ - 0.175 | 0.5 * VDDQ + 0.175 | V | 4 |
| VOX(ac) | AC differential cross point output voltage | 0.5 * VDDQ - 0.125 | 0.5 * VDDQ + 0.125 | V | 5 |

notes:
1) VIN(dc) specifies the allowable DC execution of each input of differential pair such as CK, $\overline{CK}$, DQS, $\overline{DQS}$,etc.
2) VID(dc) specifies the input differential voltage VTR - VCP required for switching. The minimum value is equal to VIH(dc) - VIL(dc).
3) VID(ac) specifies the input differential voltage VTR - VCP required for switching. The minimum value is equal to VIH(ac) - VIL(ac).
4) The value of VIX(ac) is expected to equal 0.5 x VDDQ of the transmitting device and VIX(ac) is expected to track variations in VDDQ. VIX(ac) indicates the voltage at which differential input signals must cross.
5) The value of VOX(ac) is expected to equal 0.5 x VDDQ of the transmitting device and VOX(ac) is expected to track variations in VDDQ. VOX(ac) indicates the voltage at which differential input signals must cross.



# Output Buffer Levels

## Output AC Test Conditions

| Symbol | Parameter | SSTL_18 Class II | Units | Notes |
|---|---|---|---|---|
| $V_{OTR}$ | Output Timing Measurement Reference Level | 0.5 * $V_{DDQ}$ | V | 1 |

1. The VDDQ of the device under test is referenced.

## Output DC Current Drive

| Symbol | Parameter | Class II | Units | Notes |
|---|---|---|---|---|
| $I_{OH}$ | Output Minimum Source DC Current, nominal | -13.4 | mA | 1, 3, 4 |
| $I_{OL}$ | Output Minimum Sink DC Current, nominal | 13.4 | mA | 2, 3, 4 |

1. VDDQ = 1.7 V ; $V_{OUT}$ = 1.42 V. ($V_{OUT}$-VDDQ) / IOH must be less than 21 ohm for values of $V_{OUT}$ between VDDQ and VDDQ - 280 mV.
2. VDDQ = 1.7 V ; $V_{OUT}$ = 280 mV. $V_{OUT}$ / IOL must be less than 21 ohm for values of VOUT between 0V and 280 mV.
3. The dc value of VREF applied to the receiving device is set to VTT
4. The values of $I_{OH}$(dc) and $I_{OL}$(dc) are based on the conditions given in note 1 and 2. They are used to test drive current capability to ensure VIHmin. plus a noise margin and VILmax. minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating points along 21 ohm load line to define a convenient current for measurement.

## OCD Default Setting Table

| Symbol | Description | min. | nominal | max. | Unit | Notes |
|---|---|---|---|---|---|---|
| - | Pull-up / Pull down mismatch | 0 | - | 4 | Ohms | 1,2, 3 |
| - | Output Impedance step size for OCD calibration | 0 | | 1.5 | Ohms | 6 |
| Sout | Output Slew Rate | 1.5 | - | 5 | V / ns | 1, 4, 5 |

1) Absolute Specification: 0 $^{o}$C <$T_{CASE}$ <85$^{o}$C ; $V_{DDQ}$ = 1.8V ± 0.1V; $V_{DD}$ = 1.8V ± 0.1V.
2) Impedance measurement condition for output source dc current : VDDQ = 1.7V, VOUT = 1420 mV; (VOUT-VDDQ)/IOH must be less than 23.4 ohms for values of VOUT between VDDQ and VDDQ-280mV. Impedance measurement condition for output sink dc current : VDDQ = 1.7 V; VOUT = -280mV; VOUT / IOL must be less than 23.4 ohms for values of VOUT between 0V and 280 mV.
3) Mismatch is absolute value between pull-up and pull-down, both are measured at same temperature and voltage.
4) Slew rates measured from Vil(AC) to Vih(AC) with the load specified in Section 8.2.
5) The absolute value of the slew rate as measured from DC to DC is equal to or greater than the slew rate as measured from AC to AC. This is guaranteed by design and characterisation.
6) This represents the step size when the OCD is near 18 ohms at nominal conditions across all process corners/variations and represents only the DRAM uncertainty. A 0 ohm value (no valibration) can only be achieved if the OCD impedance is 18 ohms +/- 0.75 ohms under nominal conditions.

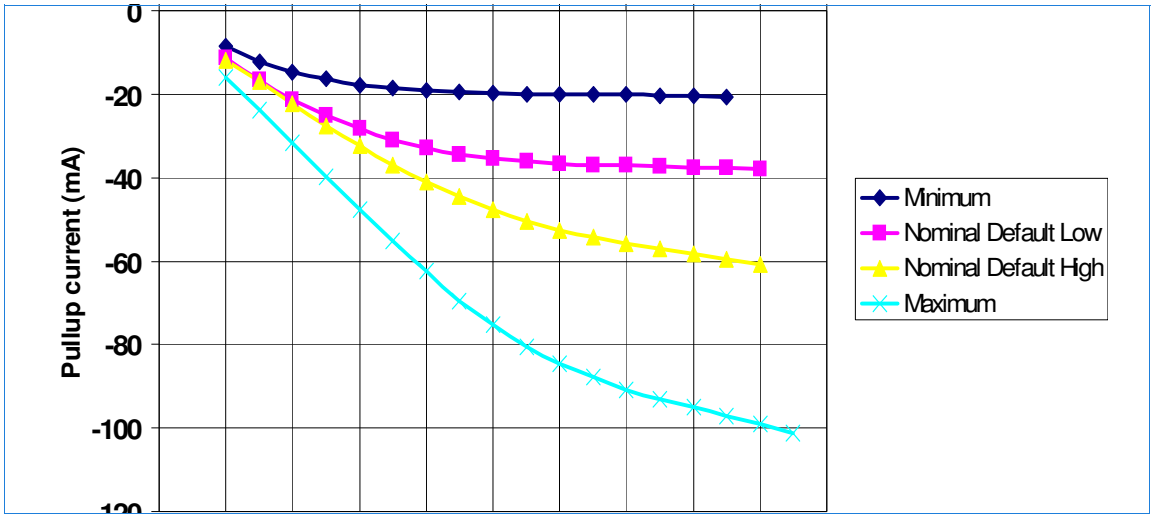
## Default Output V-I Characteristics

DDR2 SDRAM output driver characteristics are defined for full strength default operation as selected by the EMRS(1) bits A7~A9 = '111'. Figures  in Section 5.3.5 and 5.3.6 show the driver characteristics graphically and the tables sow the same data suitable for input into simulation tools.

### Full Strength Default Pullup Driver Characteristics

| Voltage (V) | Minimum (23.4 Ohms) | Nomal Default low (18 Ohms) | Nomal Default high (18 Ohms) | Maximum (12.6 Ohms) |
|---|---|---|---|---|
| 0.2 | -8.5 | -11.1 | -11.8 | -15.9 |
| 0.3 | -12.1 | -16.0 | -17.0 | -23.8 |
| 0.4 | -14.7 | -20.3 | -22.2 | -31.8 |
| 0.5 | -16.4 | -24.0 | -27.5 | -39.7 |
| 0.6 | -17.8 | -27.2 | -32.4 | -47.7 |
| 0.7 | -18.6 | -29.8 | -36.9 | -55.0 |
| 0.8 | -19.0 | -31.9 | -40.8 | -62.3 |
| 0.9 | -19.3 | -33.4 | -44.5 | -69.4 |
| 1.0 | -19.7 | -34.6 | -47.7 | -75.3 |
| 1.1 | -19.9 | -35.5 | -50.4 | -80.5 |
| 1.2 | -20.0 | -36.2 | -52.5 | -84.6 |
| 1.3 | -20.1 | -36.8 | -54.2 | -87.7 |
| 1.4 | -20.2 | -37.2 | -55.9 | -90.8 |
| 1.5 | -20.3 | -37.7 | -57.1 | -92.9 |
| 1.6 | -20.4 | -38.0 | -58.4 | -94.9 |
| 1.7 | -20.6 | -38.4 | -59.6 | -97.0 |
| 1.8 | | -38.6 | -60.8 | -99.1 |
| 1.9 | | | | -101.1 |

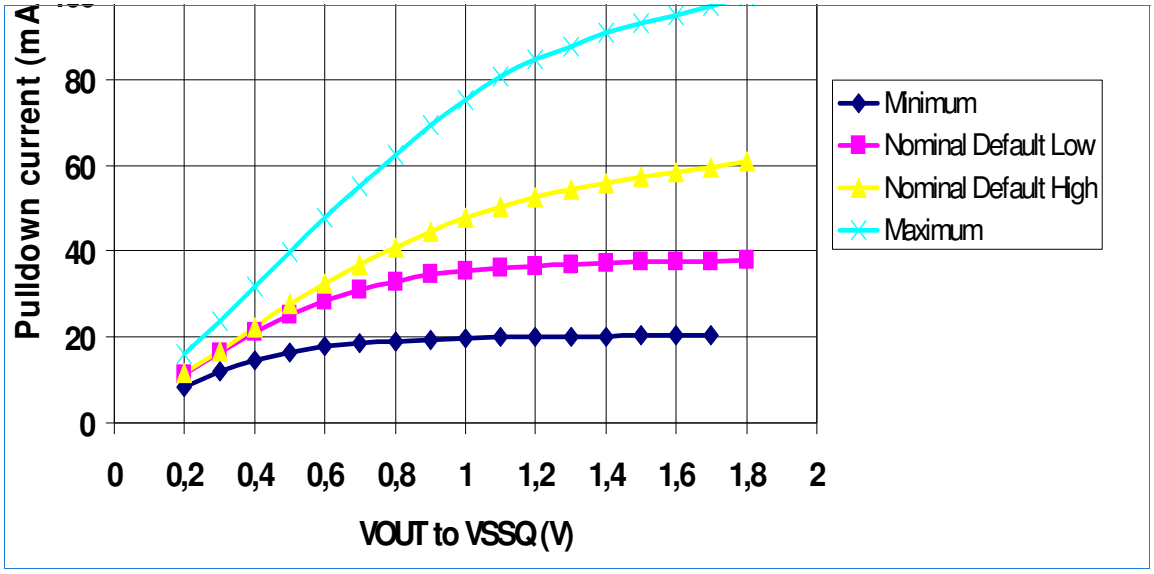
The driver characteristics evaluetion conditions are:
Nominal Default 25°C (Tcase) , VDDQ = 1.8 V, typical process
Minimum Toper(max.), VDDQ = 1.7V, slow-slow process
Maximum 0 °C (Tcase). VDDQ = 1.9 V, fast-fast process



## Full Strength Default Pulldown Driver Characteristics

| Voltage (V) | Minimum (23.4 Ohms) | Nomal Default low (18 Ohms) | Nomal Default high (18 Ohms) | Maximum (12.6 Ohms) |
|---|---|---|---|---|
| 0.2 | 8.5 | 11.3 | 11.8 | 15.9 |
| 0.3 | 12.1 | 16.5 | 16.8 | 23.8 |
| 0.4 | 14.7 | 21.2 | 22.1 | 31.8 |
| 0.5 | 16.4 | 25.0 | 27.6 | 39.7 |
| 0.6 | 17.8 | 28.3 | 32.4 | 47.7 |
| 0.7 | 18.6 | 30.9 | 36.9 | 55.0 |
| 0.8 | 19.0 | 33.0 | 40.9 | 62.3 |
| 0.9 | 19.3 | 34.5 | 44.6 | 69.4 |
| 1.0 | 19.7 | 35.5 | 47.7 | 75.3 |
| 1.1 | 19.9 | 36.1 | 50.4 | 80.5 |
| 1.2 | 20.0 | 36.6 | 52.6 | 84.6 |
| 1.3 | 20.1 | 36.9 | 54.2 | 87.7 |
| 1.4 | 20.2 | 37.1 | 55.9 | 90.8 |
| 1.5 | 20.3 | 37.4 | 57.1 | 92.9 |
| 1.6 | 20.4 | 37.6 | 58.4 | 94.9 |
| 1.7 | 20.6 | 37.7 | 59.6 | 97.0 |
| 1.8 | | 37.9 | 60.9 | 99.1 |
| 1.9 | | | | 101.1 |

The driver characteristics evaluetion conditions are:
Nominal Default 25°C (Tcase) , VDDQ = 1.8 V, typical process
Minimum Toper(max), VDDQ = 1.7V, slow-slow process
Maximum 0 °C (Tcase). VDDQ = 1.9 V, fast-fast process



## Calibrated Output Driver V-I Characteristics

DDR2 SDRAM output driver characteristics are defined for full strength calibrated operation as selected by the procedure outlined in the Off-Chip Driver (OCD) Impedance Adjustment. The following tables show the data in tabular format suitable for input into simulation tools. The nominal points represent a device at exactly 18 ohms. The nominal low and nominal high values represent the range that can be achieved with a maximum 1.5 ohms step size with no calibration error at the exact nominal conditions only (i.e. perfect calibration procedire, 1.5 ohm maximum step size guarantedd by specification). Real system calibration error needs to be added to these values. It must be understodd that these V-I curves are represented here or in supplier IBIS models need to be adjusted to a wider range as a result of any system calibration error. Since this a system specific phenomena, it cannot be quantified here. the values in the calibrated tables represent just the DRAM portion of uncertainty while looking at one DQ only. If the calibration procedure is used, it is possible to cause the device to operate outside the bounds of the default device characterisitcs tables and figure. in such a situation, the timing paramters in the specification cannot be guaranteed. It is solely up to the system application to ensure that the device is calibrated between the minimum and maximum default values at all times. If this can't be guaranteed by the system calibration procedure, recalibration policy and uncertainty with DQ to DQ variation, the it is recommende that only the default values to be used. The nominal maximum ad minmum values represent the change in impedance from nominal low and high as a result of voltage and temperature change from the nominal condition to the maximum and minimum conditions. If calibrated at an extreme condition, the amount of variation could be as much as from the nominal minimum to the nominal maximum or vice versa.

### Full Strength Calibrated Pulldown Driver Characteristics

| Voltage (V) | Nominal Minimum (21 Ohms) | Nomal Low (18.75 Ohms) | Nominal (18 ohms) | Nomal High (17.25 Ohms) | Nominal Maximum (15 Ohms) |
|---|---|---|---|---|---|
| 0.2 | 9.5 | 10.7 | 11.5 | 11.8 | 13.3 |
| 0.3 | 14.3 | 16.0 | 16.6 | 17.4 | 20.0 |
| 0.4 | 18.7 | 21.0 | 21.6 | 23.0 | 27.0 |
| The driver characteristics evaluetion conditions are:<br>Nominal 25°C (Tcase) , VDDQ = 1.8 V, typical process<br>Nominal Low and Nominal High 25°C (Tcase), VDDQ = 1.8V, any process<br>Nominal Minimum Toper(max), VDDQ = 1.7 V, any process<br>Nominal Maximum 0°C (Tcase), VDDQ = 1.9 V, any process | | | | | |

### Full Strength Calibrated Pullup Driver Characteristics

| Voltage (V) | Nominal Minimum (21 Ohms) | Nomal Low (18.75 Ohms) | Nominal (18 ohms) | Nomal High (17.25 Ohms) | Nominal Maximum (15 Ohms) |
|---|---|---|---|---|---|
| 0.2 | -9.5 | -10.7 | -11.4 | -11.8 | -13.3 |
| 0.3 | -14.3 | -16.0 | -16.5 | -17.4 | -20.0 |
| 0.4 | -18.3 | -21.0 | -21.2 | -23.0 | -27.0 |
| The driver characteristics evaluetion conditions are:<br>Nominal 25°C (Tcase) , VDDQ = 1.8 V, typical process<br>Nominal Low and Nominal High 25°C (Tcase), VDDQ = 1.8V, any process<br>Nominal Minimum Toper(max), VDDQ = 1.7 V, any process<br>Nominal Maximum 0°C (Tcase), VDDQ = 1.9 V, any process | | | | | |

## Input / Output Capacitance

| Symbol | Parameter | min. | max. | Units | Note |
|---|---|---|---|---|---|
| CCK | Input capacitance, CK and $\overline{CK}$ | 1.0 | 2.0 | pF | |
| CDCK | Input capacitance delta, CK and $\overline{CK}$ | - | 0.25 | pF | |
| CI | Input capacitance, all other input-only pins | 1.0 | 2.0 | pF | |
| CDI | Input capacitance delta, all other input-only pins | - | 0.25 | pF | |
| CIO | Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$ | 3.0 | 4.0/3.5 | pF | 1 |
| CDIO | Input/output capacitance delta, DQ, DM, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$ | - | 0.5 | pF | |
| Note1: DDR2-400/533 CIO max. 4.0pF; DDR2-667 CIO max 3.5pF | | | | | |

## Power & Ground Clamp V-I Characteristics

Power and Ground clamps are provided on address (A0~A13, BA0, BA1), $\overline{RAS}$, $\overline{CAS}$, $\overline{CS}$, $\overline{WE}$, CKE and ODT pins. The V-I characterisitcs for pins with clamps is shown in the following table :

| Voltage across clamp (V) | Minimum Power Clamp Current (mA) | Minimum Ground Clamp Current (mA) |
|---|---|---|
| 0.0 | 0 | 0 |
| 0.1 | 0 | 0 |
| 0.2 | 0 | 0 |
| 0.3 | 0 | 0 |
| 0.4 | 0 | 0 |
| 0.5 | 0 | 0 |
| 0.6 | 0 | 0 |
| 0.7 | 0 | 0 |
| 0.8 | 0.1 | 0.1 |
| 0.9 | 1.0 | 1.0 |
| 1.0 | 2.5 | 2.5 |
| 1.1 | 4.7 | 4.7 |
| 1.2 | 6.8 | 6.8 |
| 1.3 | 9.1 | 9.1 |
| 1.4 | 11.0 | 11.0 |
| 1.5 | 13.5 | 13.5 |
| 1.6 | 16.0 | 16.0 |
| 1.7 | 18.2 | 18.2 |
| 1.8 | 21.0 | 21.0 |

# IDD Specifications and Measurement Conditions

## IDD Specifications

( VDDQ = 1.8V ± 0.1V; VDD = 1.8V ± 0.1V)

| Symbol | Parameter/Condition | | I/O | -5A DDR2 -400 | -37B DDR2 -533 | -3C DDR2 -667 | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| | | | | max. | max. | max. | | |
| IDD0 | Operating Current | | x4/ x8<br>x16 | 65<br>70 | 70<br>80 | 75<br>95 | mA | 1, 2 |
| IDD1 | Operating Current | | x4/ x8<br>x16 | 70<br>75 | 80<br>95 | 90<br>110 | mA | 1, 2 |
| IDD2P | Precharge Power-Down Current | | all | 5 | 5 | 5 | mA | 1, 2 |
| IDD2N | Precharge Standby Current | | all | 32 | 40 | 50 | mA | 1, 2 |
| IDD2Q | Precharge Quiet Standby Current: | | all | 25 | 30 | 40 | mA | 1, 2 |
| IDD3P | Active Power-Down Standby Current | MRS(12)=0 | all | 13 | 16 | 19 | mA | 1, 2 |
| | | MRS(12)=1 | all | 5 | 5 | 6 | mA | 1, 2 |
| IDD3N | Active Standby Current | | all | 35 | 42 | 50 | mA | 1, 2 |
| IDD4R | Operating Current Burst Read | | x4/x8<br>x16 | 80<br>95 | 90<br>130 | 130<br>150 | mA | 1, 2 |
| IDD4W | Operating Current Burst Write | | x4/x8<br>x16 | 75<br>95 | 95<br>130 | 140<br>170 | mA | 1, 2 |
| IDD5B | Burst Auto-Refresh Current (tRFC=tRFCmin) | | all | 130 | 150 | 160 | mA | 1, 2 |
| IDD5D | Distributed Auto-Refresh Current (tRFC=tREFI) | | all | 6 | 6 | 6 | mA | 1, 2 |
| IDD6 | Self-Refresh Current for standard products | | all | 5 | 5 | 5 | mA | 1, 2 |
| IDD7 | Operating Current | | x4/x8<br>x16 | 150<br>210 | 160<br>220 | 170<br>240 | mA | 1 |

**Note:**
1. IDD specifications are tested after the device is properly initialized. IDD parameters are specified with ODT disabled.
2. Input slew rate = 1 V/ns.

## IDD Measurement Conditions

( VDDQ = 1.8V ± 0.1V; VDD = 1.8V ± 0.1V)

| Symbol | Parameter/Condition |
|---|---|
| $I_{DD0}$ | **Operating Current** - **One bank Active - Precharge**<br>tCK =tCKmin.; tRC = tRCmin; tRAS = tRASmin; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands.<br>Address and control inputs are SWITCHING; Data bus inputs are SWITCHING; |
| $I_{DD1}$ | **Operating Current** - **One bank Active - Read - Precharge**<br>IOUT = 0 mA; BL = 4, tCK = tCKmin, tRC = tRCmin; tRAS = tRASmin; tRCD = tRCDmin, CL = CLmin.;AL = 0;<br>CKE is HIGH, $\overline{CS}$ is HIGH between valid commands;Address bus inputs are SWITCHING,Data bus inputs are SWITCHING; |
| $I_{DD2P}$ | **Precharge Power-Down Current:** All banks idle; CKE is LOW; tCK = tCKmin.; Other control and address inputs are STABLE, Data Bus inputs are FLOATING. |
| $I_{DD2N}$ | **Precharge Standby Current**: All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; tCK = tCKmin.; Other control and address bus inputs are SWICHTING; Data bus inputs are SWITCHING. |
| $I_{DD2Q}$ | **Precharge Quiet Standby Current**:All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; tCK = tCKmin.; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING. |
| $I_{DD3P(0)}$ | **Active Power-Down Current**: All banks open; tCK = tCKmin.;CKE is LOW; Other control and address inputs are STABLE; Data Bus inputs are FLOATING. MRS A12 bit is set to "0"( Fast Power-down Exit); |
| $I_{DD3P(1)}$ | **Active Power-Down Current**: All banks open; tCK = tCKmin.;CKE is LOW; Other control and address inputs are STABLE; Data Bus inputs are FLOATING. MRS A12 bit is set to "1"( Slow Power-down Exit); |
| $I_{DD3N}$ | **Active Standby Current**: All banks open; tCK = tCKmin.; tRAS = tRASmax.; tRP = tRPmin., CKE is HIGH; $\overline{CS}$ is HIGH between valid commands; Other control and address inputs are SWITCHING; Data Bus inputs are SWITCHING. |
| $I_{DD4R}$ | **Operating Current - Burst Read:** All banks open; Continuous burst reads; BL = 4; AL = 0, CL = CLmin.; tCK = tCKmin.; tRAS = tRASmax., tRP = tRPmin., CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address inputs are SWITCHING; Data bus inputs are SWITCHING; IOUT = 0mA. |
| $I_{DD4W}$ | **Operating Current - Burst Write:** All banks open; Continuous burst writes; BL = 4; AL = 0, CL = CLmin.; tCK = tCKmin.; tRAS = tRASmax., tRP = tRPmin.;CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address inputs are SWITCHING; Data Bus inputs are SWITCHING. |
| $I_{DD5B}$ | **Burst Auto-Refresh Current**: tCK = tCKmin.; Refresh command every tRFC = tRFCmin interval; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and adress inputs are SWITCHING; Data bus inputs are SWITCHING. |
| $I_{DD5D}$ | **Distributed Auto-Refresh Current**: tCK = tCKmin.; Refresh command every tREFI interval; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and adress inputs are SWITCHING; Data bus inputs are SWITCHING |
| $I_{DD6}$ | **Self-Refresh Current**: CKE <= 0.2V; external clock off, CK and $\overline{CK}$ at 0V; Other control and address inputs are FLOATING; Data Bus inputs are FLOATING. |
| $I_{DD7}$ | **Operating Bank Interleave Read Current:**<br>1. All bank interleaving reads; IOUT = 0 mA, BL =4, CL = CLmin., AL = tRCDmin. - 1*tCK; tCK = tCKmin., tRC = TRCmin.; tRRD = tRRDmin; tRCD = 1*tCK, CKE = HIGH, CS is HIGH between valid commands; Address bus inputs are STABLE during DESELECTS.<br>2. Timing pattern:<br>- ***DDR2 -400*** : A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D D D<br>- ***DDR2 -533*** : A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D D D<br>- ***DDR2 -667*** : A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D<br>3. Legend : A=Activate, RA=Read with Auto-Precharge, D=DESELECT |

1. IDD specifications are tested after the device is properly initialized.
2. IDD parameter are specified with ODT disabled.
3. Data Bus consists of DQ, DM, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$, LDQS, $\overline{LDQS}$, UDQS and $\overline{UDQS}$.
4. Definitions for IDD :
   LOW is defined as VIN <= VILAC(max.); HIGH is defined as VIN >= VIHAC(min.);
   STABLE is defined as inputs are stable at a HIGH or LOW level
   FLOATING is defined as inputs are VREF = VDDQ / 2
   SWITCHING is defined as:
   Inputs are changing between HIGH and LOW every other clock (once per two clocks) for adress and control signals, and
   inputs changing between HIGH and LOW every other clock (once per two clocks) for DQ signals not including mask or strobes
5. Timing parameter minimum and maximum values for IDD current measurements are defined in the following table.

### IDD Measurement Conditions (cont'd)

For testing the IDD parameters, the following timing parameters are used:

| Parameter | | Symbol | -5A DDR2 -400 | -37B DDR2 -533 | -3C DDR2 -667 | Unit |
|---|---|---|---|---|---|---|
| | | | 3-3-3 | 4-4-4 | 5-5-5 | |
| CAS Latency | | CL(IDD) | 3 | 4 | 5 | $t_{CK}$ |
| Clock Cycle Time | | tCK(IDD) | 5 | 3.75 | 3 | ns |
| Active to Read or Write delay | | tRCD(IDD) | 15 | 15 | 15 | ns |
| Active to Active / Auto-Refresh command period | | tRC(IDD) | 55 | 60 | 60 | ns |
| Active bank A to Active bank B command delay | x4 & x8 | tRRD(IDD) | 7.5 | 7.5 | 7.5 | ns |
| | x16 | tRRD(IDD) | 10 | 10 | 10 | ns |
| Active to Precharge Command | | tRASmin(IDD) | 40 | 45 | 45 | ns |
| | | tRASmax(IDD) | 70000 | 70000 | 70000 | ns |
| Precharge Command Period | | tRP(IDD) | 15 | 15 | 15 | ns |
| Auto-Refresh to Active / Auto-Refresh command period | | tRFC(IDD) | 105 | 105 | 105 | ns |
| Average periodic Refresh interval | | tREFI | 7.8 | 7.8 | 7.8 | µs |

## ODT (On Die Termination) Current

The ODT function adds additional current consumption to the DDR2 SDRAM when enabled by the EMRS(1). Depending on address bits A6 & A2 in the EMRS(1) a "week" or "strong" termination can be selected. The current consumption for any terminated input pin, depends on the input pin is in tri-strate or driving "0" or "1", as long a ODT is enabled during a given period of time.

### ODT current per terminated input pin :

| | | EMRS(1) State | min. | typ. | max. | Unit |
|---|---|---|---|---|---|---|
| Enabled ODT current per DQ added IDDQ current for ODT enabled; ODT is HIGH; Data Bus inputs are FLOATING | IODTO | A6 = 0, A2 = 1 | 5 | 6 | 7.5 | mA/DQ |
| | | A6 = 1, A2 = 0 | 2.5 | 3 | 3.75 | mA/DQ |
| | | A6 = 1, A2 = 1 | 7.5 | 9 | 11.25 | mA/DQ |
| Active ODT current per DQ added IDDQ current for ODT enabled; ODT is HIGH; worst case of Data Bus inputs are STABLE or SWITCHING. | IODTT | A6 = 0, A2 = 1 | 10 | 12 | 15 | mA/DQ |
| | | A6 = 1, A2 = 0 | 5 | 6 | 7.5 | mA/DQ |
| | | A6 = 1, A2 = 1 | 15 | 18 | 22.5 | mA/DQ |
| note: For power consumption calculations the ODT duty cycle has to be taken into account | | | | | | |

## Electrical Characteristics & AC Timing - Absolute Specification

### Timing Parameter by Speed Grade

( $V_{DDQ}$ = 1.8V ± 0.1V; $V_{DD}$ = 1.8V ± 0.1V) (notes 1-4)

| Symbol | Parameter | | -5A DDR2 -400 | | -37B DDR2 -533 | | -3C DDR2 -667 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | min | max | min | max | min | max | | |
| $t_{AC}$ | DQ output access time from CK / $\overline{CK}$ | | - 600 | + 600 | -500 | +500 | -450 | +450 | ps | |
| $t_{DQSCK}$ | DQS output access time from CK / $\overline{CK}$ | | - 500 | + 500 | -450 | +450 | -400 | +400 | ps | |
| $t_{CH}$ | CK, $\overline{CK}$ high-level width | | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | $t_{CK}$ | |
| $t_{CL}$ | CK, $\overline{CK}$ low-level width | | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | $t_{CK}$ | |
| $t_{HP}$ | Clock half period | | min ($t_{CL}$, $t_{CH}$) | | min ($t_{CL}$, $t_{CH}$) | | min ($t_{CL}$, $t_{CH}$) | | | 5 |
| $t_{CK}$ | Clock cycle time | | 5000 | 8000 | 3750 | 8000 | 3000 | 8000 | ps | 6 |
| $t_{DS}$ | DQ and DM input setup time | | 150 | - | 100 | - | 100 | - | ps | 8 |
| $t_{DH}$ | DQ and DM input hold time | | 275 | - | 225 | - | 175 | - | ps | 8 |
| $t_{IPW}$ | Address and control input pulse width (each input) | | 0.6 | - | 0.6 | - | 0.6 | - | $t_{CK}$ | |
| $t_{DIPW}$ | DQ and DM input pulse width (each input) | | 0.35 | - | 0.35 | - | 0.35 | - | $t_{CK}$ | |
| $t_{HZ}$ | Data-out high-impedence time from CK / $\overline{CK}$ | | - | tACmax | - | tACmax | - | tACmax | ps | 9 |
| $t_{LZ(DQS)}$ | DQS low-impedence time from CK / $\overline{CK}$ | | tACmin | tACmax | tACmin | tACmax | tACmin | tACmax | ps | 9 |
| $t_{LZ(DQ)}$ | Data-out low-impedence time from CK / $\overline{CK}$ | | 2tACmin | tACmax | 2tACmin | tACmax | 2tACmin | tACmax | ps | 9 |
| $t_{DQSQ}$ | DQS-DQ skew (for DQS & associated DQ signals) | | - | 350 | - | 300 | - | 240 | ps | |
| $t_{QHS}$ | Data hold skew factor | | - | 450 | - | 400 | - | 340 | ps | |
| $t_{QH}$ | Data output hold time from DQS | | $t_{HP}$-$t_{QHS}$ | - | $t_{HP}$-$t_{QHS}$ | - | $t_{HP}$-$t_{QHS}$ | - | ps | |
| $t_{DQSS}$ | Write command to 1st DQS latching transition | | -0.25 | +0.25 | -0.25 | +0.25 | -0.25 | +0.25 | $t_{CK}$ | |
| $t_{DQSL,H}$ | DQS input low (high) pulse width (write cycle) | | 0.35 | - | 0.35 | - | 0.35 | - | $t_{CK}$ | |
| $t_{DSS}$ | DQS falling edge to CK setup time (write cycle) | | 0.2 | - | 0.2 | - | 0.2 | - | $t_{CK}$ | |
| $t_{DSH}$ | DQS falling edge hold time from CK (write cycle) | | 0.2 | - | 0.2 | - | 0.2 | - | $t_{CK}$ | |
| $t_{MRD}$ | Mode register set command cycle time | | 2 | - | 2 | - | 2 | - | $t_{CK}$ | |
| $t_{WPST}$ | Write postamble | | 0.40 | 0.60 | 0.40 | 0.60 | 0.40 | 0.60 | $t_{CK}$ | 10 |
| $t_{WPRE}$ | Write preamble | | 0.35 | - | 0.35 | - | 0.35 | - | $t_{CK}$ | |
| $t_{IS}$ | Address and control input setup time | | 350 | - | 250 | - | 200 | - | ps | 7 |
| $t_{IH}$ | Address and control input hold time | | 475 | - | 375 | - | 275 | - | ps | 7 |
| $t_{RPRE}$ | Read preamble | | 0.9 | 1.1 | 0.9 | 1.1 | 0.9 | 1.1 | $t_{CK}$ | 9 |
| $t_{RPST}$ | Read postamble | | 0.40 | 0.60 | 0.40 | 0.60 | 0.40 | 0.60 | $t_{CK}$ | 9 |
| $t_{RRD}$ | Active bank A to Active bank B command period | x4 & x8 (1k page size) | 7.5 | - | 7.5 | - | 7.5 | - | ns | |
| | | x16 (2k page size) | 10 | - | 10 | - | 10 | - | ns | |
| $t_{FAW}$ | Four Active window | x4 & x8 (1k page size) | 37.5 | - | 37.5 | - | 37.5 | - | ns | |
| | | x16 (2k page size) | 50 | - | 50 | - | 50 | - | ns | |

| Symbol | Parameter | -5A DDR2 -400 | | -37B DDR2 -533 | | -3C DDR2 -667 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | min | max | min | max | min | max | | |
| $t_{CCD}$ | $\overline{CAS}$ A to $\overline{CAS}$ B command period | 2 | - | 2 | - | 2 | - | $t_{CK}$ | |
| $t_{WR}$ | Write recovery time | 15 | - | 15 | - | 15 | - | ns | |
| $t_{DAL}$ | Auto-Precharge write recovery + precharge time | WR+$t_{RP}$ | - | WR+$t_{RP}$ | - | WR+$t_{RP}$ | - | $t_{CK}$ | 14 |
| $t_{WTR}$ | Internal Write to Read command delay | 10 | - | 7.5 | - | 7.5 | - | ns | 15 |
| $t_{RTP}$ | Internal Read to Precharge command delay | 7.5 | - | 7.5 | - | 7.5 | - | ns | |
| $t_{XSNR}$ | Exit Self-Refresh to non-Read command | $t_{RFC}$+10 | - | $t_{RFC}$+10 | - | $t_{RFC}$+10 | - | ns | |
| $t_{XSRD}$ | Exit Self-Refresh to Read command | 200 | - | 200 | - | 200 | - | $t_{CK}$ | |
| $t_{XP}$ | Exit precharge power-down to any valid command (other than NOP or Deselect) | 2 | - | 2 | - | 2 | - | $t_{CK}$ | |
| $t_{XARD}$ | Exit power down to any valid command (other than NOP or Deselect) | 2 | - | 2 | - | 2 | - | $t_{CK}$ | 16 |
| $t_{XARDS}$ | Exit active power-down mode to Read command (slow exit, lower power) | 6 - AL | - | 6 - AL | - | 7 - AL | - | $t_{CK}$ | 16 |
| $t_{CKE}$ | CKE minimum high and low pulse width | 3 | - | 3 | - | 3 | - | $t_{CK}$ | |
| WR | Wrtie recovery time with Auto-Precharge | $t_{WR}$/$t_{RP}$ | | $t_{WR}$/$t_{RP}$ | | $t_{WR}$/$t_{RP}$ | | | |
| $t_{RAS}$ | Active to Precharge command | 40 | 70000 | 45 | 70000 | 45 | 70000 | ns | 11 |
| $t_{RC}$ | Active to Active/Auto-Refresh command period | 55 | - | 60 | - | 60 | - | ns | |
| $t_{RFC}$ | Auto-Refresh to Active/Auto-Refresh command period | 105 | - | 105 | - | 105 | - | ns | 12 |
| $t_{RCD}$ | Active to Read or Write (with and without Auto-Precharge) delay | 15 | - | 15 | - | 15 | - | ns | 13 |
| $t_{RP}$ | Precharge command period | 15 | - | 15 | - | 15 | - | ns | |
| $t_{RC}$ | RAS cycle time | 55 | - | 60 | - | 60 | - | ns | |
| $t_{OIT}$ | OCD drive mode output delay | 0 | 12 | 0 | 12 | 0 | 12 | ns | |
| $t_{MOD}$ | MRS command to ODT update delay | 0 | 12 | 0 | 12 | 0 | 12 | ns | |
| $t_{DELAY}$ | Minimum time clocks remain ON after CKE asynchronously drops LOW | $t_{IS}$+$t_{CK}$ +$t_{IH}$ | - | $t_{IS}$+$t_{CK}$ +$t_{IH}$ | - | $t_{IS}$+$t_{CK}$ +$t_{IH}$ | - | ns | 17 |

Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restartet through the specified initialization sequence before normal operation can continue.

## ODT AC Electrical Characteristics and Operating Conditions (all speed bins)

| Symbol | Parameter / Condition | min. | max. | Units | Notes |
|---|---|---|---|---|---|
| $t_{AOND}$ | ODT turn-on delay | 2 | 2 | $t_{CK}$ | |
| $t_{AON}$ | ODT turn-on | tAC(min) | tAC(max) + 1* | ns | 18 |
| $t_{AONPD}$ | ODT turn-on (Power-Down Modes) | tAC(min) + 2 | 2 $t_{CK}$ + tAC(max) + 1 | ns | |
| $t_{AOFD}$ | ODT turn-off delay | 2.5 | 2.5 | $t_{CK}$ | |
| $t_{AOF}$ | ODT turn-off | tAC(min) | tAC(max) + 0.6 | ns | 19 |
| $t_{AOFPD}$ | ODT turn-off (Power-Down Modes) | tAC(min) + 2 | 2.5 $t_{CK}$ + tAC(max) + 1 | ns | |
| $t_{ANPD}$ | ODT to Power Down Mode Entry Latency | 3 | - | $t_{CK}$ | |
| $t_{AXPD}$ | ODT Power Down Exit Latency | 8 | - | $t_{CK}$ | |

* DDR2-667 $t_{AON}$ max = tAC(max) + 0.7

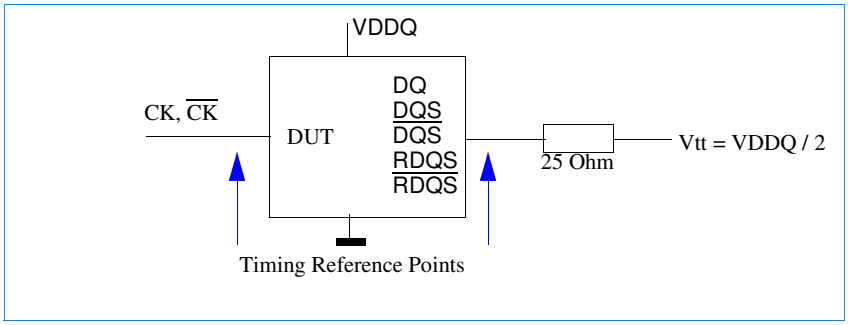
## Notes for Electrical Characteristics & AC Timing

1. Timings are guaranteed with CK/$\overline{CK}$ differential slew rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential slew rate of 2.0 V/ns in differential strobe mode and a slew rate of 1 V/ns in single ended mode. For other slew rates see Section 8 of this datasheet.
2. The CK / $\overline{CK}$ input reference level (for timing reference to CK / $\overline{CK}$) is the point at which CK and $\overline{CK}$ cross.
   The DQS / $\overline{DQS}$,RDQS/ $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode;
   The input reference level for signals other than CK/$\overline{CK}$, DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, tIS, tiH,tDS, tDH is VREF.
   For tIS, tiH, tDS, tDH input reference levels see section 8.3 of this datasheet
3. Inputs are not recognized as valid until VREF stabilizes. During the period before VREF stabilizes, CKE = 0.2 x VDDQ is recognized as LOW.
4. The output timing reference voltage level is VTT. See section 8 for the reference load for timing measurements.
5. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH.
6. For input frequency change during DRAM operation, see the 2.11 section of this datasheet.
7. For timing definition, slew rate and slew rate derating see Section 8.3
8. For timing definition, slew rate and slew rate derating see Section 8.3
9. The tHZ, tRPST and tLZ, tRPRE parameters are referenced to a specific voltage level, which specify when the device output is no longer driving (tHZ, tRPST), or begins driving (tLZ, tRPRE). tHZ and tLZ transitions occur in the same access time windows as valid data transitions.These parameters are guaranteed by design and characterisation, but are not tested on each device.
10. The maximum limit for this parameter is not a device limit. The device operate with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
11. tRAS(max) is calculated from the maximum amount of time a DDR2 device can operate without a Refresh command which is equal to 9 * tREFI
12. A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM device.
13. The tRCD timing parameter is valid for both activate command to read or write command with and without Auto-Precharge. Therefore a separate parameter tRAP for activate command to read or write command with Auto-Precharge is not necessary anymore.
14. For each of the terms, if not allready an integer, round to the next highest integer. tCK refers to the application clock period. WR refers to the WR parameter stored in the MRS.
15. tWTR is at least two clocks independent of operation frequency.
16. User can choose two different active power-down modes for additional power saving via MRS address bit A12.
    In “standard active power-down mode” (MRS, A12 = “0”) a fast power-down exit timing tXARD can be used. In “low active power-down mode” (MRS, A12 =”1”) a slow power-down exit timing tXARDS has to be satisfied.
17. The clock frequency is allowed to change during self-refresh mode or precharge power-down mode. In case of clock frequency change during power-down, a specific procedure is required as describes in section 2.12.
18. ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on.
    ODT turn on time max is when the ODT resistance is fully on. Both are measure from tAOND.
19. ODT turn off time min is when the device starts to turn off ODT resistance
    ODT turn off time max is when the bus is in high impedance. Both are measured from tAOFD.

# Reference Loads, Setup & Hold Timing Definition and Slew Rate Derating

## Reference Load for Timing Measurements

The figure represents the timing reference load used in defining the relevant timing parameters of the device. It is not intended to either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally a coaxial transmission line terminated at the tester electronics. This reference load is also used for output slew rate characterisation.




The output timing reference voltage level for single ended signals is the crosspoint with VTT.
The output timing reference voltage level for differential signals is the crosspoint of the true ( e.g. DQS) and the complement (e.g. DQS) signal.

## Slewrate Measurements

### Output Slewrate

With the reference load for timing measurements output slew rate for falling and rising edges is measured between VTT - 250 mV and VTT + 250 mV for single ended signals.For differential signals (e.g. DQS / DQS) output slew rate is measured between DQS - DQS = - 500 mV and DQS - DQS = + 500 mV. Output slew rate is guaranteed by design, but is not necessarily tested on each device.

### Input Slewrate - Differential signals

Input slewrate for differential signals ( CK / CK, DQS / DQS, RDQS / RDQS) for rising edges are measured from f.e. CK - CK = -250 mV to CK - CK = + 500 mV and from CK - CK = +250 mV to CK - CK = - 500mV for falling edges.

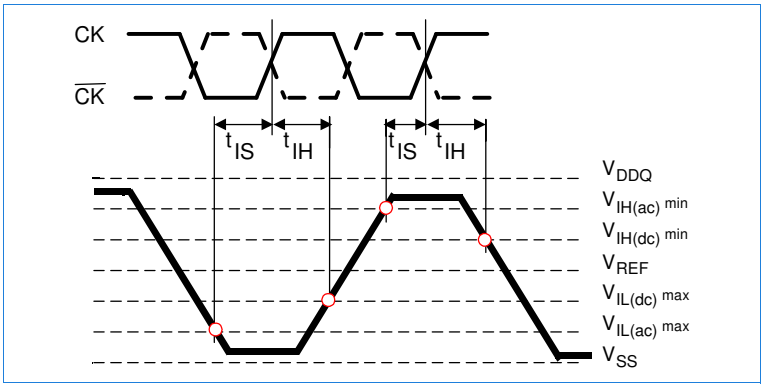
### Input Slewrate - Single ended signals

Input slew rate for single ended signals (other than tis, tih, tds and tdh) are measured from dc-level to ac-level: VREF -125 mV to VREF + 250 mV for rising edges and from VREF + 125 mV to VREF - 250 mV for falling edges. For slew rate definition of the input and data setup and hold parameters see section 8.3 of this datasheet.

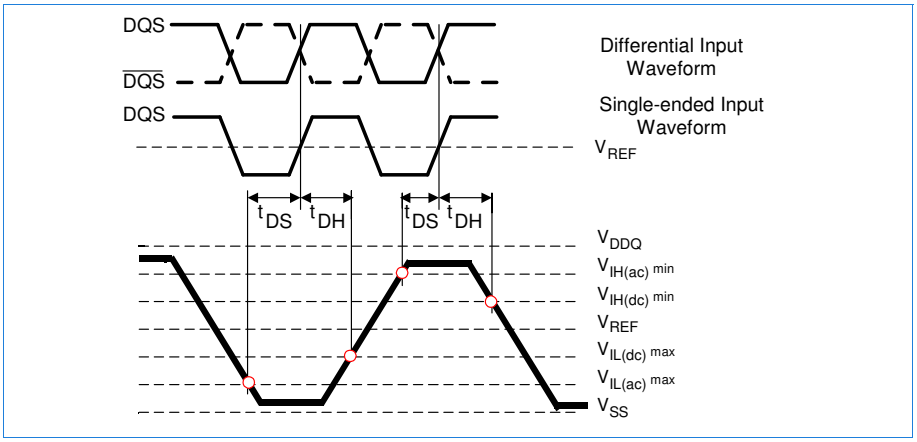
## Input and Data Setup and Hold Time

### Timing Definition for Input Setup (tIS) and Hold Time (tIH)

Address and control input setup time (tIS) is referenced from the input signal crossing at the VIH(ac) level for a rising signal and VIL(ac) for a falling signal applied to the device under test. Address and control input hold time (tIH) is referenced from the input signal crossing at the VIL(dc) level for a rising signal and VIH(dc) for a falling signal applied to the device under test




### Timing Definition for Data Setup (tDS) and Hold Time (tDH)



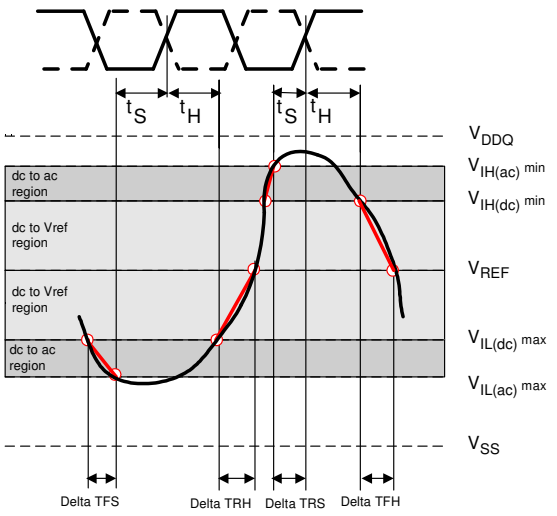

1. Data input setup time with differential data strobe enabled MR[bit10]=0, is referenced from the input signal crossing at the VIH(ac) level to the differential data strobe crosspoint for a rising signal, and from the input signal crossing at the VIL(ac) level tothe differential data strobe crosspoint for a falling signal applied to the device under test. Input waveform timing with single-endeddata strobe enabled MR[bit10]=1, is referenced from the input signal crossing at the VIH(ac) level to the data strobe crossing Vref for a rising signal, and from the input signal crossing at the VIL(ac) level to the single-ended data strobe crossing Vref for a falling signal applied to the device under test.

2. Data input hold time with differential data strobe enabled MR[bit10]=0, is referenced from the input signal crossing at the VIL(dc) level to the differential data strobe crosspoint for a rising signal and VIH(dc) to the differential data strobe crosspoint for a falling signal applied to the device under test. Input waveform timing with single-ended data strobe enabled MR[bit10]=1, is referenced from the input signal crossing at the VIL(dc) level to the single-ended data strobe crossing Vref for a rising signal and VIH(dc) to the single-ended data strobe crossing Vref for a falling signal applied to the device under test

### Slew Rate Definition for Input and Data Setup and Hold Times

Setup (tIS & tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIH(dc)min and the first crossing of VIH(ac)min. Setup (tIS & tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIL(dc)max and the first crossing of VIL(ac)max, (fig. A) If the actual signal is always earlier than the nominal slew rate line between shaded 'dc to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded 'dc to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value.(fig.B)

Hold (tIH & tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(dc)max and the first crossing of Vref. Hold (tIH & tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(dc)min and the first crossing of Vref.(fig. A). If the actual signal is always later than the nominal slew rate line between shaded 'dc to Vref region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to Vref region', the slew rate of a tangent line to the actual signal from the dc level to Vref level is used for derating value.(fig.B)



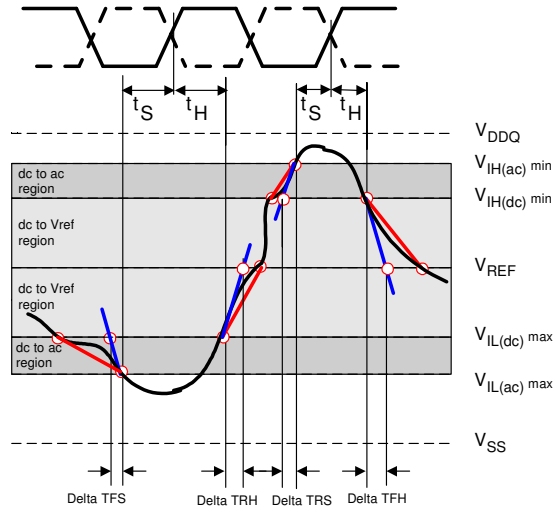

$$\text{Setup Slew Rate} = \frac{\text{VIL(dc)max - VIL(ac)max}}{\text{Delta TFS}} \quad \text{falling signal}$$

$$\text{Setup Slew Rate} = \frac{\text{VIH(dc)min - VIL(ac)min}}{\text{Delta TRS}} \quad \text{rising signal}$$

$$\text{Hold Slew Rate} = \frac{\text{VREF - VIL(dc)max}}{\text{Delta TRH}} \quad \text{rising signal}$$

$$\text{Hold Slew Rate} = \frac{\text{VIH(dc)min - VREF}}{\text{Delta TFH}} \quad \text{falling signal}$$

fig. A




$$\text{Setup Slew Rate} = \frac{\text{tangent line [VIL(dc)max - VIL(ac)max]}}{\text{Delta TFS}} \quad \text{falling signal}$$

$$\text{Setup Slew Rate} = \frac{\text{tangent line [VIH(dc)min - VIL(ac)min]}}{\text{Delta TRS}} \quad \text{rising signal}$$

$$\text{Hold Slew Rate} = \frac{\text{tangent line [REF - VIL(dc)max]}}{\text{Delta TRH}} \quad \text{rising signal}$$

$$\text{Hold Slew Rate} = \frac{\text{tangent line [VIH(dc)min - VREF]}}{\text{Delta TFH}} \quad \text{falling signal}$$

fig. B

## Input Setup (tIS) and Hold (tIH) Time DeratingTable

| | | CK, $\overline{CK}$ Differential Slew Rate | | | | | |
|---|---|---|---|---|---|---|---|
| | | 2.0 V/ns | | 1.5 V/ns | | 1.0 V/ns | |
| | | D tIS | D tIH | D tIS | D tIH | D tIS | D tIH |
| Command / Address Slew rate | 4.0 | 187 | 94 | 217 | 124 | 247 | 154 |
| | 3.5 | 179 | 89 | 209 | 119 | 239 | 149 |
| | 3.0 | 167 | 83 | 197 | 113 | 227 | 143 |
| | 2.5 | 150 | 75 | 180 | 105 | 210 | 135 |
| | 2.0 | 125 | 45 | 155 | 75 | 185 | 105 |
| | 1.5 | 83 | 21 | 113 | 51 | 143 | 81 |
| | 1.0 | 0 | 0 | 30 | 30 | 60 | 60 |
| | 0.9 | -11 | -14 | 19 | 16 | 49 | 46 |
| | 0.8 | -25 | -31 | 5 | -1 | 35 | 29 |
| | 0.7 | -43 | -54 | -13 | -24 | 17 | 6 |
| | 0.6 | -67 | -83 | -37 | -53 | -7 | -23 |
| | 0.5 | -110 | -125 | -80 | -95 | -50 | -65 |
| | 0.4 | -175 | -188 | -145 | -158 | -115 | -128 |
| | 0.3 | -285 | -292 | -255 | -262 | -225 | -232 |
| | 0.25 | -350 | -375 | -320 | -345 | -290 | -315 |
| | 0.2 | -525 | -500 | -495 | -470 | -465 | -440 |
| | 0.15 | -800 | -708 | -770 | -678 | -740 | -648 |
| | 0.1 | -1450 | -1125 | -1420 | -1095 | -1390 | -1065 |

1. All units in ps.
2. For all input signals the total tIS (input setup time) and tIH (input hold time) required is calculated by adding the individual datasheet value to the derating value listed in the previous table.

## DDR2-667 Data Setup (tDS) and Hold Time (tDH) Derating Table

| | | DQS, $\overline{DQS}$ Differential Slew Rate | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 4.0 V/ns | | 3.0 V/ns | | 2.0 V/ns | | 1.8 V/ns | | 1.6 V/ns | | 1.4 V/ns | | 1.2 V/ns | | 1.0 V/ns | | 0.8 V/ns | |
| | | D tDS | D tDH | D tDS | D tDH | D tDS | D tDH | D tDS | D tDH | D tDS | D tDH | D tDS | D tDH | D tDS | D tDH | D tDS | D tDH | D tDS | D tDH |
| DQ Slewrate (V/ns) | **2.0** | 100 | 45 | 100 | 45 | 100 | 45 | - | - | - | - | - | - | - | - | - | - | - | - |
| | **1.5** | 67 | 21 | 67 | 21 | 67 | 21 | 79 | 33 | - | - | - | - | - | - | - | - | - | - |
| | **1.0** | 0 | 0 | 0 | 0 | 0 | 0 | 12 | 12 | 24 | 24 | - | - | - | - | - | - | - | - |
| | **0.9** | - | - | -5 | -14 | -5 | -14 | 7 | -2 | 19 | 10 | 31 | 22 | - | - | - | - | - | - |
| | **0.8** | - | - | - | - | -13 | -31 | -1 | -19 | 11 | -7 | 23 | 5 | 35 | 17 | - | - | - | - |
| | **0.7** | - | - | - | - | - | - | -10 | -42 | 2 | -30 | 14 | -18 | 26 | -6 | 38 | 6 | - | - |
| | **0.6** | - | - | - | - | - | - | - | - | -10 | -59 | 2 | -47 | 14 | -35 | 26 | -23 | 38 | -11 |
| | **0.5** | - | - | - | - | - | - | - | - | - | - | -24 | -89 | -12 | -77 | 0 | -65 | 12 | -53 |
| | **0.4** | - | - | - | - | - | - | - | - | - | - | - | - | -52 | -140 | -40 | -128 | -28 | -116 |

1. All units in ps.
2. For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the individual datasheet value to the derating value listed in the previous table.

## DDR2-400/533 Data Setup (tDS1) and Hold Time (tDH1) Derating Table

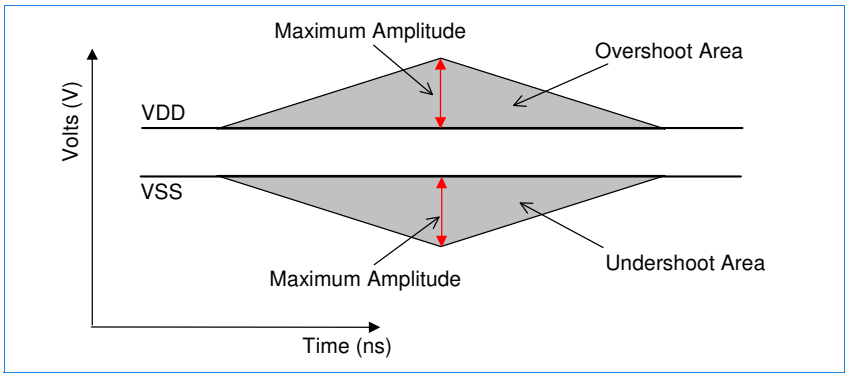
| | | DQS Single-ended Slew Rate | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 2.0 V/ns | | 1.5 V/ns | | 1.0 V/ns | | 0.9 V/ns | | 0.8 V/ns | | 0.7 V/ns | | 0.6 V/ns | | 0.5 V/ns | | 0.4 V/ns | |
| | | D tDS1 | D tDH1 | D tDS1 | D tDH1 | D tDS1 | D tDH1 | D tDS1 | D tDH1 | D tDS1 | D tDH1 | D tDS1 | D tDH1 | D tDS1 | D tDH1 | D tDS1 | D tDH1 | D tDS1 | D tDH1 |
| DQ Slewrate (V/ns) | **2.0** | 188 | 188 | 167 | 146 | 125 | 63 | - | - | - | - | - | - | - | - | - | - | - | - |
| | **1.5** | 146 | 167 | 125 | 125 | 83 | 42 | 81 | 43 | - | - | - | - | - | - | - | - | - | - |
| | **1.0** | 63 | 125 | 42 | 83 | 0 | 0 | -2 | 1 | -7 | -13 | - | - | - | - | - | - | - | - |
| | **0.9** | - | - | 31 | 69 | -11 | -14 | -13 | -13 | -18 | -27 | -29 | -45 | - | - | - | - | - | - |
| | **0.8** | - | - | - | - | -25 | -31 | -27 | -30 | -32 | -44 | -43 | -62 | -60 | -86 | - | - | - | - |
| | **0.7** | - | - | - | - | - | - | -45 | -53 | -50 | -67 | -61 | -85 | -78 | -109 | -108 | -152 | - | - |
| | **0.6** | - | - | - | - | - | - | - | - | -74 | -96 | -85 | -114 | -102 | -138 | -132 | -181 | -183 | -246 |
| | **0.5** | - | - | - | - | - | - | - | - | - | - | -128 | -156 | -145 | -180 | -175 | -223 | -226 | -288 |
| | **0.4** | - | - | - | - | - | - | - | - | - | - | - | - | -210 | -243 | -240 | -286 | -291 | -351 |

1. All units in ps.
2. For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the individual datasheet value to the derating value listed in the previous table.

# Overshoot and Undershoot Specification

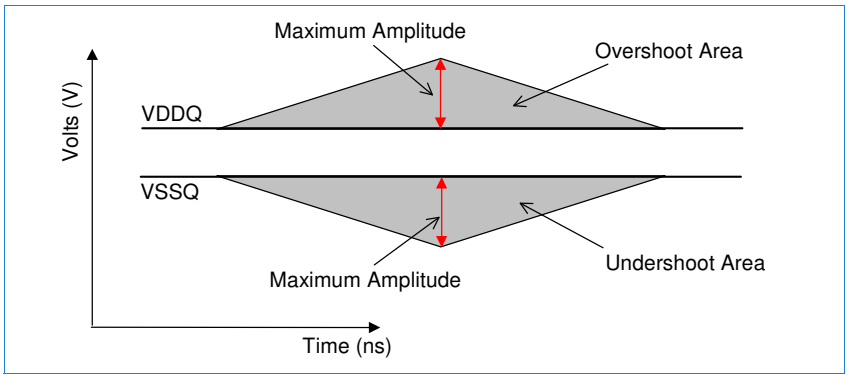
## AC Overshoot / Undershoot Specification for Address and Control Pins

| Parameter | DDR2 -400 | DDR2 -533 | DDR2 -667 | Units |
|---|---|---|---|---|
| Maximum peak amplitude allowed for overshoot area | (0.5)0.9 | (0.5)0.9 | (0.5)0.9 | V |
| Maximum peak amplitude allowed for undershoot area | (0.5)0.9 | (0.5)0.9 | (0.5)0.9 | V |
| Maximum overshoot area above VDD | 1.33 | 1.0 | 0.8 | V.ns |
| Maximum undershoot area below VSS | 1.33 | 1.0 | 0.8 | V.ns |
| Note: The maximum requirements of peak amplitude were reduced from 0.9V to 0.5V. | | | | |

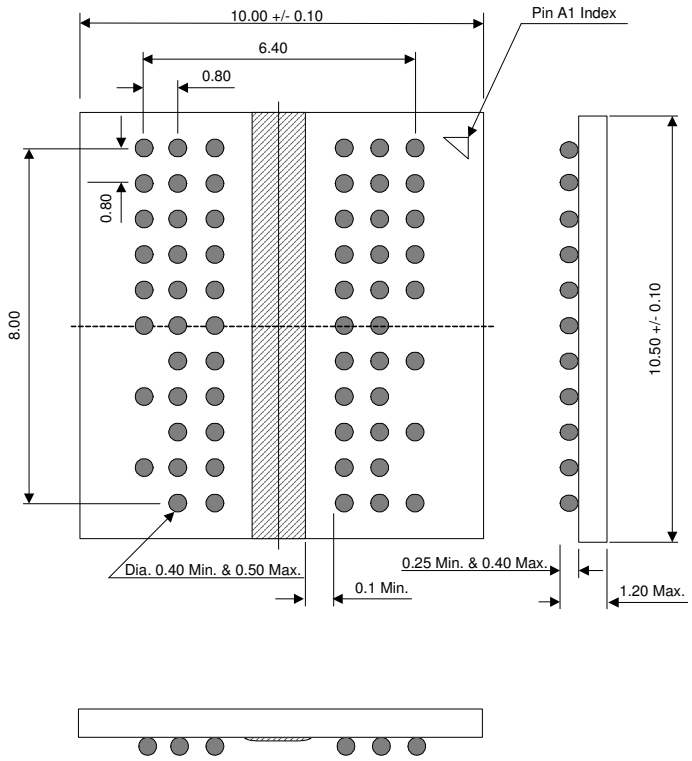



## AC Overshoot / Undershoot Specification for Clock, Data, Strobe and Mask Pins

| Parameter | DDR2 -400 | DDR2 -533 | DDR2 -667 | Units |
|---|---|---|---|---|
| Maximum peak amplitude allowed for overshoot area | 0.5 | 0.5 | 0.5 | V |
| Maximum peak amplitude allowed for undershoot area | 0.5 | 0.5 | 0.5 | V |
| Maximum overshoot area above VDDQ | 0.38 | 0.28 | 0.23 | V.ns |
| Maximum undershoot area below VSSQ | 0.38 | 0.28 | 0.23 | V.ns |

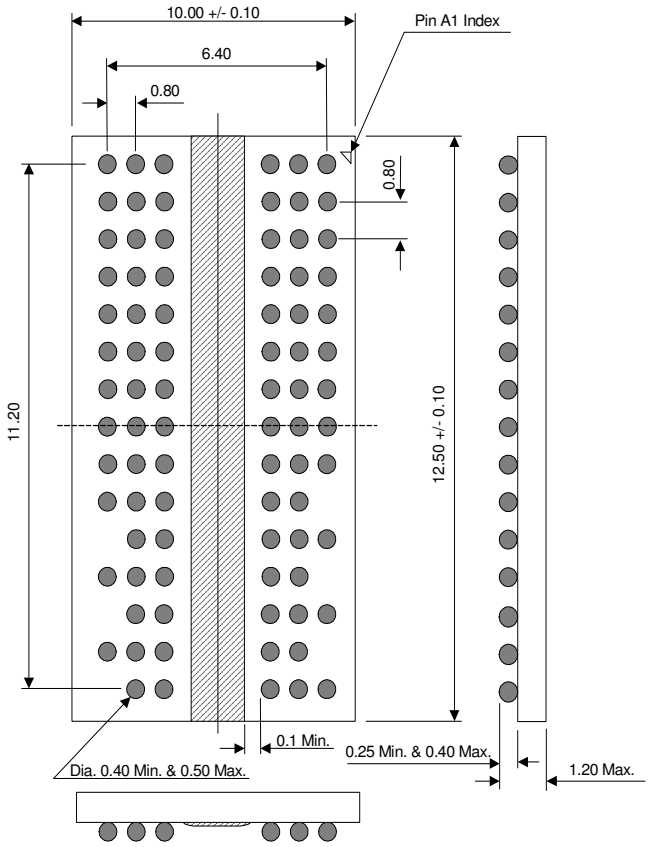


## Package Dimensions (60 balls; 0.8mmx0.8mm Pitch; BGA Package)




Note : All dimensions are typical unless otherwise stated.
Unit : Millimeters

## Package Dimensions (84 balls; 0.8mmx0.8mm Pitch; BGA Package)




Note : All dimensions are typical unless otherwise stated.
Unit : Millimeters

## Revision Log

| Rev | Date | Modification |
|---|---|---|
| 0.1 | 08/2003 | Preliminary Release |
| 1.0 | 09/2004 | Added Idd to specification |
| 1.1 | 11/2004 | Added derating values and x4/x8 60 balls and 84 balls pin configuration |
| 1.2 | 03/2005 | Added green product part number |
| 1.3 | 06/2005 | Remove 84Ball x8 ball assignment |
| 1.4 | 07/2005 | Update IDD measurement & Timing Parameters |
| 1.5 | 09/2005 | Update EMR(2) |
| 1.6 | 03/2006 | Update Overshoot/undershoot spec |
| 1.7 | 03/2006 | All products are BGA package; Update ODT current. |
| 1.8 | 04/2006 | Update Functional Presentation of ODT |
| 1.9 | 06/2006 | Add TSOP spec.<br>Update ODT DC Electrical Characteristrics, DC & AC Logic Input Levels, and Input / Output Capacitance. |
| 2.0 | 07/2006 | update EMR(2). This device does not support high temp self refresh. |
| 2.1 | 03/2007 | Modified x16 84 balls pin configuration |
| 2.2 | 10/2007 | Remove NT5TU32M16AS-5A/37B/3C with TSOP support |
| 2.3 | 06/2008 | Modified Block Diagram |



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