± 2g Tri-Axis Digital Accelerometer Specifications

PART NUMBER:

KXP74-1050

36 Thornwood Drive
Ithaca, New York 14850
Tel: 607-257-1080
Fax: 607-257-1146
www.kionix.com

	APPROVED BY	DATE
PROD. MGR.	S. Miller	12/01/06
TECH. MGR.	K. Foust	12/01/06
TEST MGR.	J. Chong	12/01/06
VP ENG.	T. Davis	12/01/06

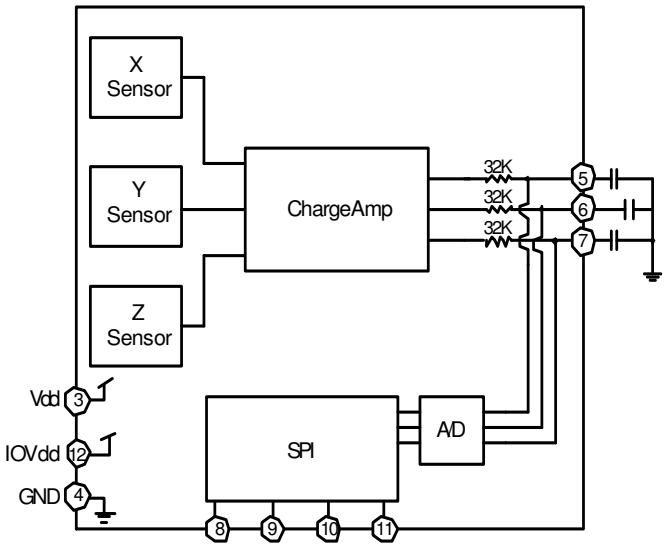
ECN #	PCN #	REV	PG #	REVISION DESCRIPTION	DATE	REV'D BY
		1	3,6	12-bit operation	7/7/05	S. Miller
06-004		2		Updated specification to new format	3/23/06	A. Bergstrom, S. Miller
		3	2,3,5	Functional Diagram, 0g Offset (RT), App Schem	5/25/06	K. Foust
	06-005	4	3-6,8	Improved performance	12/01/06	S. Miller

Kionix®	**± 2g Tri-Axis Digital Accelerometer Specifications**	**PART NUMBER:** **KXP74-1050**

Product Description

The KXP74-1050 is a tri-axis, serial-output (SPI), silicon micromachined accelerometer with a full-scale output range of ±2g (19.6m/s^2). The sense element is fabricated using Kionix's proprietary plasma micromachining process technology. Acceleration sensing is based on the principle of a differential capacitance arising from acceleration-induced motion of the sense element, which further utilizes common mode cancellation to decrease errors from process variation, temperature, and environmental stress. The sense element is hermetically sealed at the wafer level by bonding a second silicon lid wafer to the device using a glass frit. A separate ASIC device packaged with the sense element provides signal conditioning and self-test. The accelerometer is delivered in an 5 x 5 x 1.2mm Dual Flat No-lead (DFN) plastic package operating from a 2.7 - 5V DC supply. The digital I/O pads are powered from a separate power pin, and will interface to 1.8V logic. The three outputs are read through the digital SPI interface, which is also used to command Selftest and Standby Mode.

Functional Diagram



Kionix®	± 2g Tri-Axis Digital Accelerometer Specifications	PART NUMBER: KXP74-1050

Product Specifications

Table 1. Mechanical

(specifications are for 12-bit operation at V_{dd} = 2.8V and T = 25ºC unless stated otherwise)

Parameters	Units	Min	Typical	Max
Operating Temperature Range	ºC	-40	-	85
Zero-g Offset	counts	1925	2048	2171
Zero-g Offset Variation from RT over Temp.	mg/ºC		±1.0	
Sensitivity	counts/g	794	819	844
Sensitivity Variation from RT over Temp.	%/ºC		±0.015	
Offset Ratiometric Error (V_{dd} = 2.8V ± 5%)	%		0.3	1.5
Sensitivity Ratiometric Error (V_{dd} = 2.8V ± 5%)	%		0.5	1.5
Resolution	mg		1.22	
Non-Linearity	% of FS		0.1	
Cross Axis Sensitivity	%		2.0	
Self Test Output change on Activation	g	1.6 (xy) 0.4 (z)	2.0 (xy) 0.7 (z)	2.4 (xy) 1.0 (z)
Bandwidth (-3dB)[1]	Hz		3300 (xy) 1700 (z)	
Noise Density (on filter pins)	µg / √Hz		175	

Notes:

1. User definable with external capacitors. Maximum defined by the frequency response of the sensors.

Table 2. Electrical

(specifications are for 12-bit operation at V_{dd} = 2.8V and T = 25ºC unless stated otherwise)

Parameters		Units	Min	Typical	Max
Supply Voltage (V_{dd})	Operating	V	2.7	2.8	5.25
I/O Pads Supply Voltage (V_{IO})		V	1.7		V_{dd}
Current Consumption	Operating[1]	mA	0.6	0.8	1
	Standby	µA			10
Input Low Voltage		V			0.2 * V_{IO}
Input High Voltage		V	0.8 * V_{IO}		
Input Pull-down Current		µA		60	
A/D Conversion time		µs		40	
SPI Communication Rate		MHz		5	
Analog Output Resistance(R_{out})		kΩ	24	32	40
Power Up Time[2]		ms		5*R_{out}*C	

Notes:

1. Actual current consumption during operation depends on user selected sampling speed.
2. Power up time is determined by 5 times the RC time constant of the user defined low pass filter.

Table 4. Environmental

Parameters		Units	Min	Typical	Max
Supply Voltage (V_{dd})	Absolute Limits	V	-0.3		7.0
Operating Temperature Range		ºC	-40		85
Storage Temperature Range		ºC	-55		150
Mech. Shock (powered and unpowered)		g			5000 for 0.5ms
ESD	HBM	V			3000

Caution: ESD Sensitive and Mechanical Shock Sensitive Component, improper handling can cause permanent damage to the device.

The 14-pin DFN package conforms to European Union Directive 2002/95/EC on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS).

Soldering

Soldering recommendations available upon request or from www.kionix.com.

Application Schematic

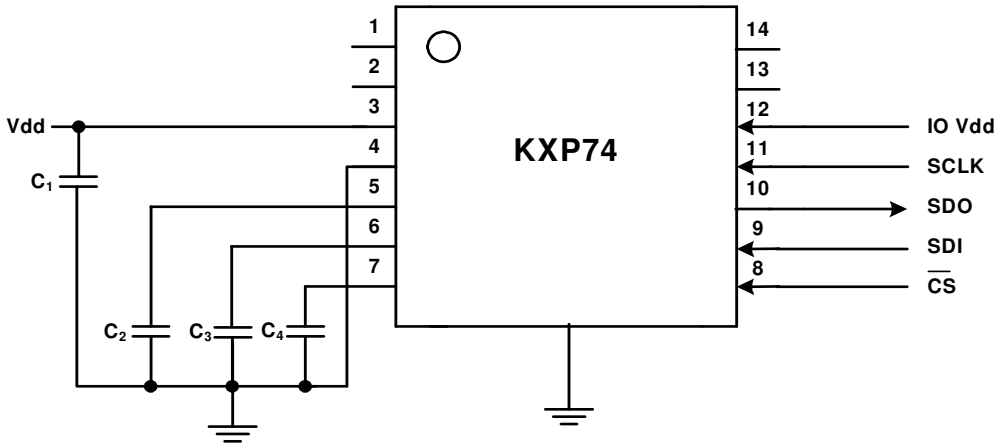


Table 4. KXP74 Pin Descriptions

Pin	Name	Description
1	NC	Not Connected Internally
2	NC	Not Connected Internally
3	Vdd	The power supply input. Decouple this pin to ground with a 0.1uF ceramic capacitor (C_1).
4	GND	Ground
5	X Output	Analog output of the x-channel. Optionally, a capacitor (C_2) placed between this pin and ground will form a low pass filter.
6	Y Output	Analog output of y-channel. Optionally, a capacitor (C_3) placed between this pin and ground will form a low pass filter.
7	Z Output	Analog output of z-channel. Optionally, a capacitor (C_4)placed between this pin and ground will form a low pass filter.
8	nCS	SPI Chip Select
9	SDI	SPI Serial Data Input
10	SDO	SPI Serial Data Output
11	SCLK	SPI Communication Clock
12	IO Vdd	Power Supply for I/O pads
13	NC	Not Connected Internally
14	NC	Not Connected Internally
	Center pad	Not Connected Internally – recommend grounding

Application Design Equations:

The bandwidth is determined by the filter capacitors connected from pins 5, 6 and 7 to ground. The response is single pole.
Given a desired bandwidth, f_{BW}, the filter capacitors are determined by:

$$C_2 = C_3 = C_4 = \frac{4.97x10^{-6}}{f_{BW}}$$

Notes:

1. Self test and standby modes are enabled through the SPI interface.
2. X, Y and Z analog outputs are active when the KXP74 is enabled through SPI.

Test Specifications

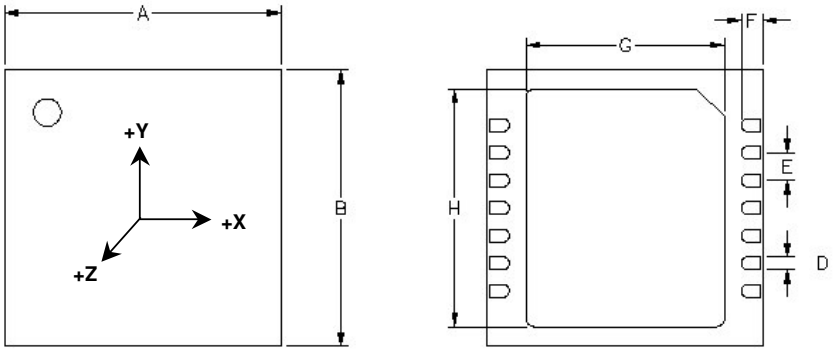
Special Characteristics:

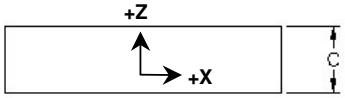
These characteristics have been identified as being critical to the customer. Every part is tested to verify its conformance to specification prior to shipment.

Parameter		Specification	Test Conditions
Zero-g Offset @ RT		2048 ± 123	25ºC, V_{dd} = 2.8V
Sensitivity @ RT		819 ± 25	25ºC, V_{dd} = 2.8V
Current Consumption	Operating	0.65 <= I_{dd} <= 1mA	25ºC, V_{dd} = 2.8V

Package Dimensions and Orientation

5 x 5 x 1.2 mm DFN



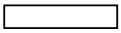
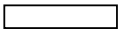


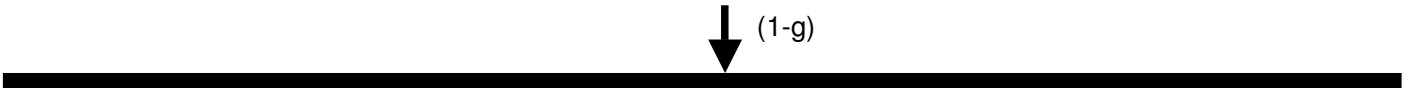
Dimension	mm			inch		
	Min	Nom	Max	Min	Nom	Max
A		5.00			0.197	
B		5.00			0.197	
C	1.10	1.20	1.30	0.043	0.047	0.051
D	0.18	0.23	0.28	0.007	0.009	0.011
E		0.50			0.020	
F	0.35	0.40	0.45	0.014	0.016	0.018
G	3.50	3.60	3.70	0.138	0.142	0.146
H	4.20	4.30	4.40	0.165	0.169	0.173

All dimensions and tolerances conform to ASME Y14.5M-1994

When device is accelerated in +X, +Y or +Z direction, the corresponding output will increase.

Static X/Y/Z Output Response versus Orientation to Earth's surface (1-g):

Position	1	2	3	4	5	6
Diagram					Top  Bottom	Bottom  Top
X	2048	2867	2048	1229	2048	2048
Y	2867	2048	1229	2048	2048	2048
Z	2048	2048	2048	2048	2867	1229
X-Polarity	**0**	**+**	**0**	**-**	**0**	**0**
Y-Polarity	**+**	**0**	**-**	**0**	**0**	**0**
Z-Polarity	**0**	**0**	**0**	**0**	**+**	**-**



Earth's Surface

KXP74 Digital Interface

The Kionix KXP74 digital accelerometer has the ability to communicate on a SPI digital serial interface bus. This flexibility allows for easy system integration by eliminating analog-to-digital converter requirements and by providing direct communication with system micro-controllers.

The serial interface terms and descriptions as indicated in Table 6 below will be observed throughout this document.

Term	Description
Transmitter	The device that transmits data to the bus.
Receiver	The device that receives data from the bus.
Master	The device that initiates a transfer, generates clock signals and terminates a transfer.
Slave	The device addressed by the Master.

Table 6. Serial Interface Terminologies

SPI Interface

The KXP74 utilizes an integrated Serial Peripheral Interface (SPI) for digital communication. The SPI interface is primarily used for synchronous serial communication between one Master device and one or more Slave devices. The Master, typically a micro controller, provides the SPI clock signal (SCLK) and determines the state of Chip Select (nCS). The KXP74 always operates as a Slave device during standard Master-Slave SPI operation.

SPI is a 4-wire synchronous serial interface that uses two control and two data lines. With respect to the Master, the Serial Clock output (SCLK), the Data Output (MOSI) and the Data Input (MISO) are shared among the Slave devices. The Master generates an independent Chip Select (nCS) for each Slave device that goes low at the start of transmission and goes back high at the end. The Slave Data Output (SDO) line, remains in a high-impedance (hi-z) state when the device is not selected, so it does not interfere with any active devices. This allows multiple Slave devices to share a master SPI port as shown in Figure 2 below.

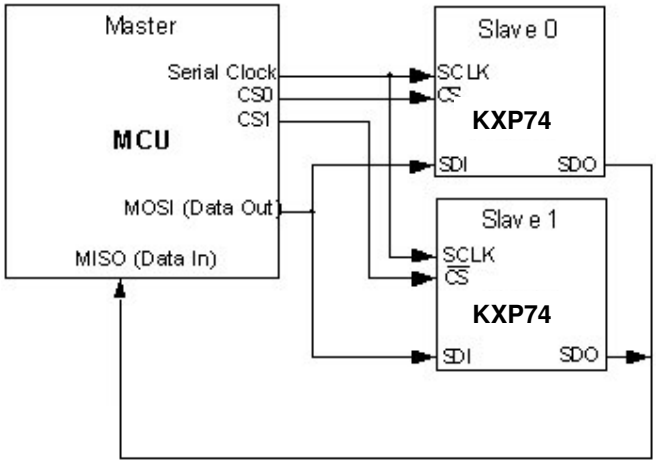


Figure 2 KXP74 SPI Connections

Control Register Write and Read

The control register embedded in the KXP74 has an 8-bit address. Upon power up, the Master must write to the accelerometer's control register to set its operational mode. On the falling edge of nCS, a 2-byte command is written to the control register. The first byte, 0x04, initiates the write to the appropriate register, and is followed by the user-defined, operational-mode byte. All commands are sent MSB (most significant bit) first, and the host must return nCS high for at least 200nS before the next data request. Figure 3 below shows the timing diagram for carrying out the 8-bit control register write operation.

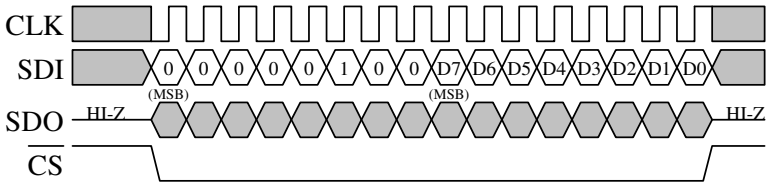


Figure 3 Timing Diagram for 8-Bit Control Register Write Operation

In order to read the 8-bit control register, an 8-bit read command, 0x03, must be written to the accelerometer to initiate the read. Upon receiving the command, the accelerometer returns the 8-bit operational-mode data stored in the control register. This operation also occurs over 16 clock cycles. All

returned data is sent MSB first, and the host must return nCS high for at least 200nS before the next data request. Figure 4 shows the timing diagram for an 8-bit control register read operation.

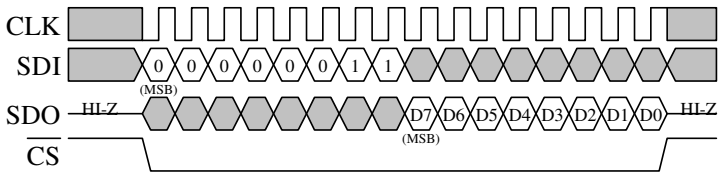


Figure 4 Timing Diagram for 8-Bit Control Register Read Operation

Accelerometer Read Back Operation

The KXP74 has an onboard 12-bit ADC that can sample, convert and read back sensor data at any time. Transmission of an 8-bit axis-conversion command (see Table 8) begins on the falling edge of nCS. After the eight clock cycles used to send the command, the host must wait for at least 40µs during the A/D conversion time. Note that all returned data is sent MSB first. Once the data is received, nCS must be returned high for 200nS before the next data request. Figure 5 on the following page shows the timing and register diagrams for the accelerometer 12-bit ADC read operation.

The Read Back Operation is a 3-byte SPI command. The first byte of SDI contains the command to convert one of the axes. The second and third bytes of SDO contain the 12 bits of the A/D result plus four bits of padding in the LSB to make a total of 16 bits. See Figure 6 below.

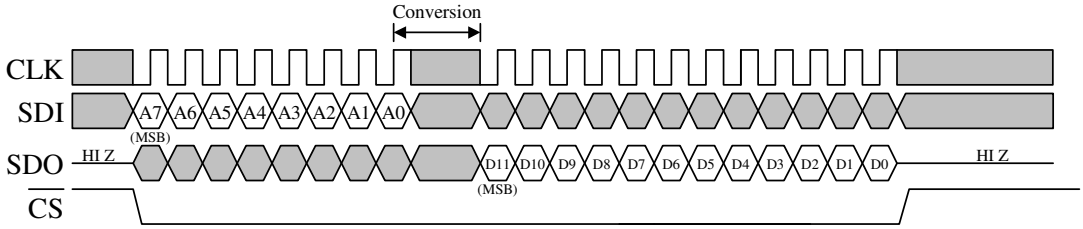


Figure 5 Timing Diagram for an A/D conversion and 12-Bit data read operation.

Axis Conversion Command

SDI	A7	A6	A5	A4	A3	A2	A1	A0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
	MSB																							
SDO	X	X	X	X	X	X	X	X	MSB D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X

X = Don't Care Bits

Conversion Read Back Data

Figure 6 Register Diagram for 12-Bit ADC Read Operation

SPI Commands

The accelerometer SPI interface uses an 8-bit command register to carry out all of its functions. The commands are given in Table 7.

Description	1st byte (SDI) (Command)
Convert X axis	0x00
Convert Z axis	0x01
Convert Y axis	0x02
Read Control Register	0x03
Write Control Register	0x04

Table 7 Command Register Bit Utilization

Convert X axis (0x00 or 0000 0000) samples the X-axis sensor data held on the filter cap, digitizes it and returns it as 12-bits through SDO.

Convert Z axis (0x01 or 0000 0001) samples the Z-axis sensor data held on the filter cap, digitizes it and returns it as 12-bits through SDO.

Convert Y axis (0x02 or 0000 0010) samples the Y-axis sensor data held on the filter cap, digitizes it and returns it as 12-bits through SDO.

Read Control Register (0x03 or 0000 0011) reads back the current contents of the control register and returns it as 8-bits through SDO.

Write Control Register (0x04 or 0000 0100) is used to initiate a write to the control register and set the operational mode of the accelerometer. The first byte initiates the write to the register, and the second byte specifies the operational mode.

Accelerometer Operational Modes

The 8-bit read/write control register selects the various operational modes of the accelerometer. Table 8 shows the bit assignments for the available modes.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	Speed_0	Speed_1	Enable	Self test	Parity

Table 8 Read/Write Control Register

Parity reports on even (0) or odd (1) EEPROM parity. A properly functioning part will return even (0) EEPROM parity. This bit is read-only and operates independently of the other modes.

The sampling and power modes controlled by the following bits are detailed below. These bits can be read or written.

Enable powers up the accelerometer for operation.
Enable = 1 – normal operation
Enable = 0 – low-power standby

Self test activates the self-test function for the sensor elements on all three axes. A correctly functioning part will increase all channel outputs by approximately 1g when Self test = 1 and Enable = 1. This bit can be read or written.

Speed_1 is one of two bits used to select the speed/power mode of the accelerometer. See Table 9 below.

Speed_0 is one of two bits used to select the speed/power mode of the accelerometer. See Table 9 below.

Accelerometer Sample/Power Modes

The KXP74's ASIC sequentially samples each sensor element in a "round robin" fashion. Note that this is a differential capacitance sampling of each sensor element, which stores an analog value on the filter cap for each axis. In its lowest noise/fastest sample mode, it samples each sensor at 32KHz. This mode also results in the maximum current draw. To reduce system power, four sensor sample rates can be selected in the ASIC control register. See Table 9 below.

Speed_1	Speed_0	Sensor Sample Rate
0	0	32KHz – lowest noise mode
0	1	8KHz
1	0	4KHz
1	1	2KHz – lowest power mode

Table 9 Sensor Sample Rate

Digital Accelerometer SPI Sequence

An example of a SPI sequence for reading sensor data is as follows:

1. Power up KXP74
2. nCS low to select
3. Write operational mode command to 8-bit control register – for example: 0x0404. The first 0x04 is the command to write to the control register, the second 0x04 sets the enable bit in the internal register.
4. nCS high for at least 200nS (SCLK = 5MHz)
5. nCS low to select
6. Send convert axis command – for example: 0x000000. The first 0x00 is the command to convert the X-channel. The second and third 0x00 are placeholders. There should be a minimum of 40µs between the first and second bytes in order to give the A/D conversion adequate time to complete.
7. The 12-bit A/D data is read in on the second and third SDO bytes.
8. nCS high for at least 200nS (SCLK = 5MHz)
9. Repeat data read cycle. Recommend reading X-axis, Y-axis, Z-axis, and the Control Register for each read cycle to verify the Control Register mode selection.