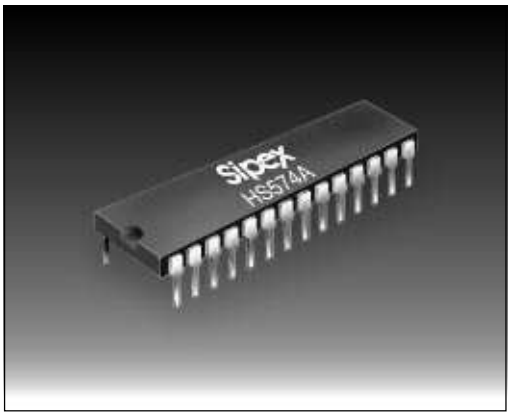
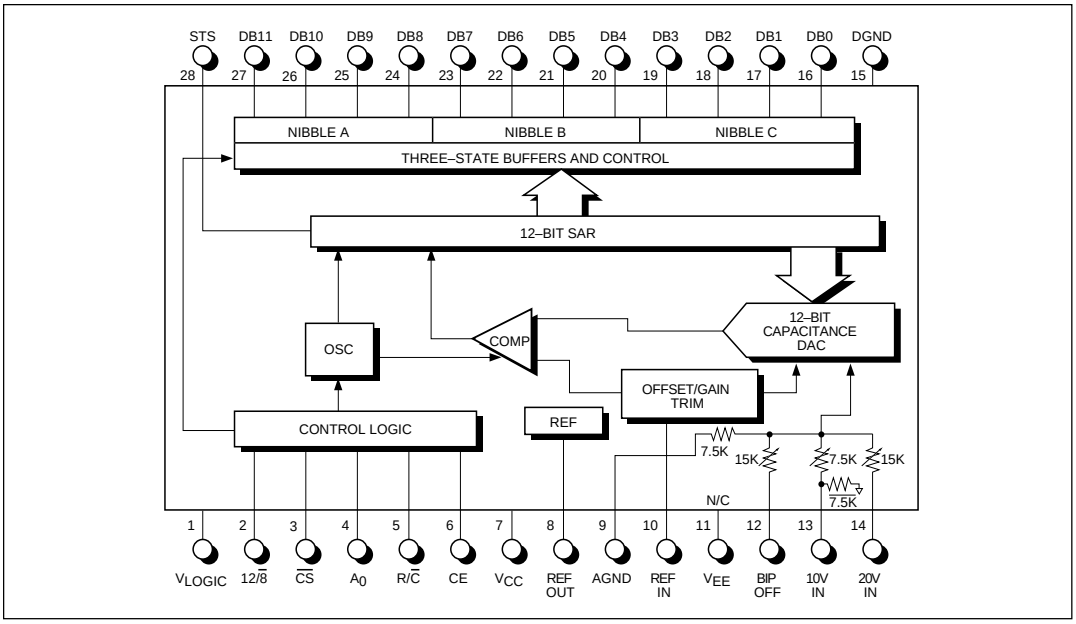
12–Bit Sampling A/D Converters

- Complete 12–bit A/D Converters with Sample–Hold, Reference, Clock and Tri–state Outputs
- Low Power Dissipation — 110mW Maximum
- 12–Bit Linearity Over Temperature
- Fast Conversion time:
  25µs Max (HS574A)
  15µs Max (SP674A)
- Monolithic Construction



DESCRIPTION…

The **HS574A/SP674A Series** are complete 12–bit successive–approximation A/D converters integrated on a single die with tri-state output latches, an internal reference, clock and a sample–hold. They feature 12–bit linearity over temperature, low power dissipation and fast conversion time. They are available in commercial and military temperature ranges.



ABSOLUTE MAXIMUM RATINGS

V_{CC} to Digital Common ..... 0 to +16.5V
V_{LOGIC} to Digital Common ..... 0 to +7V
Analog Common to Digital Common ..... ±1V
Control Inputs to Digital Common ..... –0.5V to V_{LOGIC} +0.5V
(CE, CS, A_0, 12/8, R/C)
Analog Inputs to Analog Common ..... ±16.5V
(REF IN, BIP OFF, $10V_{IN}$)
$20V_{IN}$ to Analog Common ..... ±24V
REF OUT ..... Indefinite short to common
Momentary short to V_{CC}
Power Dissipation 1000mW
Lead Temperature, Soldering ..... 300˚C, 10Sec
ΘJ/C ..... 45˚C/W
MTBF–25˚C Ground Base ..... 2.915 million hours
MTBF–125˚C Missile Launch ..... 10.16 thousand hours

* Inputs exceeding +30% or –30% of FS will cause erratic performance.

CAUTION:
ESD (ElectroStatic Discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Personnel should be properly grounded prior to handling this device. The protective foam should be discharged to the destination socket before devices are removed.

SPECIFICATIONS

(Typical @ 25°C with V_{CC} = +15V, V_{EE} = 0V, V_{LOGIC} = +5V unless otherwise noted)

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
RESOLUTION					
All models			12	Bits	
ANALOG INPUTS					
Input Ranges					
Bipolar		±5, ±10		V	
Unipolar		0 to +10, 0 to +20		V	
Input Impedance					
10 Volt Input	3.75		6.25	KΩ	
20 Volt Input	15		25	KΩ	
DIGITAL INPUTS					
Logic Inputs CE, $\overline{CS}$ R/$\overline{C}$, A_0, 12/$\overline{8}$					
Logic 1	+2.4		+5.5	V	
Logic 0	–0.3		+0.8	V	
Current		±0.1	±50	µA	0V to +5.5V Input
Capacitance		5		pF	
12/8 Control Input		Hardwire to V_{LOGIC} or DIGITAL COMMON (SP574A only)			
DIGITAL OUTPUTS					
Logic Outputs DB_{11}–DB_0, STS					
Logic 1	+2.4			V	$I_{SOURCE} \leq 500\mu A$
Logic 0			+0.4	V	$I_{SINK} \leq 1.6mA$
Leakage (High Z State)			±40	µA	Data bits only
Capacitance		5		pF	
Parallel Data Output Codes					
Unipolar		Positive true binary			
Bipolar		Positive true offset binary			
REFERENCE					
Internal			10.00 ±0.1	V	
Output Current		2		mA	Note 1
CONVERSION TIME					
HS574A					
12–Bit Conversion	13		25	µs	
8–Bit Conversion	10		19	µs	
SP674A					
12–Bit Conversion	9		15	µs	
8–Bit Conversion	6		11.25	µs	

SPECIFICATIONS *(continued)*

(Typical @ 25°C with V_{CC} = +15V, V_{EE} = 0V, V_{LOGIC} = +5V unless otherwise noted)

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
ACCURACY					
Linearity Error @ 25°C					
–J, –S			±1.0	LSB	@ 25°C and T_{MIN} to T_{MAX}
–K, –L, –T, –U			±0.5	LSB	@ 25°C and T_{MIN} to T_{MAX}
Differential Linearity Error					Note 2
–J, –S	11			Bits	@ 25°C
	11			Bits	T_{MIN} to T_{MAX}
–K, –L, –T, –U	12			Bits	@ 25°C
	12			Bits	T_{MIN} to T_{MAX}
Offset					Note3
Unipolar		±2		LSB	
Bipolar					
–J, –S		±10		LSB	
–K, –L, –T, –U		±4		LSB	
Full Scale (Gain) Error					% of full scale; T_{MIN} to T_{MAX}
			±0.3	%FS	Note 4
–J			±0.5	%FS	No adjustment @ 25°C
			±0.22	%FS	With adjustment @ 25°C
–K			±0.4	%FS	No adjustment @ 25°C
			±0.12	%FS	With adjustment @ 25°C
–L			±0.35	%FS	No adjustment @ 25°C
			±0.05	%FS	With adjustment @ 25°C
–S			±0.8	%FS	No adjustment @ 25°C
			±0.5	%FS	With adjustment @ 25°C
–T			±0.6	%FS	No adjustment @ 25°C
			±0.25	%FS	With adjustment @ 25°C
–U			±0.4	%FS	No adjustment @ 25°C
			±0.12	%FS	With adjustment @ 25°C
STABILITY					
Unipolar Offset					
–J			±10	ppm/°C	T_{MIN} to T_{MAX}
–K, –L, –S			±5	ppm/°C	T_{MIN} to T_{MAX}
–T, –U			±2.5	ppm/°C	T_{MIN} to T_{MAX}
Bipolar Offset					
–J, –S			±10	ppm/°C	T_{MIN} to T_{MAX}
–K, –L, –T			±5	ppm/°C	T_{MIN} to T_{MAX}
–U			±2.5	ppm/°C	T_{MIN} to T_{MAX}
Gain (Scale Factor)					
–J, –S			±50	ppm/°C	T_{MIN} to T_{MAX}
–K, –T			±25	ppm/°C	T_{MIN} to T_{MAX}
–L, –U			±10	ppm/°C	T_{MIN} to T_{MAX}
PSRR					
V_{LOGIC}			±0.5	LSB	+4.5V ≤ V_{LOGIC} ≤ +5.5V
V_{CC}					Note 5
–J, –S			±2	LSB	
–K, –L, –T, –U			±1	LSB	
POWER REQUIREMENTS					
V_{LOGIC}	+4.5		+5.5	V	
I_{LOGIC}					
HS574A		1	3	mA	
SP674A		1	3	mA	
V_{CC}	+11.4		+16.5	V	
I_{CC}					
HS574A		7	9	mA	
SP674A		7	9	mA	

SPECIFICATIONS *(continued)*

(Typical @ 25°C with V_{CC} = +15V, V_{EE} = 0V, V_{LOGIC} = +5V unless otherwise noted)

PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Power Dissipation					
HS574A		110	150	mW	
SP674A		110	150	mW	
ENVIRONMENTAL					
Operating Temperature Range					
–J, –K, –L	0		+70	°C	
–S, –T, –U	–55		+125	°C	
Storage Temperature Range					
–J, –K, –L	–40		+85	°C	
–A, –S, –T, –U	–65		+150	°C	

Notes:

1. Available for external loads. External load should not change during conversion. When supplying an external load and operating on a +12V supply, a buffer amplifier must be provided for the reference output.
2. Minimum resolution for which no missing codes are guaranteed.
3. Externally adjustable to zero. See *Calibration* information.
4. Fixed 50Ω resistor between REF OUT and REF IN.
5. +13.5V ≤ V_{CC} ≤ +16.5V or +11.4V ≤ V_{CC} ≤ +12.6V.
6. Specifications are identical for all models unless otherwise noted.

PIN ASSIGNMENTS...

PIN	FUNCTION	PIN	FUNCTION
1	V_{LOGIC}	28	STS
2	12/$\overline{8}$	27	DB_{11}(MSB)
3	$\overline{CS}$	26	DB_{10}
4	A_0	25	DB_9
5	R/$\overline{C}$	24	DB_8
6	CE	23	DB_7
7	V_{CC}	22	DB_6
8	REF OUT	21	DB_5
9	ANA GND(AC)	20	DB_4
10	REF IN	19	DB_3
11	N/C*	18	DB_2
12	BIP OFF	17	DB_1
13	$10V_{IN}$	16	DB_0(LSB)
14	$20V_{IN}$	15	DIG. GND

*HS574A – This pin is not connected to the device; it can be tied to –15V, ground, or left floating.

*SP674A – This pin is not connected to the device; V_{EE} is generated internally.

FEATURES...

The **HS574A/SP674A** feature standard bipolar and unipolar input ranges of 10V and 20V. Input ranges are controlled by a bipolar offset pin and laser-trimmed for specified linearity, gain and offset accuracy. Power requirements are +5V and +12V to +15V with a maximum dissipation of 150mW at the specified voltages. Conversion times of 8µs, 10µs, 15µs and 25µs are available, as are units with 10, 25 or 50ppm/°C temperature coefficients for flexible matching to specific application requirements.

The **HS574A/SP674A** are available in six product grades for each conversion time. The –J, –K and –L models are specified over 0˚C to + 70˚C commercial temperature range; the –S, –T and –U models are specified over the –55˚C to +125˚C military temperature range. Processing in accordance with MIL–STD–883C is also available. The HS574A/SP674A are packaged in a 28–pin CerDIP. Please consult the factory for other packaging options.

CIRCUIT OPERATION...

The **HS574A/SP674A** are complete 12–bit analog-to-digital converters with integral voltage reference, comparator, successive–approximation register (SAR), sample–and–hold, clock, output buffers and control circuitry. The high level of integration of the **HS574A/SP674A** means they require few external components.

When the control section of the **HS574A/SP674A** initiates a conversion command, the clock is enabled and the successive–approximation register is reset to all zeros. Once the conversion cycle begins, it can not be stopped or re–started and data is not available from the output buffers.

The SAR, timed by the clock, sequences through the conversion cycle and returns an end–of–convert flag to the control section of the ADC. The clock is then disabled by the control section, the output status goes low, and the control section is enabled to allow the data to be read by external command.

The internal **HS574A/SP674A** 12–bit CDAC is sequenced by the SAR starting from the MSB to the LSB at the beginning of the conversion cycle to provide an output voltage from the CDAC that is equal to the input signal voltage (which is divided by the input voltage divider network). The comparator determines whether the addition of each successively–weighted bit voltage causes the CDAC output voltage summation to be greater or less than the input voltage; if the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12–bit binary code which accurately represents the input signal to within $\pm\frac{1}{2}$ LSB.

The internal reference provides the voltage reference to the CDAC with excellent stability over temperature and time. The reference is trimmed to 10.00 Volts ±1% and can supply up to 2mA to an external load in addition to that required to drive the reference input resistor (1mA) and offset resistor (1mA) when operating with ±15V supplies. If the **HS574A/SP674A** is used with ±12V supplies, or if external current must be supplied over the full temperature range, an external buffer amplifier is recommended. Any external load on the **HS574A/SP674A** reference must remain constant during conversion.

The sample and hold is a default function by virtue of the CDAC architecture. Therefore the majority of the S/H specifications are included within the A/D specifications.

Sample–and–Hold Function

Although there is no sample-and-hold circuit in the classical sense, the sampling nature of the capacitive DAC makes the **HS574A/SP674A** appear to have a built in sample and hold. This sample and hold action substantially increases the usefulness of the **HS574A/SP674A** over that of similar competing devices.

Note that even though the user may use an external sample and hold for very high frequency inputs, the internal sample and hold still provides a very useful isolation function. Once the internal sample is taken by the CDAC capacitance, the input of the **HS574A/SP674A** is disconnected from the input. This prevents transients occurring during conversion from being inflicted upon the attached buffer. All other 574/674 circuits will cause a transient load current on

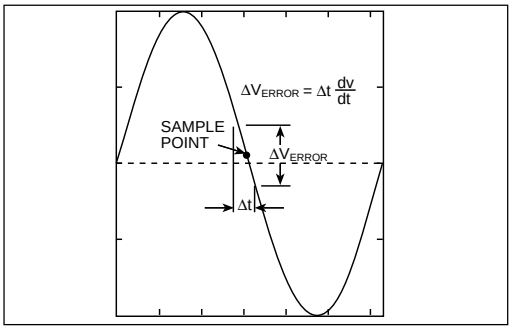


Figure 1. Aperture Uncertainty

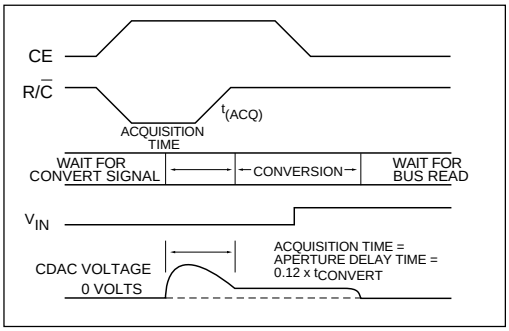


Figure 3. Sample–and–Hold Function

the input which will upset the buffer output and may add error to the conversion itself.

Furthermore, the isolation of the input after the acquisition time in the **HS574A/SP674A** allows the user an opportunity to release the hold on an external sample-and-hold and start it tracking the next sample. This will increase system throughput with the user's existing components.

When using an external S/H, the **HS574A/SP674A** acts as any other 574–type device because the internal S/H is transparent. The sample/hold function in the **HS574A/SP674A** is inherent to the capacitor DAC structure, and its timing characteristics are determined by the internally generated clock. However, for multiplexer operation, the internal S/H may eliminate the need for an external S/H. The operation of the S/H function is internal to the **HS574A/SP674A** and is controlled through the normal R/$\overline{C}$ control line (refer to *Figure 3*). When the R/$\overline{C}$ line makes a negative transition, the **HS574A/SP674A** starts the timing of the sampling and conversion. The first two clock cycles are allocated to signal acquisition of the input by the CDAC (this time is defined as t_{ACQ}). Following these two cycles, the input sample is taken and held. The A/D conversion follows this cycle with the duration controlled by the internal clock cycle, which is determined by the specific product model. Note that because the sample is taken relative to the R/$\overline{C}$ transition, t_{ACQ} is also the traditional "aperture delay" of this internal sample and hold. Since t_{ACQ} is measured in clock cycles, its duration will vary with the internal clock frequency. This results in T_{ACQ} = 2.9µ sec ±1.1µsecs between units and over temperatures.

Offset, gain and linearity errors of the S/H circuit, as well as the effects of its droop rate, are included in the overall specs for the **HS574A/SP674A**.

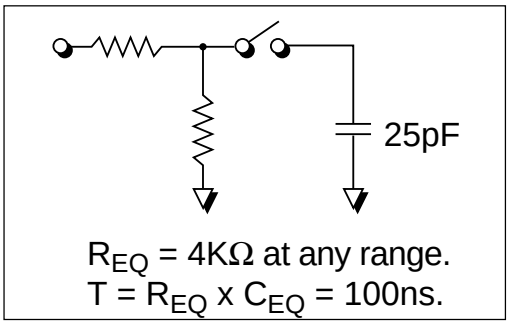


Figure 2. Equivalent SP574A Input Circuit

USING THE SPX74A SERIES

Typical Interface Circuit

The **HS574A/SP674A** is a complete A/D converter that is fully operational when powered up and issued a Start Convert Signal. Only a few external components are necessary. *Figure 4* depicts a typical interface circuit for operating the **HS574A/SP674A** in a unipolar input mode. *Figure 5* depicts a typical interface circuit for operating the **HS574A/SP674A** in a bipolar input mode. Further information is given in the following sections on these connections, but first a few considerations concerning board layout to achieve the best operation.

For each application of this device, strict attention must be given to power supply decoupling, board layout (to reduce pickup between analog

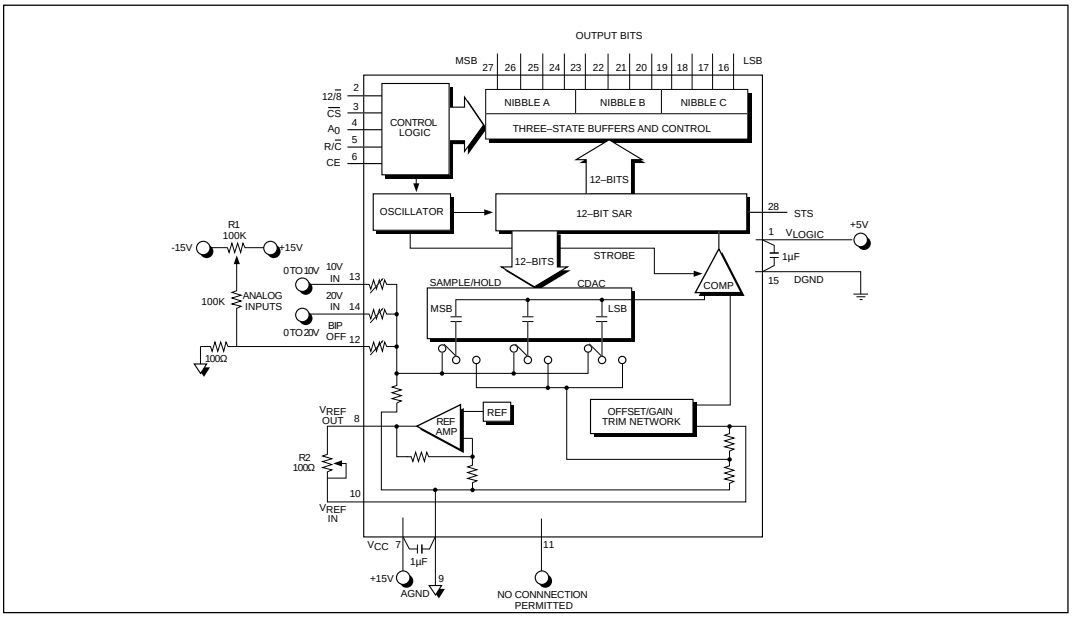


Figure 4. Unipolar Input Connections

and digital sections), and grounding. Digital timing, calibration and the analog signal source must be considered for correct operation.

To achieve specified accuracy, a double–sided printed circuit board with a copper ground plane on the component side is recommended. Keep analog signal traces away from digital lines. It is best to lay the PC board out such that there is an analog section and a digital section with a single point ground connection between the two through an RF bead. If this is not possible, run analog

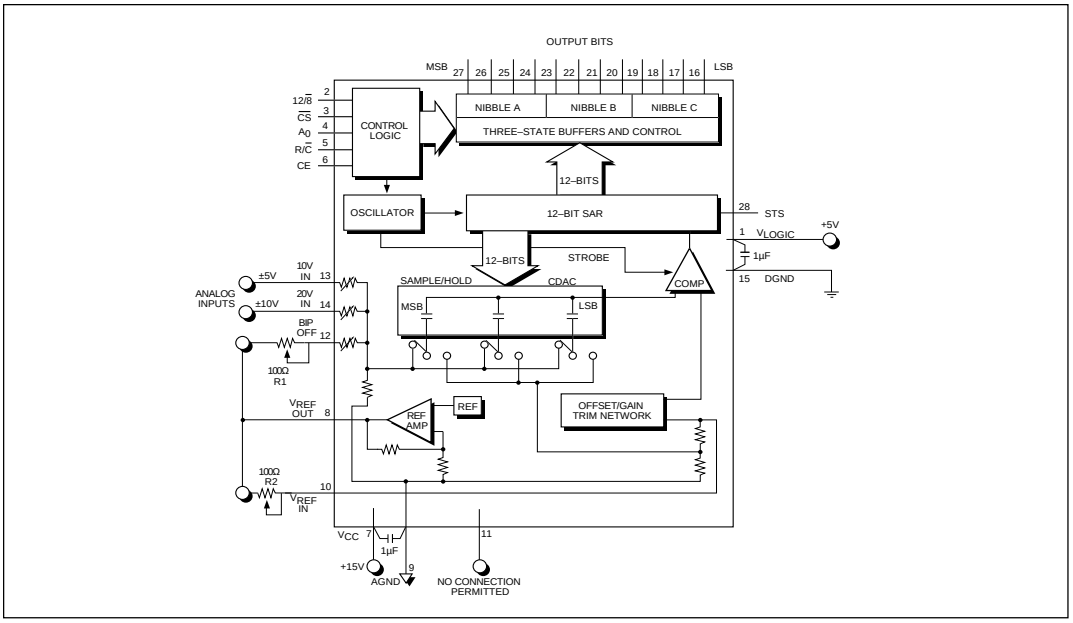


Figure 5. Bipolar Input Connections

signals between ground traces and cross digital lines at right angles only.

Grounding Considerations

Any ground path from the analog and digital ground should be as low resistance as possible to accommodate the ground currents present with this device.

The analog ground current is approximately 6mA DC while the digital ground is 3mA DC. The analog and digital common pins should be tied together as close to the package as possible to guarantee best performance. The code–dependent currents flow through the V_{LOGIC} and V_{CC} terminals and not through the analog and digital common pins.

Power Supplies

The supply voltages for the **SPx74A** must be kept as quiet as possible from noise pickup and also regulated from transients or drops. Because the part has 12–bit accuracy, voltage spikes on the supply lines can cause several LSB deviations on the output. Switching power supply noise can be a problem. Careful filtering and shielding should be employed to prevent the noise from being picked up by the converter.

Capacitor bypass pairs are needed from each supply pin to its respective ground to filter noise and counter the problems caused by the variations in supply current. A 10µF tantalum and a 0.1µF ceramic type in parallel between V_{LOGIC} (pin 1) and digital common (pin15), and V_{CC} (pin 7) and analog common (pin 9) is sufficient. V_{EE} is generated internally so pin 11 may be grounded or connected to a negative supply if the **SPx74A** is being used to upgrade an already existing design.

CALIBRATION AND CONNECTION PROCEDURES

Unipolar

The calibration procedure consists of adjusting the converter's most negative output to its ideal value for offset adjustment, and then adjusting the most positive output to its ideal value for gain adjustment.

Starting with offset adjustment and referring to *Figure 4*, the midpoint of the first LSB increment should be positioned at the origin to get an output code of all 0s. To do this, an input of +½ LSB or +1.22mV for the 10V range and +2.44mV for the 20V range should be applied to the **SPx74A**. Adjust the offset potentiometer R_1 for code transition flickers between 0000 0000 0000 and 0000 0000 0001.

The gain adjustment should be done at positive full scale. The ideal input corresponding to the last code change is applied. This is 1½LSB below the nominal full scale which is +9.9963V for the 10V range and +19.9927V for the 20V range. Adjust the gain potentiometer R_2 for flicker between codes 1111 1111 1110 and 1111 1111 1111. If calibration is not necessary for the intended application, replace R_2 with a 50Ω, 1% metal film resistor and remove the network ana-

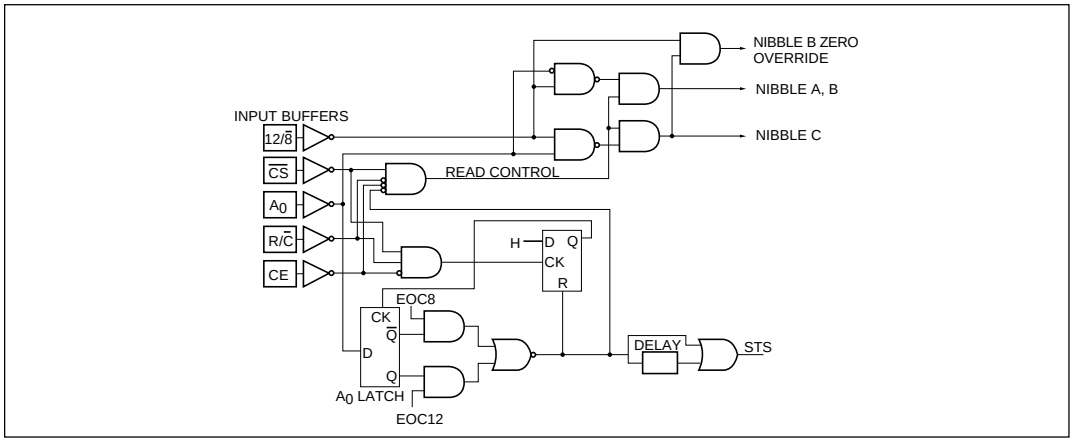


Figure 6. SPx74A Control Logic

log input to pin 13 for the 0V to 10V range or to pin 14 for the 0V to 20V range.

Bipolar

The gain and offset errors listed in the specifications may be adjusted to zero using the potentiometers R_1 and R_2 (See *Figure 5*). If adjustment is not needed, either or both pots may be replaced by a 50Ω, 1% metal film resistor.

To calibrate, connect the analog input signal to pin 13 for a ±5V range or to pin 14 for a ±10V range. First apply a DC input voltage ½ LSB above negative full scale which is –4.9988V for the ±5V range or –9.9976V for the ±10V range. Adjust the offset potentiometer R_1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage 1½ LSB below positive full scale which is +4.9963V for the ±5 range or +9.9927V for the ±10V range. Adjust the gain potentiometer R_2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

Alternative

The 100Ω potentiometer R_2 provides gain adjust for 10V and 20V ranges. In some applications, a full scale of 10.24V (for and LSB of 2.5mV) or 20.48 (for an LSB of 5.0mV) is more convenient. For these, replace R_2 by a 50Ω, 1% metal film resistor. Then to provide gain adjust for the 10.24 range, add a 200Ω potentiometer and a 95Ω fixed resistor, all in series with pin 13. For the 20.48V range, add a 500Ω potentiometer and a 200Ω fixed resistor in series with pin 14.

CONTROLLING THE SPx74A

The **SPx74A** can be operated by most microprocessor systems due to the control input pins and on–chip logic. It may also be operated in the "stand–alone" mode and enabled by the R/$\overline{C}$ input pin. Full microprocessor control consists of selecting an 8– or 12–bit conversion cycle, initiating the conversion, and reading the output data when ready. The output read has the options of choosing either 12–bits at once or 8–bits followed by 4–bits in a left–justified format. All five control inputs are TTL/CMOS compatible and include 12/$\overline{8}$, $\overline{CS}$, A_0, R/$\overline{C}$ and CE. The use of these inputs in controlling the converter's operation is shown in *Table 1*, and the internal control logic is shown in a simplified schematic in *Figure 6*.

Conversion Start

A conversion may be initiated by a logic transition on any of the three inputs: CE, $\overline{CS}$ R/$\overline{C}$, as shown in *Table* 1. The last of the three to reach the correct state starts the conversion, so one, two or all three may be dynamically controlled. The nominal delay from each is the same and all three may change state simultaneously. In order to assure that a particular input controls the start of conversion, the other two should be setup at least 50ns earlier. Refer to the convert mode timing specifications. The Convert Mode timing diagram is shown in *Figure 8*.

The output signal STS is the status flag and goes high only when a conversion is in progress. While STS is high, the output buffers remain in a high impedance state so that data can not be read. Also, when STS is high, an additional Start Convert will not reset the converter or reinitiate a conversion. Note, if A_0 changes state after a conversion begins, an additional Start Convert command will latch the new state of A_0 and possibly cause a wrong cycle length for that conversion (8–versus 12–bits).

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	x	x	x	x	None
x	1	x	x	x	None
↓	0	0	x	0	Initiate 12–Bit Conversion
↓	0	0	x	1	Initiate 8–Bit Conversion
1	↓	0	x	0	Initiate 12–Bit Conversion
1	↓	0	x	1	Initiate 8–Bit Conversion
1	0	↓	x	0	Initiate 12–Bit Conversion
1	0	↓	x	1	Initiate 8–Bit Conversion
1	0	1	1	x	Enable 12–Bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's plus 4 Trailing Zeroes

Table 1. SPx74A Control Input Truth Table

Conversion Length

A conversion start transition latches the state of A_0 as shown in *Figure 8* and *Table 1*. The latched state determines if the conversion stops with 8–bits (A_0 high) or continues for 12–bits (A_0 low). If all 12–bits are read following an 8–bit conversion, the three LSB's will be a logic "0" and DB_3 will be a logic "1". A_0 is latched because it is also involved in enabling the output buffers as explained elsewhere. No other control inputs are latched.

Stand–Alone Operation

The simplest interface is a control line connected to R/$\overline{C}$. The other controls must be tied to known states as follows: CE and 12/$\overline{8}$ are wired high, A_0 and $\overline{CS}$ are wired low. The output data arrives in words of 12–bits each. The limits on R/$\overline{C}$ duty cycle are shown in *Figures 9* and *10*. The duty cycle may be within and including the extremes shown in the specifications. In general, data may be read when R/$\overline{C}$ is high unless STS is also high, indicating a conversion is in progress.

Reading Output Data

The output data buffers remain in a high impedance state until the following four conditions are met: R/$\overline{C}$ is high, STS is low, CE is high and $\overline{CS}$ is low. The data lines become active in response to these four conditions, and output data according to the conditions of the control lines 12/$\overline{8}$ and A_0. The timing diagram for this process is shown in *Figure 11*. When 12/$\overline{8}$ is high, all 12 data outputs become active simultaneously and the A_0 input is ignored. The 12/$\overline{8}$ input is usually tied high or low; it is TTL/CMOS compatible. When 12/$\overline{8}$ is low, the output is separated into two 8–bit bytes as shown below:

BYTE 1	BYTE2
xxxx xxxx	xxxx 0000
MSB	LSB

This configuration makes it easy to connect to an 8–bit address bus as shown in *Figure 7*. The A_0 control can be connected to the least significant bit of the data bus in order to store the output data into two consecutive memory locations. When A_0 is pulled low, the 8 MSB's are enabled only. When A_0 is high, the 8 MSB's are disabled, bits 4 through 7 are forced to a zero and the four LSB's are enabled. The two byte format is "left justified data" as shown above and can be considered to have a decimal point or binary to the left of byte 1.

A_0 may be toggled without damage to the converter at any time. Break–before–make action is guaranteed between the two data bytes. This assures that the outputs which are strapped together in *Figure 11* will never be enabled at the same time.

In *Figure 11*, it can be seen that a read operation usually begins after the conversion is complete and STS is low. If earlier access is needed, the read can begin no later than the addition of times t_{DD} and t_{HS} before STS goes low.

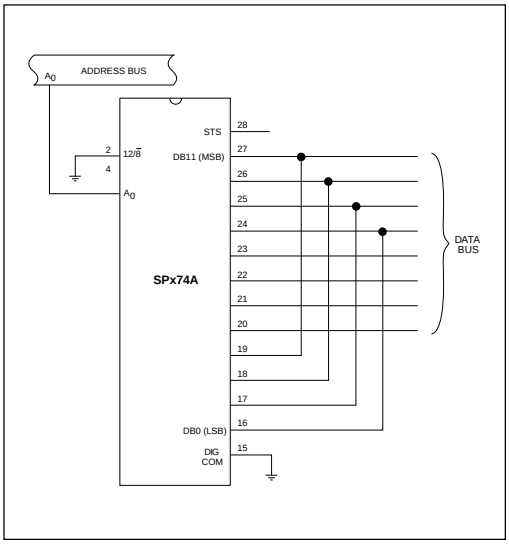
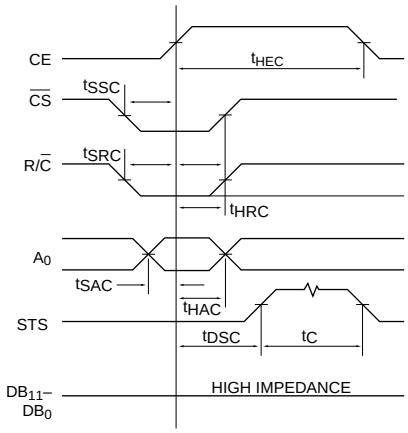


Figure 7. Interfacing SPx74A to 8–Bit Interface Bus

CONVERT MODE TIMING



CHARACTERISTICS

Typical @ 25˚C, V_{CC} = +15V or +10V, V_{LOGIC} = +5V, V_{EE} = 0V, unless otherwise specified.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{DSC} STS Delay from CE			200	ns	
t_{HEC} CE Pulse Width	50			ns	
t_{SSC} CS to CE Setup	50			ns	
t_{HSC} CS Low during CE High	50			ns	
t_{SRC} R/$\overline{C}$ to CE Setup	50			ns	
t_{HRC} R/$\overline{C}$ Low during CE High	50			ns	
t_{SAC} A_0 to CE Setup	0			ns	
t_{HAC} A_0 Valid during CE High	50			ns	
t_C Conversion Time[1, 3, 4]	See specifications				

NOTES:
1. Parameters guaranteed by design and sample tested.
2. Parameters 100% tested @ 25˚C on special orders.
3. 100% tested.
4. T_{MIN} to T_{MAX}.

Figure 8. Convert Mode Timing

STAND–ALONE MODE TIMING CHARACTERISTICS

Typical @ 25˚C, V_{CC}= +15V or +12V, V_{LOGIC} = +5V, V_{EE} =0V, unless otherwise specified.

PARAMETER		MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{HRL}	Low R/$\overline{C}$ Pulse Width [2]	50			ns	
t_{DS}	STS Delay from R/$\overline{C}$ [2]			200	ns	
t_{HDR}	Data Valid After R/$\overline{C}$ Low [2]		25		ns	
t_{HS}	STS Delay After Data Valid [2]	300		1000	ns	
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			ns	
t_{DDR}	Data Access Time			150	ns	

NOTES:
1. Parameters guaranteed by design and sample tested.
2. Parameters 100% tested @ 25˚C on special orders.

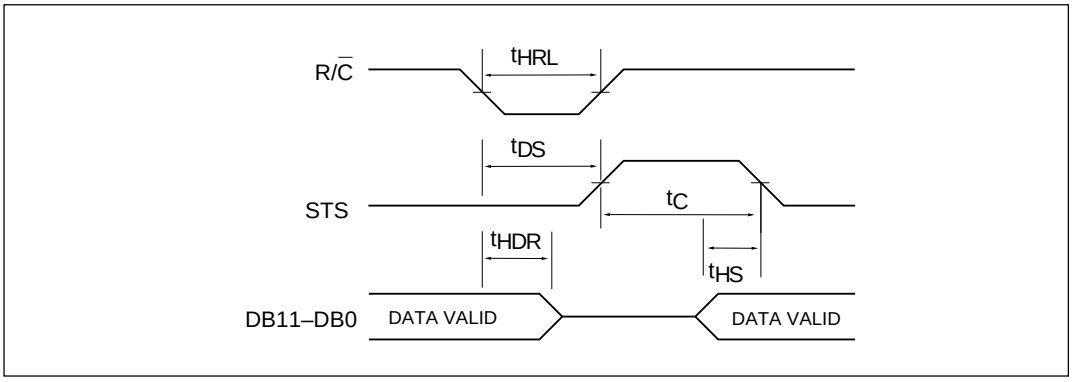


Figure 9. Low Pulse for R/$\overline{C}$ — Outputs Enabled After Conversion

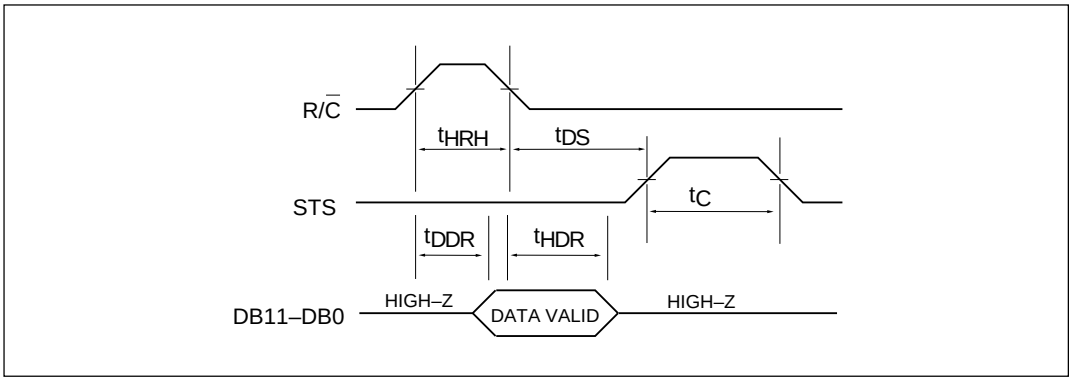
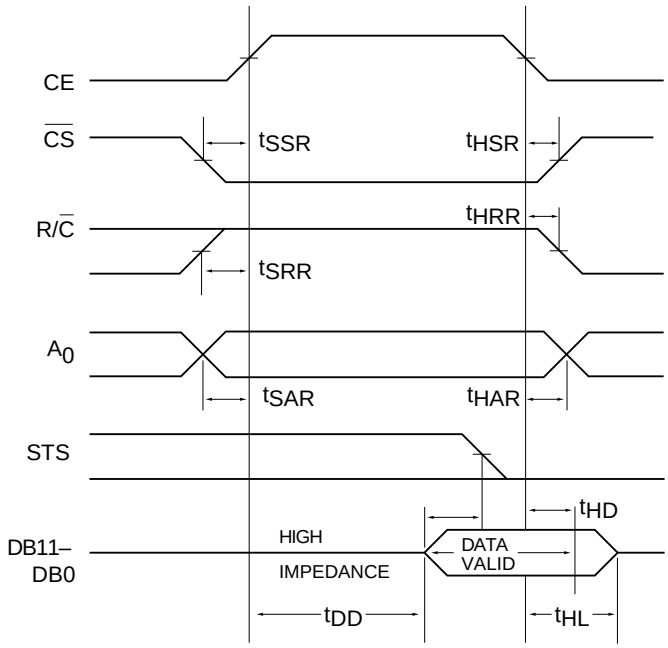


Figure 10. High Pulse For R/$\overline{C}$ — Outputs Enabled While R/C is High, Otherwise High Impedance

READ MODE TIMING



CHARACTERISTICS

Typical @ 25˚C, V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = 0V, unless otherwise specified.

PARAMETER		MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{DD}	Access Time From CE[2]			150	ns	
t_{HD}	Data Valid After CE Low[2]	25			ns	
t_{HL}	Output Float Delay[2]			150	ns	
t_{SSR}	CS to CE Setup	50	0		ns	
t_{SRR}	R/$\overline{C}$ to CE Setup	0	0		ns	
t_{SAR}	A_0 to CE Setup	50			ns	
t_{HSR}	CS Valid After CE Low	0	0		ns	
t_{HRR}	R/$\overline{C}$ High After CE Low	0	50		ns	
t_{HAR}	A_0 Valid After CE Low	50			ns	
t_{HS}	STS Delay After Data Valid	300		1000	ns	

NOTES:
1. Parameters guaranteed by design and sample tested.
2. Parameters 100% tested @ 25˚C on special orders.

Figure 11. Read Mode Timing

ORDERING INFORMATION

Model	No Missing Codes to;	Linearity	Gain TC	Temperature Range	Package Type
25µs Conversion Time					
HS574AA	11 Bits	±1.0 LSB	50ppm/°C	–40°C to +85°C	28–pin, 0.6" Ceramic DIP
HS574AB	12 Bits	±0.5 LSB	27ppm/°C	–40°C to +85°C	28–pin, 0.6" Ceramic DIP
HS574AC	12 Bits	±0.5 LSB	10ppm/°C	–40°C to +85°C	28–pin, 0.6" Ceramic DIP
HS574AJ	11 Bits	±1.0 LSB	50ppm/°C	0°C to +70°C	28–pin, 0.6" Ceramic DIP
HS574AK	12 Bits	±0.5 LSB	27ppm/°C	0°C to +70°C	28–pin, 0.6" Ceramic DIP
HS574AL	12 Bits	±0.5 LSB	10ppm/°C	0°C to +70°C	28–pin, 0.6" Ceramic DIP
HS574AS	11 Bits	±1.0 LSB	50ppm/°C	–55°C to +125°C	28–pin, 0.6" Ceramic DIP
HS574AT	12 Bits	±0.5 LSB	25ppm/°C	–55°C to +125°C	28–pin, 0.6" Ceramic DIP
HS574AU	12 Bits	±0.5 LSB	12.5ppm/°C	–55°C to +125°C	28–pin, 0.6" Ceramic DIP
HS574AS/883*	11 Bits	±1.0 LSB	50ppm/°C	–55°C to +125°C	28–pin, 0.6" Ceramic DIP
HS574AT/883*	12 Bits	±0.5 LSB	25ppm/°C	–55°C to +125°C	28–pin, 0.6" Ceramic DIP
HS574AU/883*	12 Bits	±0.5 LSB	12.5ppm/°C	–55°C to +125°C	28–pin, 0.6" Ceramic DIP
15µs Conversion Time					
SP674AA	11 Bits	±1.0 LSB	50ppm/°C	–40°C to +85°C	28–pin, 0.6" Ceramic DIP
SP674AB	12 Bits	±0.5 LSB	27ppm/°C	–40°C to +85°C	28–pin, 0.6" Ceramic DIP
SP674AC	12 Bits	±0.5 LSB	10ppm/°C	–40°C to +85°C	28–pin, 0.6" Ceramic DIP
SP674AJ	11 Bits	±1.0 LSB	50ppm/°C	0°C to +70°C	28–pin, 0.6" Ceramic DIP
SP674AK	12 Bits	±0.5 LSB	27ppm/°C	0°C to +70°C	28–pin, 0.6" Ceramic DIP
SP674AL	12 Bits	±0.5 LSB	10ppm/°C	0°C to +70°C	28–pin, 0.6" Ceramic DIP
SP674AS	11 Bits	±1.0 LSB	50ppm/°C	–55°C to +125°C	28–pin, 0.6" Ceramic DIP
SP674AT	12 Bits	±0.5 LSB	25ppm/°C	–55°C to +125°C	28–pin, 0.6" Ceramic DIP
SP674AU	12 Bits	±0.5 LSB	12.5ppm/°C	–55°C to +125°C	28–pin, 0.6" Ceramic DIP
SP674AS/883*	11 Bits	±1.0 LSB	50ppm/°C	–55°C to +125°C	28–pin, 0.6" Ceramic DIP
SP674AT/883*	12 Bits	±0.5 LSB	25ppm/°C	–55°C to +125°C	28–pin, 0.6" Ceramic DIP
SP674AU/883*	12 Bits	±0.5 LSB	12.5ppm/°C	–55°C to +125°C	28–pin, 0.6" Ceramic DIP

* MIL–STD–883C processing.

NOTE: Electrical specifications for –AA, –AB and –AC grades are the same as –AJ, –AK, and –AL models respectively, with the exception of extended operating temperature range performance from –40°C to +85°C.

Please consult the factory for other packaging options.