MN8390-C

LCD Panel Source Driver

■ Overview

The MN8390-C is for displaying an analog video signal on a TFT color liquid crystal display panel in such applications as LCD television sets and video cameras.

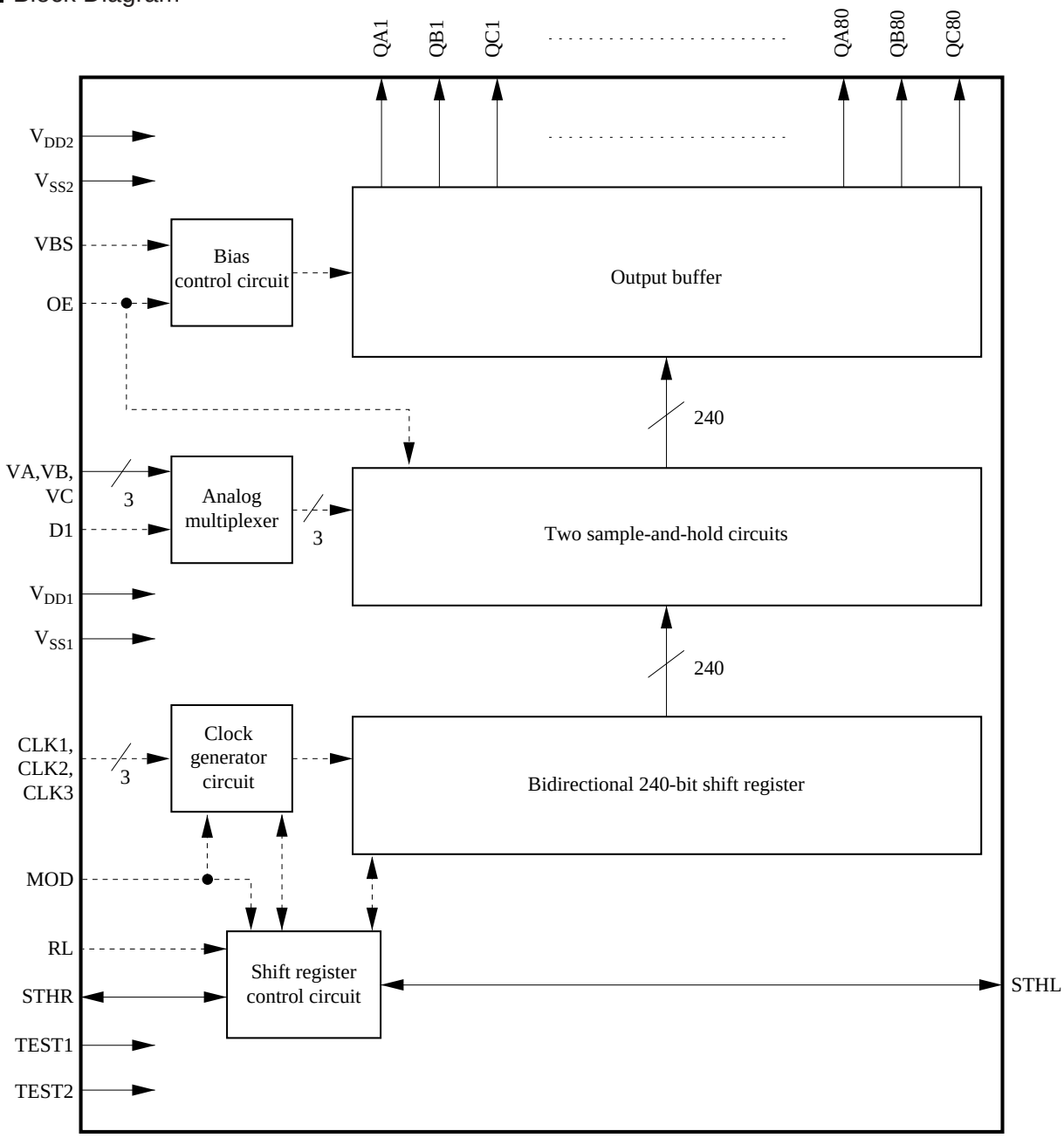
■ Features

- Lower power consumption and reduced EMI emissions owing to digital 3.0 volt power supply and analog 5.0 volt power supply
- Broad dynamic range of 4.6 V (for power supply voltage of 5.0 V)
- Low discrepancies between output pins: ±20 mV (typ.)
- 240 output channels
- Support for striped and delta panel layouts by switching analog (R, G, B) signals
- Support for sequential sampling mode (with CLK1 to CLK3 inputs)
- Support for serial cascade connections
- Automatic clock suspension after reading specified amount of data
- Choice of shift register shift directions (right/left)

■ Applications

- LCD television sets and video cameras

■ Block Diagram



■ Pin Descriptions

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Pin Name</th><th>I/O</th><th>Function Description</th></tr>
<tr><td>99 to 102
21 to 24</td><td>STHR
STHL</td><td>Shift data I/O</td><td>I/O</td><td>These are I/O pins for the bidirectional shift register. The RL pin controls their I/O directions.
<table>
<tr><th>RL</th><th>STHR</th><th>STHL</th></tr>
<tr><td>H</td><td>Input</td><td>Output</td></tr>
<tr><td>L</td><td>Output</td><td>Input</td></tr>
</table>
(1) Input
The pins provide input data to the shift register's first stage. The shift register reads in this data at the rising edge of the CLK1 signal.
(2) Output
In a cascade connection, the pins provide the data for the synchronizing output stage synchronized with the rising edge of the CLK1 signal.</td></tr>
<tr><td>27 to 30</td><td>RL</td><td>Shift direction control</td><td>I</td><td>This pin controls the shift direction for the bidirectional shift register.
RL="H" : QA1→ QB1→ QC1→ → QC80
RL="L" : QC80→ QB80→ QA80→ → QA1</td></tr>
<tr><td>42 to 45
37 to 40
32 to 35</td><td>CLK1 to 3</td><td>Clock input</td><td>I</td><td>These pins provide the shift clock signals that the sample-and-hold circuits use to generate the data for the LCD drive output pins (QA1-QC80).
The following lists the relationships between these clock signals and the output pins.
CLK1 RL="H": QA1 to QA80
RL="L": QC1 to QC80
CLK2: QB1 to QB80
CLK3 RL="H": QC1 to QC80
RL="L": QA1 to QA80</td></tr>
<tr><td>70 to 73</td><td>OE</td><td>Output enable</td><td>I</td><td>At each rising edge of this signal, the MN8390-C switches between its two sample-and-hold circuits and initiates output of new data. When the outputs reach the drive potential, the MN8390-C automatically reduces the drive power, but maintains the outputs at the drive potential.</td></tr>
<tr><td>47 to 50</td><td>D1</td><td>Analog signal swiching</td><td>I</td><td>This pin controls the mapping between the three analog inputs (VA, VB, and VC) and the drive outputs (QA, QB, and QC).
<table>
<tr><th>D1</th><th>Input</th><th>Output</th></tr>
<tr><td rowspan="3">L</td><td>VA</td><td>QA1 to QA80</td></tr>
<tr><td>VB</td><td>QB1 to QB80</td></tr>
<tr><td>VC</td><td>QC1 to QC80</td></tr>
<tr><td rowspan="3">H</td><td>VA</td><td>QB1 to QB80</td></tr>
<tr><td>VB</td><td>QC1 to QC80</td></tr>
<tr><td>VC</td><td>QA1 to QA80</td></tr>
</table></td></tr>
</table>

■ Pin Descriptions

Pin No.	Symbol	Pin Name	I/O	Function Description
93 to 97	VBS	Bias adjustment	I	The voltage applied to this pin adjusts the output buffer bias and thus the drive capacity of the LCD drive outputs.
87 to 91 81 to 85 75 to 79	VA VB VC	Analog signal input	I	These pins accept the analog signal inputs for routing to the LCD drive outputs.
147, 149 151 to 385 387, 389 391	QA1 to 80 QB1 to 80 QC1 to 80	LCD drive output	O	These pins yield the levels obtained by applying the sample-and-hold circuits to the analog inputs (VA, VB, and VC).
52	MOD	Mode selection signal input	I	Connect this pin to V_{SS1} for sequential sampling mode.
62	TEST1	Test input	I	Connect this pin to V_{DD1}.
61	TEST2	Test input	I	Connect this pin to V_{DD1}.
63 to 68	V_{DD1}	Power supply for digital circuits	—	These pins supply the driving potential for the logic and other digital circuits.
9 to 18 105 to 114	V_{DD2}	Power supply for analog circuits	—	These pins supply the driving potential for the sample-and-hold and other analog circuits.
53 to 58	V_{SS1}	Ground for digital circuits	—	These pins supply the ground potential for the logic and other digital circuits.
127 to 142 396 to 409	V_{SS2}	Ground for analog circuits	—	These pins supply the ground potential for the sample-and-hold and other analog circuits.