

Clock signal generator circuit for digital TV systems (CGC)

SAA9057A

Supersedes data of April 1991

FEATURES

- Clock generation suitable for digital TV systems (line-locked)
- PLL frequency multiplier to generate 4 times of input frequency
- Dividers to generate clocks LL1.5, LL2, LL2A, LL3 and LL3T (4th, 3rd and 2nd multiples of input frequency)
- Skew control for clock outputs
- Reset control and power fail detection

SAA9051A not for new designs, for new applications use SAA9057B or SAA7157

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DDA}	analog supply voltage (pin 5)	5.0	5.2	5.5	V
V _{DDD}	digital supply voltage (pins 8, 17)	4.5	5.0	5.5	V
I _{DDA}	analog supply current	6	-	18	mA
I _{DDD}	digital supply current	10	-	60	mA
V _{LFCO}	LFCO input voltage (peak-to-peak value)	1	-	V _{DDA}	V
f _i	input frequency range	6.25	-	7.25	MHz
V _I	input voltage LOW input voltage HIGH	0 2.4	- -	0.8 V _{DDD}	V V
V _O	output voltage LOW output voltage HIGH	0 2.6	- -	0.6 V _{DDD}	V V
T _{amb}	operating ambient temperature range	0	-	70	°C

GENERAL DESCRIPTION

The SAA9057A generates all clock signals required for a digital TV system suitable for the SAA90xx family. Optional extras (feature box etc.) can be driven via external buffers, advantageous for a digital TV system based on display standard conversion concepts.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA9057A	20	DIL	plastic	SOT146
SAA9057AT	20	mini-pack (SO20)	plastic	SOT163A

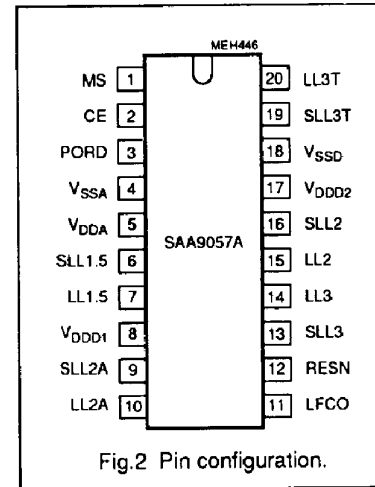
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PINNING

SYMBOL	PIN	DESCRIPTION
MS	1	mode select input (LOW = PLL mode)
CE	2	chip enable /reset (HIGH = outputs enabled)
PORD	3	power-on reset delay, dependent on external capacitor
V _{SSA}	4	analog ground (0 V)
V _{DDA}	5	analog supply voltage (+5 V)
SLL1.5	6	sensor input for output LL1.5
LL1.5	7	line-locked clock output signal (4 times f_{LFCO})
V _{DDD1}	8	digital supply voltage 1 (+5 V)
SLL2A	9	sensor input for output LL2A
LL2A	10	line-locked clock output signal for ADC (3 times f_{LFCO})
LFCO	11	line-locked input frequency
RESN	12	reset output (active-LOW)
SLL3	13	sensor input for output LL3
LL3	14	line-locked clock output signal (2 times f_{LFCO})
LL2	15	line-locked clock output signal (3 times f_{LFCO})
SLL2	16	sensor input for output LL2
V _{DDD2}	17	digital supply voltage 2 (+5 V)
V _{SSD}	18	digital ground (0 V)
SLL3T	19	sensor input for output LL3T
LL3T	20	line-locked clock output signal (2 times f_{LFCO})

PIN CONFIGURATION



LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V _{DDA}	analog supply voltage (pin 5)	-0.5	7.0	V
V _{DDD}	digital supply voltage (pins 8 and 17)	-0.5	7.0	V
V _{diff GND}	difference voltage V _{DDA} - V _{DDD}	-	±100	mV
V _O	output voltage (I _{OM} = 20 mA)	-0.5	V _{DDD}	V
P _{tot}	total power dissipation	0	1.1	W
T _{stg}	storage temperature range	-65	150	°C
T _{amb}	operating ambient temperature range	0	70	°C
V _{ESD}	electrostatic handling* for all pins	-	tbF	V

* Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is recommended to take normal handling precautions appropriate to "Handling MOS devices".

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CHARACTERISTICS
 $V_{DDA} = 5.0$ to 5.5 V; $V_{DDD} = 4.5$ to 5.5 V; $f_{LFCO} = 6.25$ to 7.25 MHz and $T_{amb} = 0$ to 70 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage (pin 5)		5.0	5.2	5.5	V
V_{DDD}	digital supply voltage (pins 8 and 17)		4.5	5.0	5.5	V
i_{DDA}	analog supply current (pin 5)		6	-	18	mA
I_{DDD}	digital supply current ($I_g + I_{17}$)	note 1	10	-	60	mA
V_{reset}	power-on reset threshold voltage	Fig.4	-	3.5	-	V
Input LFCO (pin 11)						
V_{11}	DC input voltage		0	-	V_{DDA}	V
V_i	input signal (peak-to-peak value)		1	-	V_{DDA}	V
f_{LFCO}	input frequency range		6.25	-	7.25	MHz
C_{11}	input capacitance		-	-	10	pF
Inputs MS, CE, SLLx (pins 1, 2, 6, 9, 13,16 and 19) note 3						
V_{IL}	input voltage LOW		0	-	0.8	V
V_{IH}	input voltage HIGH		2.4	-	V_{DDD}	V
I_{LI}	input leakage current		-	-	10	μ A
C_i	input capacitance		-	-	5	pF
Output RESN (pin 12)						
V_{OH}	output voltage LOW	$I_{OL} = 2$ mA	0	-	0.4	V
V_{OL}	output voltage HIGH	$I_{OH} = -0.5$ mA	2.4	-	V_{DDD}	V
I_{LI}	output leakage current		-	-	± 10	μ A
t_d	RESN delay time	$C_3 = 0.1\mu$ F; Fig.4	20	-	200	ms
Output signals LL1.5, LL2, LL2A, LL3, LL3T (pins 7, 10, 14, 15 and 20)						
V_{OL}	output voltage LOW	$I_{OL} = 2$ mA	0	-	0.6	V
V_{OH}	output voltage HIGH	$I_{OH} = -0.5$ mA	2.6	-	V_{DDD}	V
I_{LI}	output leakage current	high-impedance	-	-	± 10	μ A
t_{comp}	composite rise time	note 1; note 2	-	-	9	ns
f_{LL}	output frequency LL1.5	Fig.3	-	$4 f_{LFCO}$	-	MHz
	output frequency LL2		-	$3 f_{LFCO}$	-	MHz
	output frequency LL2A		-	$3 f_{LFCO}$	-	MHz
	output frequency LL3		-	$2 f_{LFCO}$	-	MHz
	output frequency LL3T		-	$2 f_{LFCO}$	-	MHz
f_{LL}	duty factor LL1.5 and LL2	note 1; Fig.3	40	50	60	%
	duty factor LL2A, LL3 and LL3T	note 1; Fig.3	43	50	57	%
t_r, t_f	rise and fall times	note 1; Fig.3	-	-	6	ns

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Notes to the characteristics

1. $f_{LFCO} = 7.0$ MHz and output load 40 pF. V_{SSA} and V_{SSD} short connected together.
2. t_{comp} is the rise time from LOW of all clocks to HIGH of all clocks (Fig.3) including rise time, skew and jitter components. Measurements taken between 0.6 V and 2.6 V.
3. MS function is not tested.

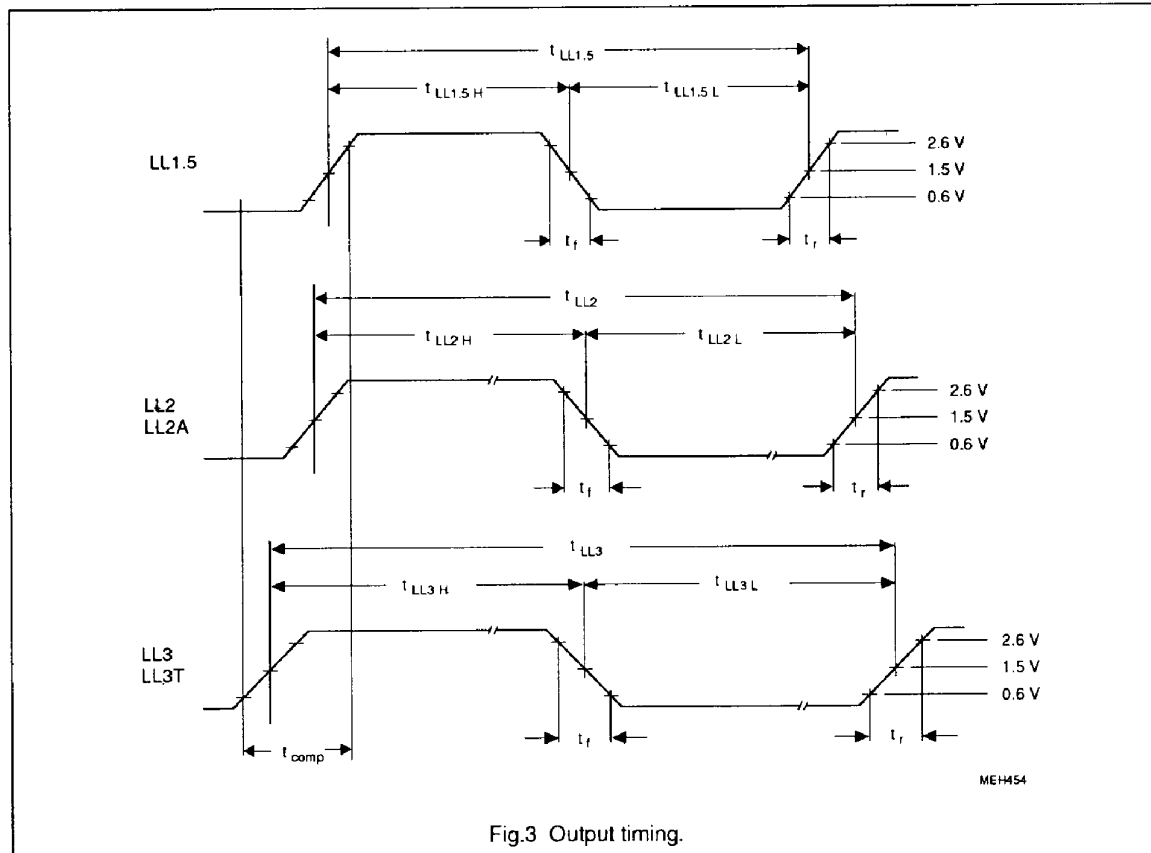


Fig.3 Output timing.

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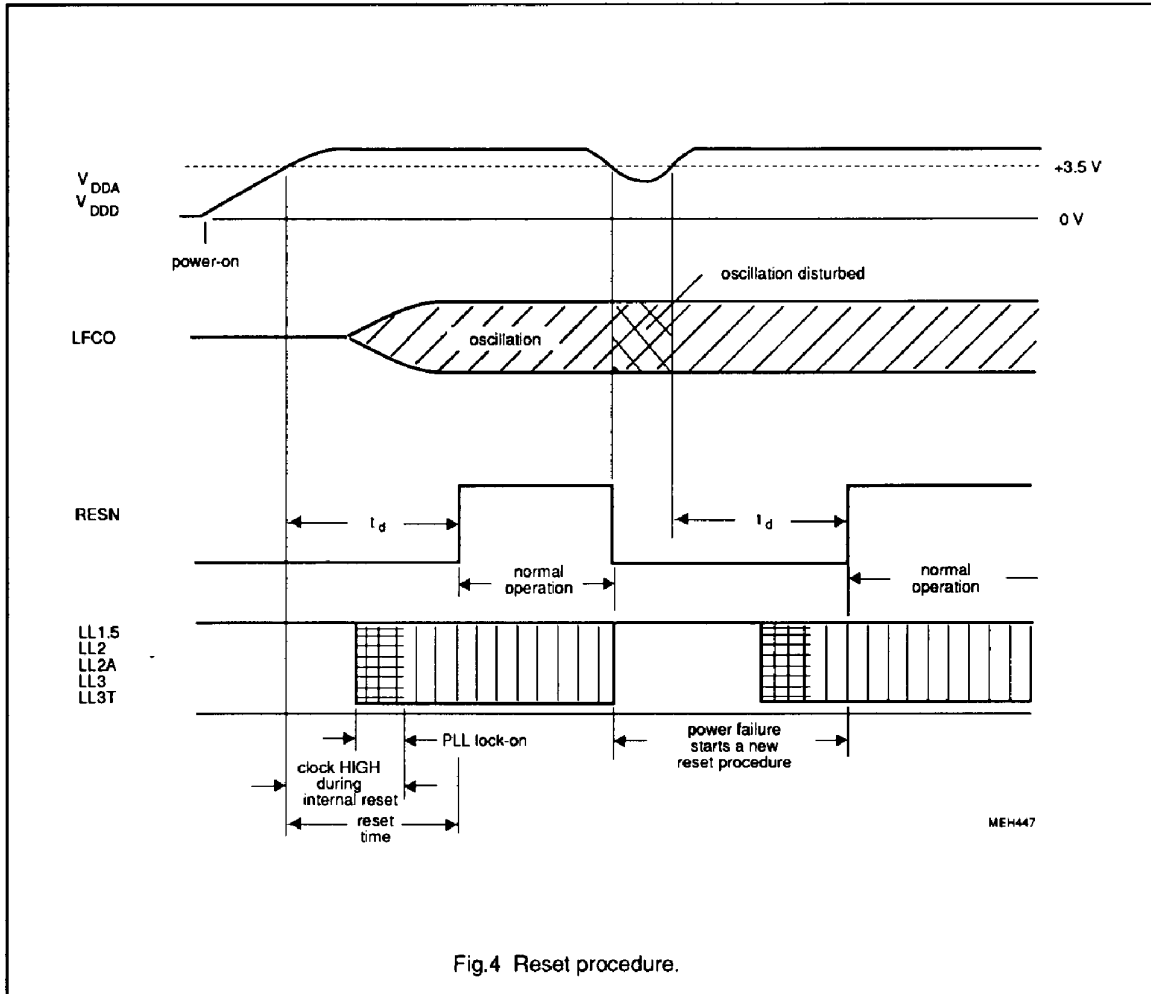


Fig.4 Reset procedure.

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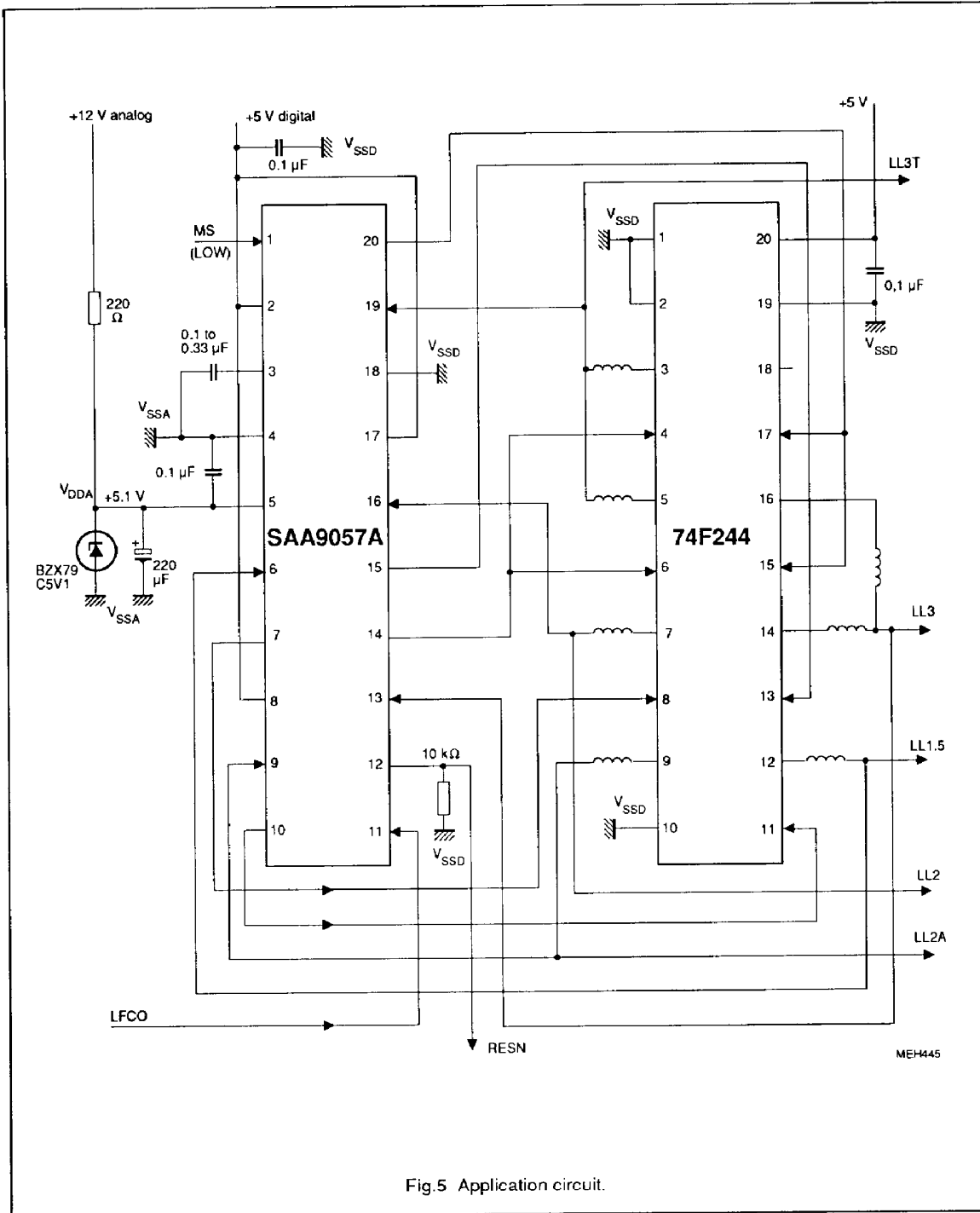


Fig.5 Application circuit.