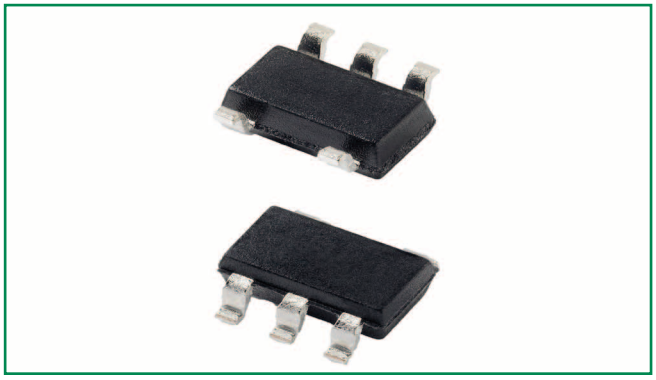
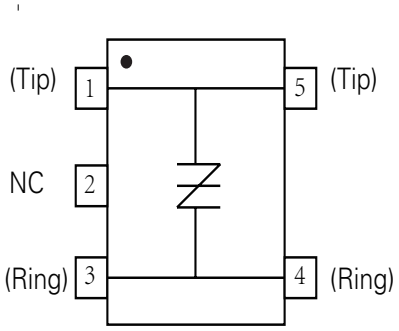
HF RoHS SDP Series - SOT23-5



Agency Approvals

Agency	Agency File Number
UL	E133083

Schematic Symbol



Description

This new SIDACtor series is targeted for the tertiary or line driver side protection position for VDSL2+, ADSL2 applications and general I/O protection functions. This new low capacitance over voltage protection does not require a bias voltage and is sufficiently robust for the chip-side position behind the coupling transformer.

This SOT23-5 solution, with its flow-through design, minimizes PCB trace layout routing, while its four different stand-off voltage values offer compatibility with a variety of line drivers. Its low capacitance makes it compatible with ADSL2 and VDSL2, and the 30MHz bandplan of VDSL2+.

Features & Benefits

- Lower overshooting protection than clamping
- SOT23-5 surface mount package
- Low insertion loss
- Low capacitance
- Bidirectional transient voltage protection
- Robust surge rating
- Starts to switch in nanoseconds
- RoHS compliant

Applicable Global Standards

- YD/T 950
- YD/T 993
- YD/T 1082
- GR 1089 Inter-building
- GR 1089 Intra-building
- IEC 61000-4-2
- IEC 61000-4-5
- ITU K.20/21 Basic Level
- ITU K.20/21 Enhanced Level
- TIA-968-A
- TIA-968-B

Surge Ratings

Series	I_{PP} 8/20µs Amps min
G	50

Electrical Characteristics

Part Number	Marking	V_{DRM}@I_{DRM}=5µA	V_S@250V/µs	I_H	I_S	V_T@I_T=1.0 Amps	Co@f=1MHz,2V
		V min	V max	mA typ	mA max	V max	pF typ
SDP0080T023G5RP	P08G	8	15	30	500	4.0	6.5
SDP0120T023G5RP	P12G	12	20	30	500	4.0	6.0
SDP0180T023G5RP	P18G	18	25	30	500	4.0	5.5
SDP0240T023G5RP	P24G	24	35	30	500	4.0	5.0

Notes:
- All measurement are made at an ambient temperature of 25°C.
- Ipp applies to -40°C through +85°C temperature range.
- Ipp is repetitive surge rating and is guaranteed for the life of the product.
- SIDACtor devices are bidirectional. All electrical parameters and surge rating apply to forward and reverse polarities.

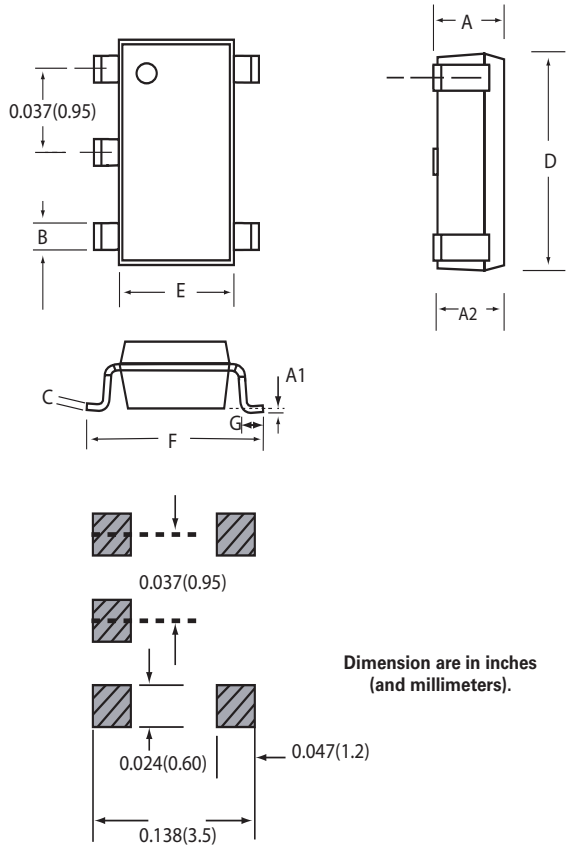
Maximum Ratings

Parameter Name	Symbol	Test Conditions	Value		Units
Lightning surge waveforms	I_{pp}	8/20µs	50		A
			min	max	
Operating Free Temperature Range	T_A		-40	+85	°C
Junction temperature	T_J		-40	+150	°C
Storage temperature	T_{STG}		-40	+150	°C

Notes:
- The device also complies with IEC 61000-4-2 ESD ±15kV (air discharge), ±8 kV(contact discharge) and IEC 61000-4-4 EFT 40A(5/50nS) in equipment level ESD test when used behind the xDSL transformer.
- The device must initially be in thermal equilibrium with -40°C ≤ T_J ≤ +150°C
- The lightning surge may be repeated after the device returns to its initial conditions.

Mechanical dimensions, recommended layout dimensions

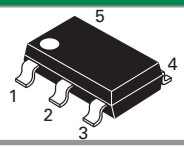
The epoxy meets UL 94V-0 ratings.



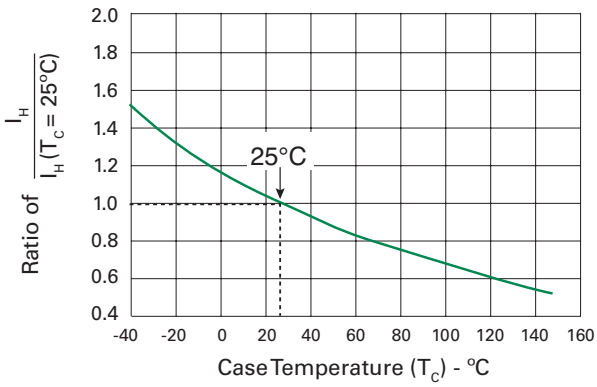
Dimension are in inches (and millimeters).

Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A	0.035	0.057	0.90	1.45
A1	0	0.004	0	0.10
A2	0.035	0.051	0.90	1.30
B	0.014	0.020	0.35	0.50
C	0.004	0.008	0.09	0.20
D	0.11	0.118	2.80	3.00
E	0.059	0.069	1.50	1.75
F	0.102	0.118	2.6	3.00
G	0.004	0.024	0.10	0.60

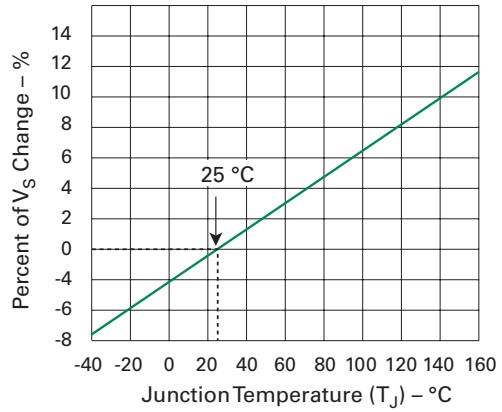
Thermal Considerations

Package	Symbol	Parameter	Value	Unit
	T_J	Operating Junction Temperature Range	-40 to +150	°C
	T_{STG}	Storage Temperature Range	-40 to +150	°C
	$R_{\theta JA}$	Thermal Resistance: Junction to Ambient	120	°C/W

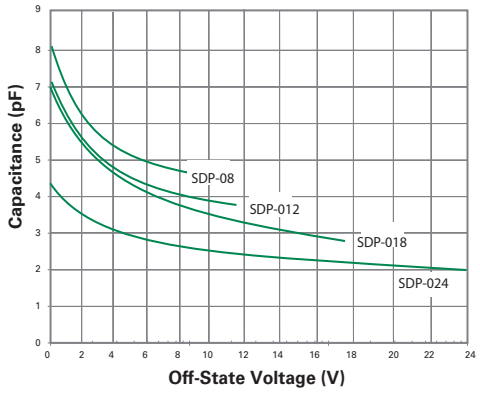
Holding Current vs. Case Temperature



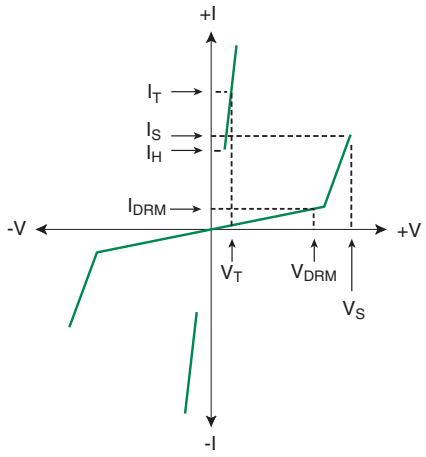
V_S vs. Junction Temperature



Capacitance vs. Bias Voltage

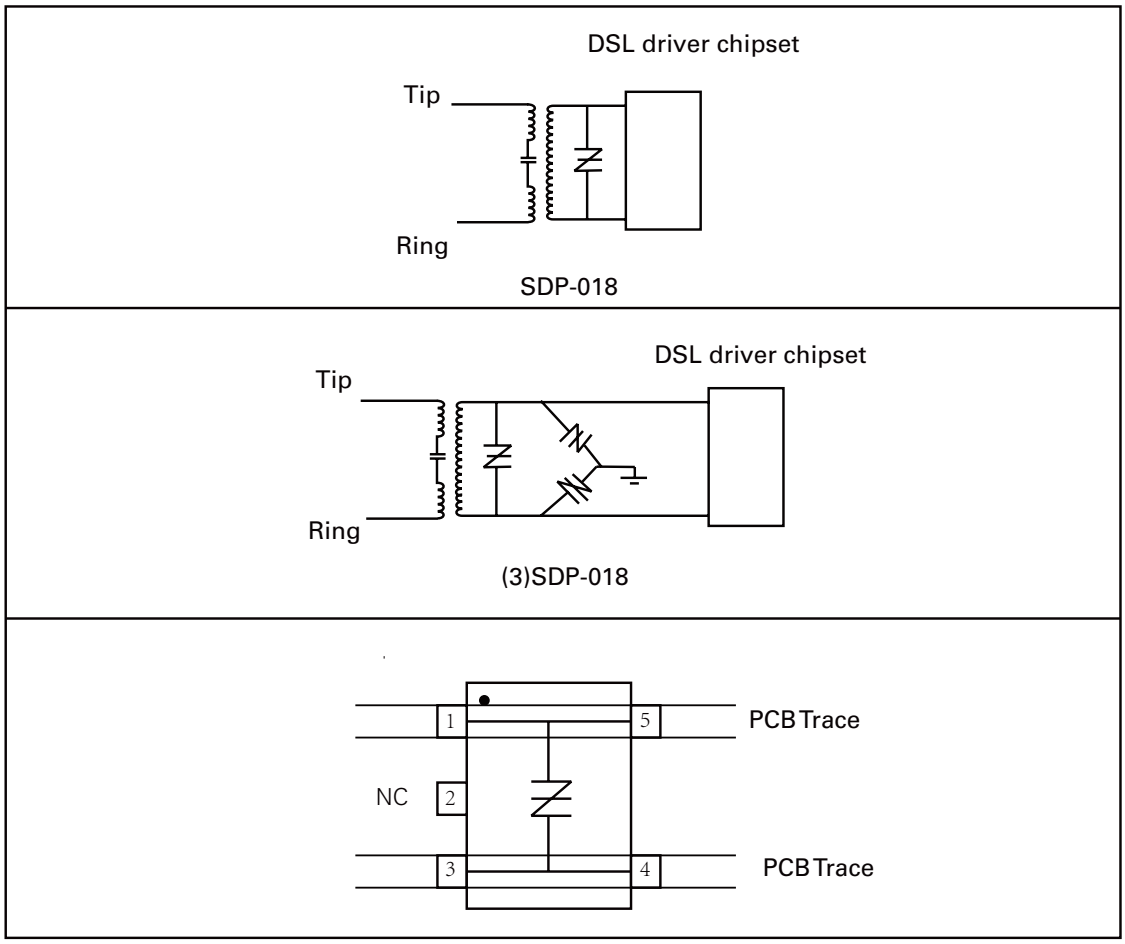


V-I Characteristics



SDP-xxx Application example

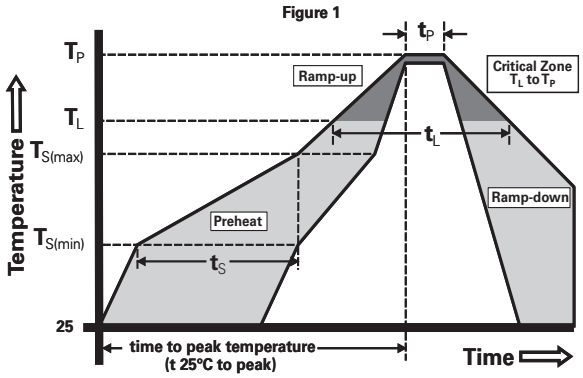
The following schematics show alternate protection solutions for a typical DSL interface that connects to outside wiring. This surface mount SOT23-5 chip-side solution provides a minimum footprint solution appropriate for high density card designs. The SDP-xxx0T023 will protect the interface from lightning induced surges on the chip-side of the coupling transformer. This tertiary protector may be preceded by line-side protection such as the TeleLink over-current protector and the SDP3500Q38CB overvoltage protector. GDTs may also be used on the line side of the coupling transformer. The flow-through design of the SOT23-5 package is illustrated below. If the inter winding capacitance of the transformer is allowing some common mode events to get coupled across, then the SDP-xxx0T023 can be placed in a three chip mode, as shown below for additional chip-side protection.



Soldering Parameters

Reflow Condition		Pb-Free assembly (see Fig. 1)
Pre Heat	-Temperature Min ($T_{s(min)}$)	+150°C
	-Temperature Max ($T_{s(max)}$)	+200°C
	-Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	-Temperature (T_L) (Liquidus)	+217°C
	-Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (t_p)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C

Figure 1



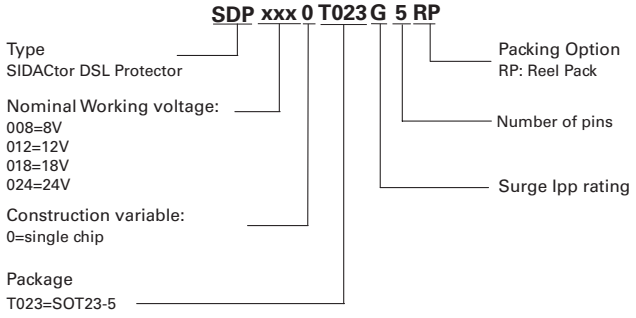
Physical Specifications

Terminal Material	100% Matte-Tin Plated
Solderability	EIA J-STD-002, TEST A.

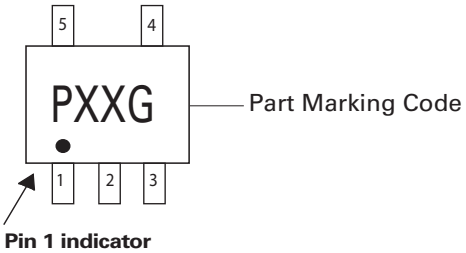
Environmental Specifications

Temp Cycling	Mil-STD-883F, Method 1010.8 Condition C, -65°C to +150°C 168 Hrs, 85°C /60%RH+3IR-Reflow, 260°C +5V, -0°C
Bias Humidity	JESD 22-A101-B 85°C , 85°CRH. 50V 168 Hrs, 85°C /60%RH+3IR-Reflow, 260°C +5V, -0°C
Pressure Cooker	JEDEC 22-A102C No Bias, 121°C, 100%RH 96Hrs/192Hrs. 168 Hrs, 85°C /60%RH+3IR-Reflow, 260°C +5V, -0°C
High Temp Storage	JESD 22-A103C Con B. 150°C, no bias 1000Hrs
HTRB	JESD 22-108C 168 Hrs, 85°C /60%RH+3IR-Reflow, 260°C +5V, -0°C
Thermal Shock	Mil-STD-883F, Method 1011.9 Condition A, 0°C to 100°C 168 Hrs, 85°C /60%RH+3IR-Reflow, 260°C +5V, -0°C
C-SAM	As per flow, JSTD-020C pre&post preconditioning test.
Wet Humidity (Tin only)	NEMI standard: 60°C/93%RH

Part Numbering



Part Marking



Packing Options

Package Type	Description	Quantity	Added Suffix	Min. Order Qty.	Industry Standard
T023	SOT23-5 Tape & Reel Pack	3000	RP	3000	EIA-481-A

Tape and Reel Specification — SOT23-5

8mm TAPE AND REEL