$N\,a\,t\,i\,o\,n\,a\,l$ $S\,e\,m\,i\,c\,o\,n\,d\,u\,c\,t\,o\,r$

January 1995

DAC0854 Quad 8-Bit Voltage-Output Serial D/A Converter with Readback

General Description

The DAC0854 is a complete quad 8-bit voltage-output digital-to-analog converter that can operate on a single 5V supply. It includes on-chip output amplifiers, internal voltage reference, and a serial microprocessor interface. By combining in one package the reference, amplifiers, and conversion circuitry for four D/A converters, the DAC0854 minimizes wiring and parts count and is hence ideally suited for applications where cost and board space are of prime concern.

The DAC0854 also has a data readback function, which can be used by the microprocessor to verify that the desired input word has been properly latched into the DAC0854's data registers. The data readback function simplifies the design and reduces the cost of systems which need to verify data integrity.

The logic comprises a MICROWIRE™-compatible serial interface and control circuitry. The interface allows the user to write to any one of the input registers or to all four at once. The latching registers are double-buffered, consisting of 4 separate input registers and 4 DAC registers. Double buffering allows all 4 DAC outputs to be updated simultaneously.

The four reference inputs allow the user to configure the system to have a separate output voltage range for each DAC. The output voltage of each DAC can range between 0.3V and 2.8V and is a function of V_{BIAS}, V_{REF}, and the input word.

Features

- Single +5V supply operation
- MICROWIRE serial interface allows easy interface to many popular microcontrollers including the COPS™ and HPC™ families of microcontrollers
- Data readback capability
- Output data can be formatted to read back MSB or LSB first
- Versatile logic allows selective or global update of the DACs
- Power fail flag
- Output amplifiers can drive 2 kΩ load
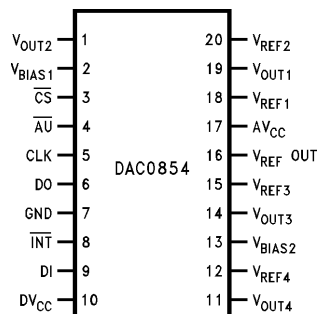- Synchronous/asynchronous update of the DAC outputs

Key Specifications

- Guaranteed monotonic over temperature
- Integral linearity error $\pm\frac{1}{2}$ LSB max
- Output settling time 2.7 μs max
- Analog output voltage range 0.3V to 2.8V
- Supply voltage range 4.5V to 5.5V
- Clock frequency 10 MHz max
- Power dissipation (f_{CLK} = 10 MHz) 95 mW max
- On-board reference 2.65V $\pm$2% max

Applications

- Automatic test equipment
- Industrial process controls
- Automotive controls and diagnostics
- Instrumentation

Connection Diagram

Pin	Signal		Pin	Signal
1	V_{OUT2}		20	V_{REF2}
2	V_{BIAS1}		19	V_{OUT1}
3	$\overline{CS}$		18	V_{REF1}
4	$\overline{AU}$		17	AV_{CC}
5	CLK		16	V_{REF} OUT
6	DO		15	V_{REF3}
7	GND		14	V_{OUT3}
8	$\overline{INT}$		13	V_{BIAS2}
9	DI		12	V_{REF4}
10	DV_{CC}		11	V_{OUT4}

DAC0854

TL/H/11261–1

Top View

Ordering Information

Industrial ($-40°C < T_A$ +85°C)	Package
DAC0854BIN, DAC0854CIN	N20A Molded DIP
DAC0854CIJ	J20A Ceramic DIP
DAC0854BIWM, DAC0854CIWM	M20B Small Outline
Military ($-55°C < T_A < +125°C$)	
DAC0854CMJ/883	J20A Ceramic DIP

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RRD-B30M75/Printed in U. S. A.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 24)

Supply Voltage (AV_{CC}, DV_{CC})	7V
Supply Voltage Difference (AV_{CC}–DV_{CC})	$\pm 5.5V$
Voltage at Any Pin (Note 3)	GND $-0.3V$ to AV_{CC}/DV_{CC} $+0.3V$
Input Current at Any Pin (Note 3)	5 mA
Package Input Current (Note 4)	20 mA
Power Dissipation (Note 5)	105 mW
ESD Susceptibility (Note 6)	1250V

Soldering Information

J Package (10 sec.)	300°C
N Package (10 sec.)	260°C
SO Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.) (Note 7)	220°C
Storage Temperature	$-65°C$ to $+150°C$

Operating Ratings (Notes 1 & 2)

Supply Voltage	4.5V to 5.5V
Supply Voltage Difference ($AV_{CC} - DV_{CC}$)	$\pm IV$
Temperature Range	$T_{MIN} < T_A < T_{MAX}$
DAC0854BIN, DAC0854CIN, DAC0854CIJ, DAC0854BIWM, DAC0854CIWM	$-40°C < T_A < 85°C$
DAC0854CMJ/883	$-55°C < T_A < 125°C$

Converter Electrical Characteristics

The following specifications apply for $AV_{CC} = DV_{CC} = 5V$, $V_{REF} = 2.65V$, $V_{BIAS} = 1.4V$, $R_L = 2$ kΩ (R_L is the load resistor on the analog outputs – pins 1, 11, 14, and 19) and $f_{CLK} = 10$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J$ from T_{MIN} to T_{MAX}.** All other limits apply for $T_A = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 8)	Limit (Note 9)	Units (Limits)
STATIC CHARACTERISTICS					
n	Resolution	$f_{CLK} = 10$ MHz	8	**8**	bits
	Monotonicity	(Note 10)	8	**8**	bits
	Integral Linearity Error	(Note 11)			
	DAC0854BIN, DAC0854BIWM			**± 0.5**	LSB (max)
	DAC0854CIN, DAC0854CIJ, DAC0854CIWM, DAC0854CMJ			**± 1.0**	LSB (max)
	Differential Linearity Error			**± 1.0**	LSB (max)
	Fullscale Error	(Note 12)		**± 35**	mV
	Fullscale Error Tempco	(Note 13)	-30		ppm/°C
	Zero Error	(Note 14)		**± 35**	mV
	Zero Error Tempco	(Note 13)	-30		ppm/°C
	Power Supply Sensitivity	(Note 15)	-42	**-34**	dB (max)
DYNAMIC CHARACTERISTICS					
t_{s+}	Positive Voltage Output Settling Time	(Note 16) $C_L = 200$ pF	1.5	**2.1**	μs
t_{s-}	Negative Voltage Output Settling Time	(Note 16) $C_L = 200$ pF	1.8	**2.7**	μs
	Digital Crosstalk	(Note 17)	1.8		$mV_{p\text{-}p}$
	Digital Feedthrough	(Note 18)	8.5		$mV_{p\text{-}p}$
	Clock Feedthrough	(Note 19)	3.3		$mV_{p\text{-}p}$
	Channel-to-Channel Isolation	(Note 20)	-78		dB
	Glitch Energy	(Note 21)	7		$nV-s$
	Peak Value of Largest Glitch		38		mV
PSRR	Power Supply Rejection Ratio	(Note 22)	-49		dB

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Converter Electrical Characteristics (Continued)

The following specifications apply for $AV_{CC} = DV_{CC} = 5V$, $V_{REF} = 2.65V$, $V_{BIAS} = 1.4V$, $R_L = 2\ k\Omega$ (R_L is the load resistor on the analog outputs – pins 1, 11, 14, and 19) and $f_{CLK} = 10$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J$ from T_{MIN} to T_{MAX}.** All other limits apply for $T_A = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 3)	Limit (Note 4)	Units (Limits)
DIGITAL AND DC ELECTRICAL CHARACTERISTICS					
$V_{IN(1)}$	Logical "1" Input Voltage	$AV_{CC} = DV_{CC} = 5.5V$		**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage	$AV_{CC} = DV_{CC} = 4.5V$		**0.8**	V (max)
I_{IL}	Digital Input Leakage Current		1	**5**	μA (max)
C_{IN}	Input Capacitance		4		pF
C_{OUT}	Output Capacitance		5		pF
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_{SOURCE} = 0.8$ mA		**2.4**	V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_{SINK} = 3.2$ mA		**0.4**	V (max)
V_{INT}	Interrupt Pin Output Voltage	10 kΩ Pullup		**0.4**	V (max)
I_S	Supply Current	Outputs Unloaded	14	**19**	mA
REFERENCE INPUT CHARACTERISTICS					
V_{REF}	Input Voltage Range		0–2.75		V
R_{REF}	Input Resistance		7	**4** **10**	kΩ (min) kΩ (max)
C_{REF}	Input Capacitance	Full-Scale Data Input	40		pF
V_{BIAS} INPUT CHARACTERISTICS					
V_{BIAS}	V_{BIAS} Input Voltage Range		0.3–1.4		V
	Input Leakage		1		μA
C_{BIAS}	Input Capacitance		9		pF
BANDGAP REFERENCE CHARACTERISTICS ($C_L = 220\mu F$)					
$V_{REF}OUT$	Output Voltage			**2.65 ± 2%**	V
$\Delta V_{REF}/\Delta T$	Tempco	(Note 23)	22		ppm/°C
	Line Regulation	$4.5V < V_{CC} < 5.5V$, $I_L = 4$ mA	2	**5**	mV
$\Delta V_{REF}/\Delta I_L$	Load Regulation	$0 < I_L < 4$ mA $0 < I_L < 4$ mA; CMJ Suffix $-1 < I_L < 0$ mA	2 2 2.5	**6** **15**	mV mV mV
I_{SC}	Short Circuit Current	$V_{REF}OUT = 0V$	12		mA
AC ELECTRICAL CHARACTERISTICS					
t_{DS}	Data Setup Time			**10**	ns (min)
t_{DH}	Data Hold Time			**0**	ns (min)
t_{CS}	Control Setup Time			**15**	ns (min)
t_{CH}	Control Hold Time			**0**	ns (min)
t_{MIN}	Clock Frequency			**10**	MHz (max)
t_H	Minimum Clock High Time			**20**	ns (min)
t_L	Minimum Clock Low Time			**40**	ns (min)

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Converter Electrical Characteristics (Continued)

The following specifications apply for $AV_{CC} = DV_{CC} = 5V$, $V_{REF} = 2.65V$, $V_{BIAS} = 1.4V$, $R_L = 2\ k\Omega$ (R_L is the load resistor on the analog outputs – pins 1, 11, 14, and 19) and $f_{CLK} = 10$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J$ from T_{MIN} to T_{MAX}.** All other limits apply for $T_A = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 3)	Limit (Note 4)	Units (Limits)
AC ELECTRICAL CHARACTERISTICS (Continued)					
t_{CZ1}	Output Hi-Z to Valid 1			**37**	ns (max)
t_{CZ0}	Output Hi-Z to Valid 0			**42**	ns (max)
t_{1H}	$\overline{CS}$ to Output Hi-Z	10 kΩ with 60 pF		**130**	ns (max)
t_{0H}	$\overline{CS}$ to Output Hi-Z	10 kΩ with 60 pF		**117**	ns (max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional. These ratings do not guarantee specific performance limits, however. For guaranteed specifications and test conditions, see the Converter Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to ground, unless otherwise specified.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} <$ GND or $V_{IN} > V+$) the absolute value of current at that pin should be limited to 5 mA or less.

Note 4: The sum of the currents at all pins that are driven beyond the power supply voltages should not exceed 20 mA.

Note 5: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), Θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\Theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. The table below details T_{Jmax} and Θ_{JA} for the various packages and versions of the DAC0854.

Part Number	T_{Jmax} (°C)	Θ_{JA} (°C/W)
DAC0854BIN, DAC0854CIN	125	46
DAC0854BIJ, DAC0854CIJ	125	53
DAC0854BIWM, DAC0854CIWM	125	64
DAC0854CMJ/883	150	53

Note 6: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 7: See AN450 ''Surface Mounting Methods and Their Effect on Production Reliability'' of the section titled ''Surface Mount'' found in any current Linear Databook for other methods of soldering surface mount devices.

Note 8: Typicals are at $T_J = 25°C$ and represent most likely parametric norm.

Note 9: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 10: A monotonicity of 8 bits for the DAC0854 means that the output voltage changes in the same direction (or remains constant) for each increase in the input code.

Note 11: Integral linearity error is the maximum deviation of the output from the line drawn between zero and full-scale (excluding the effects of zero error and full-scale error).

Note 12: Full-scale error is measured as the deviation from the ideal 2.800V full-scale output when $V_{REF} = 2.650V$ and $V_{BIAS} = 1.400V$.

Note 13: Full-scale error tempco and zero error tempco are defined by the following equation:

$$\text{Error tempco} = \left[\frac{\text{Error }(T_{MAX}) - \text{Error }(T_{MIN})}{V_{SPAN}}\right]\left[\frac{10^6}{T_{MAX} - T_{MIN}}\right]$$

where Error (T_{MAX}) is the zero error or full-scale error at T_{MAX} (in volts), and Error (T_{MIN}) is the zero error or full-scale error at T_{MIN} (in volts); V_{SPAN} is the output voltage span of the DAC0854, which depends on V_{BIAS} and V_{REF}.

Note 14: Zero error is measured as the deviation from the ideal 0.310V output when $V_{REF} = 2.650V$, $V_{BIAS} = 1.400V$, and the digital input word is all zeros.

Note 15: Power Supply Sensitivity is the maximum change in the offset error or the full-scale error when the power supply differs from its optimum 5V by up to 0.25V (5%). The load resistor $R_L = 5\ k\Omega$.

Note 16: Positive or negative settling time is defined as the time taken for the output of the DAC to settle to its final full-scale or zero output to within ± 0.5 LSB. This time shall be referenced to the 50% point of the positive edge of $\overline{CS}$, which initiates the update of the analog outputs.

Note 17: Digital crosstalk is the glitch measured on the output of one DAC while applying an all 0s to all 1s transition at the input of the other DACs.

Note 18: All DACs have full-scale outputs latched and DI is clocked with no update of the DAC outputs. The glitch is then measured on the DAC outputs.

Note 19: Clock feedthrough is measured for each DAC with its output at full-scale. The serial clock is then applied to the DAC at a frequency of 10 MHz and the glitch on each DAC full-scale output is measured.

Note 20: Channel-to-channel isolation is a measure of the effect of a change in one DAC's output on the output of another DAC. The V_{REF} of the first DAC is varied between 1.4V and 2.65V at a frequency of 15 kHz while the change in full-scale output of the second DAC is measured. The first DAC is loaded with all 0s.

Note 21: Glitch energy is the difference between the positive and negative glitch areas at the output of the DAC when a 1 LSB digital input code change is applied to the input. The glitch energy will have its largest value at one of the three major transitions. The peak value of the maximum glitch is separately specified.

Note 22: Power Supply Rejection Ratio is measured by varying $AV_{CC} = DV_{CC}$ between 4.75 and 5.25V with a frequency of 10 kHz and measuring the proportion of this signal imposed on a full-scale output of the DAC under consideration.
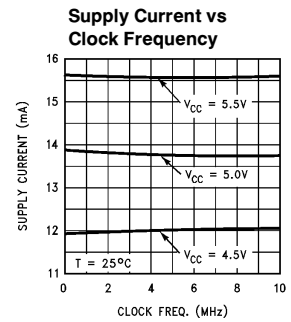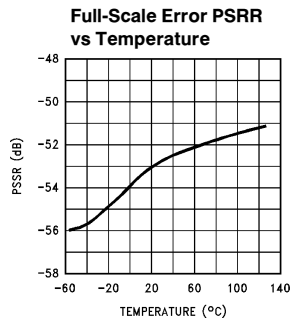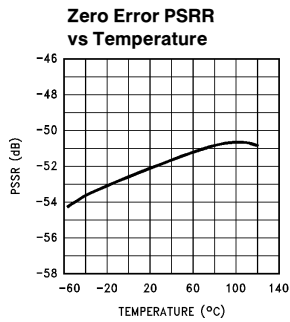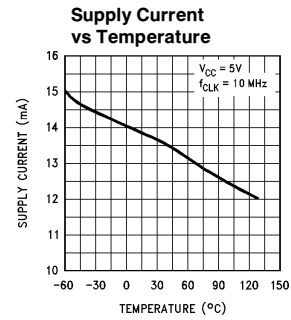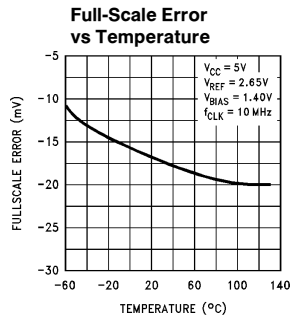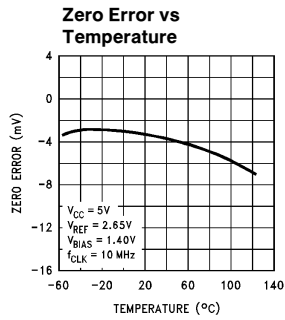
Note 23: The bandgap reference tempco is defined by the following equation:

$$\text{Tempco} = \left[\frac{V_{REF}(T_{MAX}) - V_{REF}(T_{MIN})}{V_{REF}(T_{ROOM})}\right]\left[\frac{10^6}{T_{MAX} - T_{MIN}}\right]$$

where $T_{ROOM} = 25°C$, $V_{REF}(T_{MAX})$ is the reference output at T_{MAX}, and similarly for $V_{REF}(T_{MIN})$ and $V_{REF}(T_{ROOM})$.
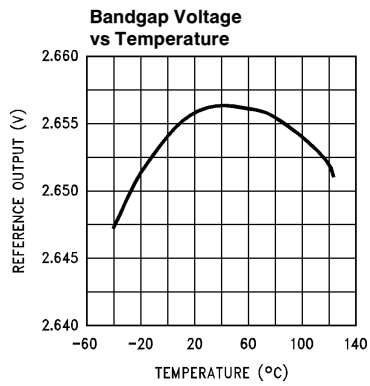
Note 24: A Military RETS specification is available upon request.

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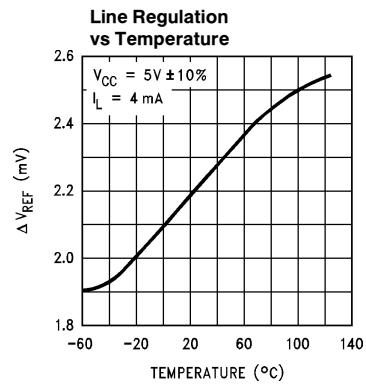# Typical Converter Performance Characteristics

Zero Error vs Temperature

(graph: ZERO ERROR (mV) vs TEMPERATURE (°C); $V_{CC} = 5V$, $V_{REF} = 2.65V$, $V_{BIAS} = 1.40V$, $f_{CLK} = 10$ MHz)

Full-Scale Error vs Temperature

(graph: FULLSCALE ERROR (mV) vs TEMPERATURE (°C); $V_{CC} = 5V$, $V_{REF} = 2.65V$, $V_{BIAS} = 1.40V$, $f_{CLK} = 10$ MHz)

Supply Current vs Temperature

(graph: SUPPLY CURRENT (mA) vs TEMPERATURE (°C); $V_{CC} = 5V$, $f_{CLK} = 10$ MHz)

Zero Error PSRR vs Temperature

(graph: PSSR (dB) vs TEMPERATURE (°C))

Full-Scale Error PSRR vs Temperature

(graph: PSSR (dB) vs TEMPERATURE (°C))

Supply Current vs Clock Frequency

(graph: SUPPLY CURRENT (mA) vs CLOCK FREQ. (MHz); $V_{CC} = 5.5V$, $V_{CC} = 5.0V$, $V_{CC} = 4.5V$, $T = 25°C$)

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Typical Reference Performance Characteristics

Bandgap Voltage vs Temperature

(graph: REFERENCE OUTPUT (V) vs TEMPERATURE (°C))

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Line Regulation vs Temperature

(graph: ΔV_{REF} (mV) vs TEMPERATURE (°C); $V_{CC} = 5V \pm 10\%$, $I_L = 4$ mA)

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TRI-STATE Test Circuits and Waveforms
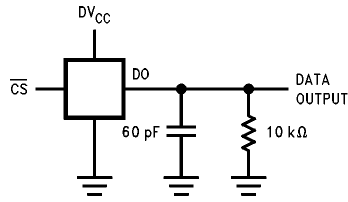
TL/H/11261–5
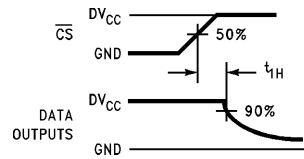
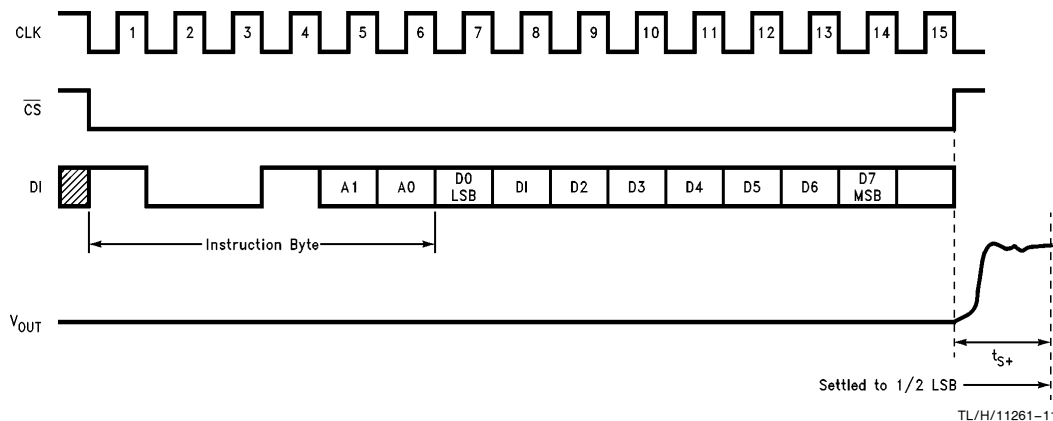TL/H/11261–6
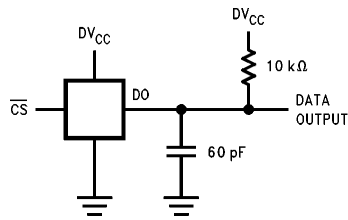
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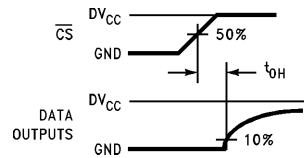
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Timing Waveforms

Data Input Timing

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Data Output Timing
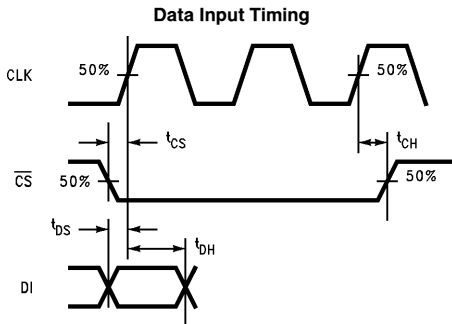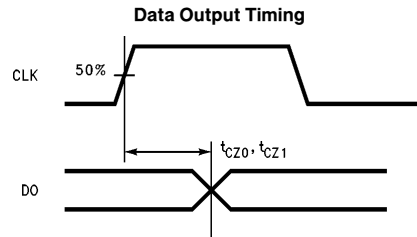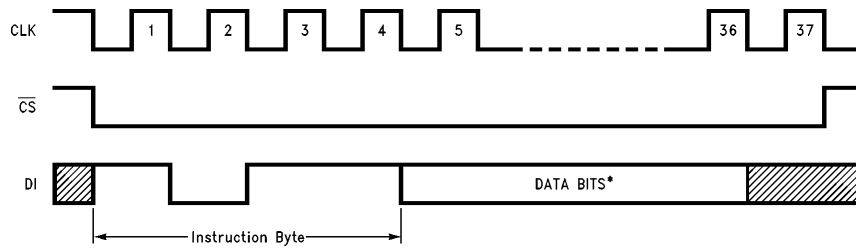

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Timing Diagrams

TL/H/11261–11

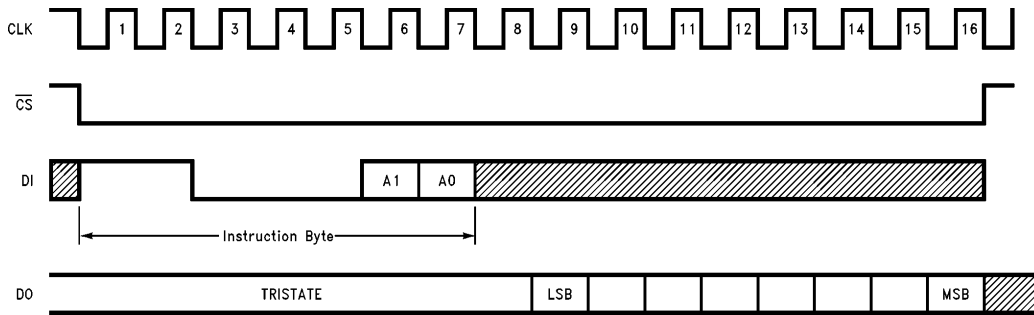**FIGURE 1. Write to One DAC with Update of Output ($\overline{AU} = 1$)**

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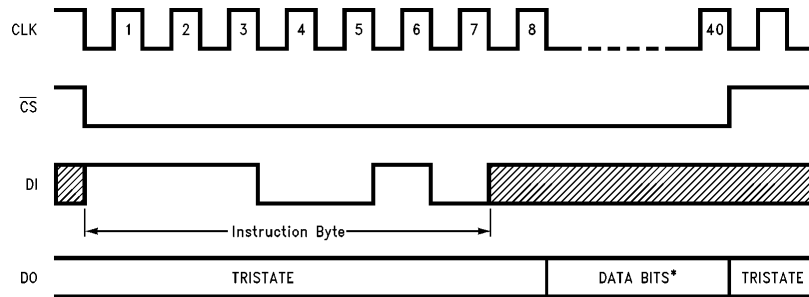## Timing Diagrams (Continued)

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* DACs are written to LSB first.

DAC1 is written to first, then DACs 2, 3, and 4.

FIGURE 2. Write to All DACs with Update of Outputs ($\overline{AU} = 1$)

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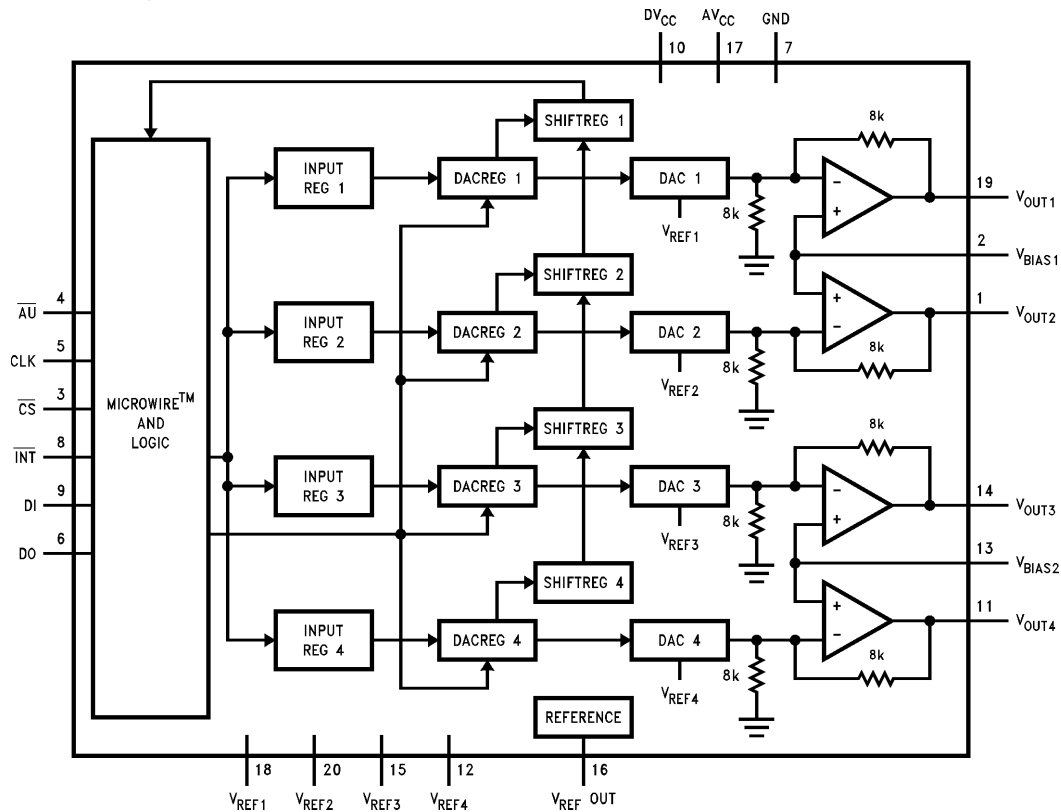**FIGURE 3. Read One DAC, DO Changes on Falling Edge, DO LSB First ($\overline{AU} = 1$)**

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*DAC1 is read first, then DACs 2, 3, and 4.

FIGURE 4. Read All DACs, DO LSB First, DO Changes on Falling Edge ($\overline{AU} = 1$)

Block Diagram

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Pin Description

$V_{OUT1}(19)$ The voltage output connections of the
$V_{OUT2}(1)$ four DACS. These provide output
$V_{OUT3}(14)$ voltages in the range 0.3V–2.8V.
$V_{OUT4}(11)$

$V_{REF}OUT(16)$ The internal voltage reference output.
The output of the reference is 2.65V
$\pm 2\%$. This pin should be bypassed with
a 220 μF capacitor.

$V_{BIAS1}(2)$ V_{BIAS1} is connected to the non-inverting
$V_{BIAS2}(13)$ inputs of output amplifiers 1 and 2,
thereby setting the virtual ground
voltage for DAC's 1 and 2, while V_{BIAS2}
performs this function for DAC's 3 and 4.
The allowed range is 0.3V – 1.4V.

GND(7) The system ground pin. Connect to
clean ground point.

$DV_{CC}(10)$ The digital and analog power supply
$AV_{CC}(17)$ pins. The power supply range of the
DAC0854 is 4.5V – 5.5V. To guarantee
accuracy, it is required that the AV_{CC}
and DV_{CC} pins be bypassed separately
with bypass capacitors of 10 μF
tantalum in parallel with 0.1 μF ceramic.

$\overline{AU}(4)$ When this pin is taken low, all DAC outputs
will be asynchronously updated. $\overline{CS}$ must be
held high during the update.

$V_{REF1}(18)$ The voltage reference inputs for the four
$V_{REF2}(20)$ DACs. The allowed range is 0V – 2.75V.
$V_{REF3}(15)$
$V_{REF4}(12)$

$\overline{CS}(3)$ The Chip Select control input. This input is
active low.

CLK(5) The external clock input pin.

DI(9) The serial data input. The data is clocked in
LSB first. Preceding the data byte are 4 or 6
bits of instructions.

DO(6) The serial data output. The data can be
clocked out either MSB or LSB first, and on
either the positive or negative edge of the
clock.

$\overline{INT}(8)$ The power interrupt output. On an
interruption of the power supply, this pin
goes low. Since this pin has an open drain
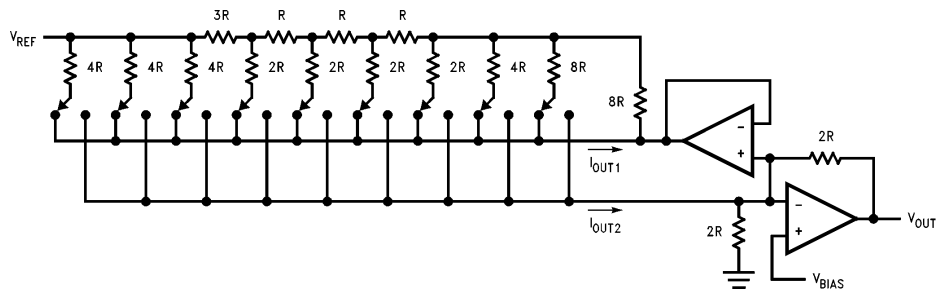output, a 10 kΩ pull-up resistor must be
connected to the supply.

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Applications Information

FUNCTIONAL DESCRIPTION

The DAC0854 is a monolithic quad 8-bit digital-to-analog converter that is designed to operate on a single 5V supply. Each of the four units is comprised of an input register, a DAC register, a shift register, a current output DAC, and an output amplifier. In addition, the DAC0854 has an onboard bandgap reference and a logic unit which controls the internal operation of the DAC0854 and interfaces it to microprocessors.
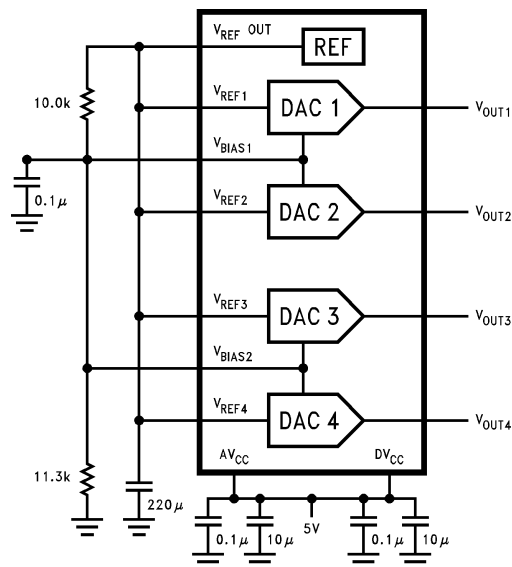
Each of the four internal 8-bit DACs uses a modified R-2R ladder to effect the digital-to-analog conversion *(Figure 5)*. The resistances corresponding to the 2 most significant bits are segmented to reduce glitch energy and to improve matching. The bottom of the ladder has been modified so that the voltage across the LSB resistor is much larger than the input offset voltage of the buffer amplifier. The input digital code determines the state of the switches in the ladder network. The sum of currents I_{OUT1} and I_{OUT2} is fixed and is given by

$$I_{OUT1} + I_{OUT2} = \left(\frac{V_{REF} - V_{BIAS}}{R} \right) \frac{255}{256}$$

The current output I_{OUT2} is applied to the internal output amplifier and converted to a voltage. The output voltage of each DAC is a function of V_{BIAS}, V_{REF}, and the digital input word, and is given by

$$V_{OUT} = 2 \, (V_{REF} - V_{BIAS}) \frac{DATA}{256} + \frac{511}{128} V_{BIAS} - \frac{255}{128} V_{REF}$$

The output voltage range for each DAC is 0.3V–2.8V. This range can be achieved by using the internal 2.65V reference and a voltage divider network which provides a V_{BIAS} of 1.40V *(Figure 6)*. In this case the DAC transfer function is

$$V_{OUT} = 2.5 \frac{(DATA)}{256} + 0.310$$

The output impedance of any external reference that is used will affect the accuracy of the conversion. In order that this error be less than $\frac{1}{2}$ LSB, the output impedance of the external reference must be less than 7.8Ω.

FIGURE 5. Equivalent Circuit of R-2R Ladder and Output Amplifier

FIGURE 6. Generating a V_{BIAS} = 1.40V from the Internal Reference

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Digital Interface

The DAC0854 has two interface modes: a WRITE mode and a READ mode. The WRITE mode is used to convert an 8-bit digital input word into a voltage. The READ mode is used to read back the digital data that was sent to one or all of the DACs. These modes are selected by the appropriate setting of the RD/$\overline{\text{WR}}$ bit, which is part of the instruction byte. The instruction byte precedes the data byte at the DI pin. In both modes, a high level on the Start Bit (SB) alerts the DAC to respond to the remainder of the input stream.

Table I lists the instruction set for the WRITE mode when writing to only a single DAC, and Table II lists the instruction set for a global write. The DACs are always written to LSB first. All DACs will be written to if the global bit (G) is high; DAC 1 is written to first, then DACs 2, 3 and 4 (in that order). If the update bit is high, then the DAC output will be updated on the rising edge of $\overline{\text{CS}}$; otherwise, the new data byte will be placed only in the input register. Chip Select ($\overline{\text{CS}}$) must remain low for at least one clock cycle after the last data bit has been entered. (See *Figures 1* and *2*)

TABLE I. WRITE Mode Instruction Set (Writing to a Single DAC)

SB	RD/$\overline{\text{WR}}$	G	U	A1	A0	Description
Bit #1	Bit #2	Bit #3	Bit #4	Bit #5	Bit #6	
1	0	0	0	0	0	Write DAC 1, no update of DAC outputs
1	0	0	0	0	1	Write DAC 2, no update of DAC outputs
1	0	0	0	1	0	Write DAC 3, no update of DAC outputs
1	0	0	0	1	1	Write DAC 4, no update of DAC outputs
1	0	0	1	0	0	Write DAC 1, update DAC 1 on $\overline{\text{CS}}$ rising edge
1	0	0	1	0	1	Write DAC 2, update DAC 2 on $\overline{\text{CS}}$ rising edge
1	0	0	1	1	0	Write DAC 3, update DAC 3 on $\overline{\text{CS}}$ rising edge
1	0	0	1	1	1	Write DAC 4, update DAC 4 on $\overline{\text{CS}}$ rising edge

TABLE II. WRITE Mode Instruction Set (Writing to all DACs)

SB	RD/$\overline{\text{WR}}$	G	U	Description
Bit # 1	Bit #2	Bit #3	Bit #4	
1	0	1	0	Write all DACs, no update of outputs
1	0	1	1	Write all DACs, update all outputs on $\overline{\text{CS}}$ rising edge

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Digital Interface (Continued)

Table III lists the instruction set for the READ mode. By the appropriate setting of the global (G) and address (A1 and A0) bits, one can select a specific DAC to be read, or one can read all the DACs in succession, starting with DAC 1. The $R/\overline{F}$ bit determines whether the data changes on the rising or the falling edge of the system clock. With the $R/\overline{F}$ bit high, the data changes on the rising edge that occurs $1\frac{1}{2}$ clock cycles after the end of the instruction byte. With the $R/\overline{F}$ bit low, the data changes on the falling edge that oc-

curs 1 clock cycle after the end of the instruction byte. One can choose to read the data back MSB first or LSB first by setting the $M/\overline{L}$ bit. (See *Figures 3* and *4*)

An asynchronous update of all the DAC outputs can be achieved by taking $\overline{AU}$ low. The contents of the input registers are loaded into the DAC registers, with the update occurring on the falling edge of $\overline{AU}$. $\overline{CS}$ must be held high during an asynchronous update.

All DAC registers will have their contents reset to all zeros on power up.

TABLE III. READ MODE Instruction Set

SB	RD/$\overline{WR}$	G	R/$\overline{F}$	M/$\overline{L}$	A1	A0	Description
Bit #1	Bit #2	Bit #3	Bit #4	Bit #5	Bit #6	Bit #7	
1	1	0	0	0	0	0	Read DAC 1, LSB first, data changes on the falling edge
1	1	0	0	0	0	1	Read DAC 2, LSB first, data changes on the falling edge
1	1	0	0	0	1	0	Read DAC 3, LSB first, data changes on the falling edge
1	1	0	0	0	1	1	Read DAC 4, LSB first, data changes on the falling edge
1	1	0	0	1	0	0	Read DAC 1, MSB first, data changes on the falling edge
1	1	0	0	1	0	1	Read DAC 2, MSB first, data changes on the falling edge
1	1	0	0	1	1	0	Read DAC 3, MSB first, data changes on the falling edge
1	1	0	0	1	1	1	Read DAC 4, MSB first, data changes on the falling edge
1	1	0	1	0	0	0	Read DAC 1, LSB first, data changes on the rising edge
1	1	0	1	0	0	1	Read DAC 2, LSB first, data changes on the rising edge
1	1	0	1	0	1	0	Read DAC 3, LSB first, data changes on the rising edge
1	1	0	1	0	1	1	Read DAC 4, LSB first, data changes on the rising edge
1	1	0	1	1	0	0	Read DAC 1, MSB first, data changes on the rising edge
1	1	0	1	1	0	1	Read DAC 2, MSB first, data changes on the rising edge
1	1	0	1	1	1	0	Read DAC 3, MSB first, data changes on the rising edge
1	1	0	1	1	1	1	Read DAC 4, MSB first, data changes on the rising edge
1	1	1	0	0	1	0	Read all DACs, LSB first, data changes on the falling edge
1	1	1	0	1	1	0	Read all DACs, MSB first, data changes on the falling edge
1	1	1	1	0	1	0	Read all DACs, LSB first, data changes on the rising edge
1	1	1	1	1	1	0	Read all DACs, MSB first, data changes on the rising edge

Power Fail Function

If a power failure occurs on the system using the DAC0854 then the $\overline{INT}$ pin will be pulled low on the next power-up cycle. To force this output high again and reset this flag, the $\overline{CS}$ pin will have to be brought low. When this is done the $\overline{INT}$ output will be pulled high again via an external 10 kΩ pull-up resistor. This feature may be used by the microprocessor to discard data whose integrity is in question.

Power Supplies

The DAC0854 is designed to operate from a $+5V$ (nominal) supply. There are two supply pins, AV_{CC} and DV_{CC}. These pins allow separate external bypass capacitors for the analog and digital portions of the circuit. To guarantee accurate conversions, the two supply pins should each be bypassed with a 0.1 μF ceramic capacitor in parallel with a 10 μF tantalum capacitor.
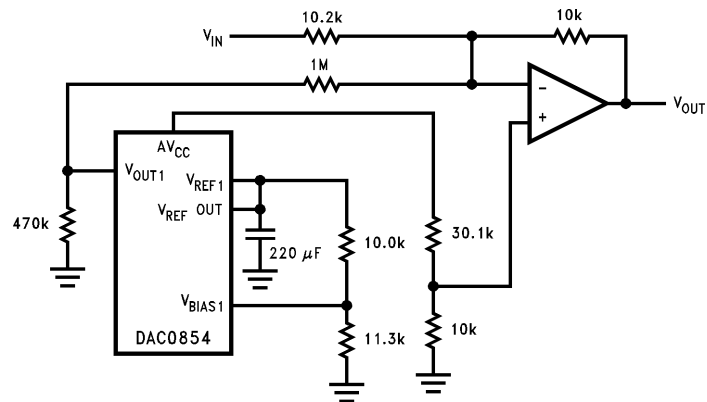
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Typical Applications

TL/H/11261–18

FIGURE 7. Trimming the Offset of a 5V Op Amp Biased at Mid Supply
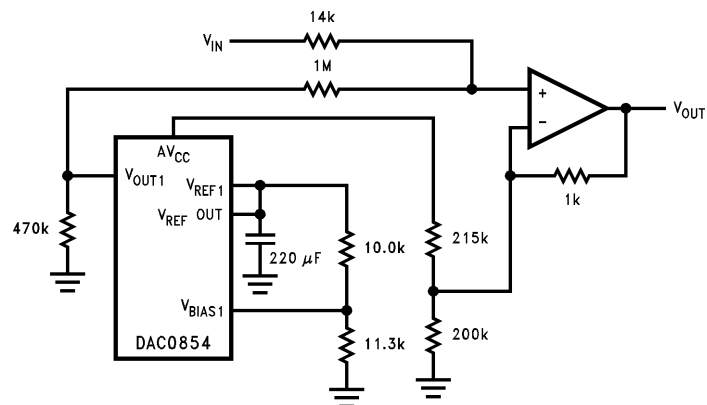

TL/H/11261–19

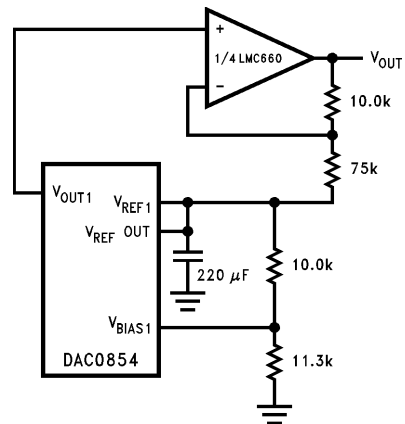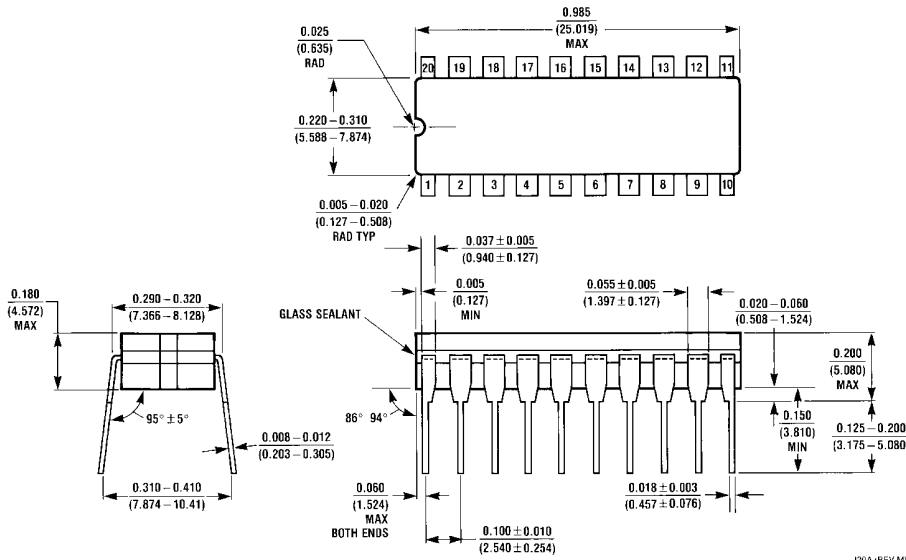**FIGURE 8. Trimming the Offset of a Dual Supply Op Amp Biased at Ground**

TL/H/11261–20
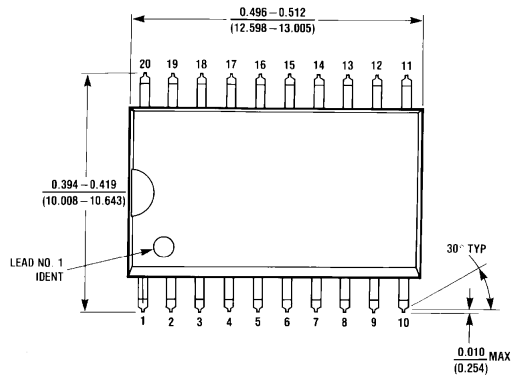
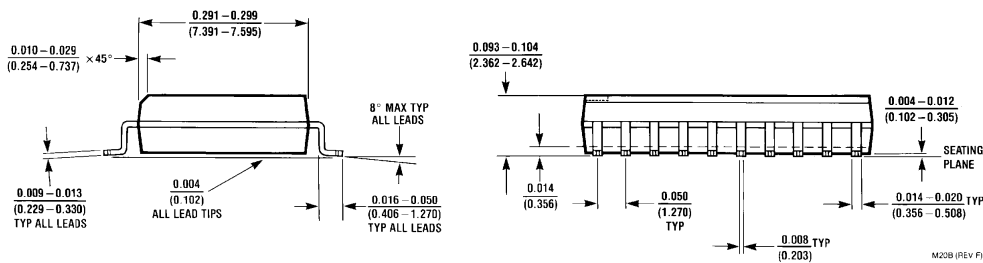**FIGURE 9. Bringing the Output Range Down to Ground**

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Physical Dimensions inches (millimeters)

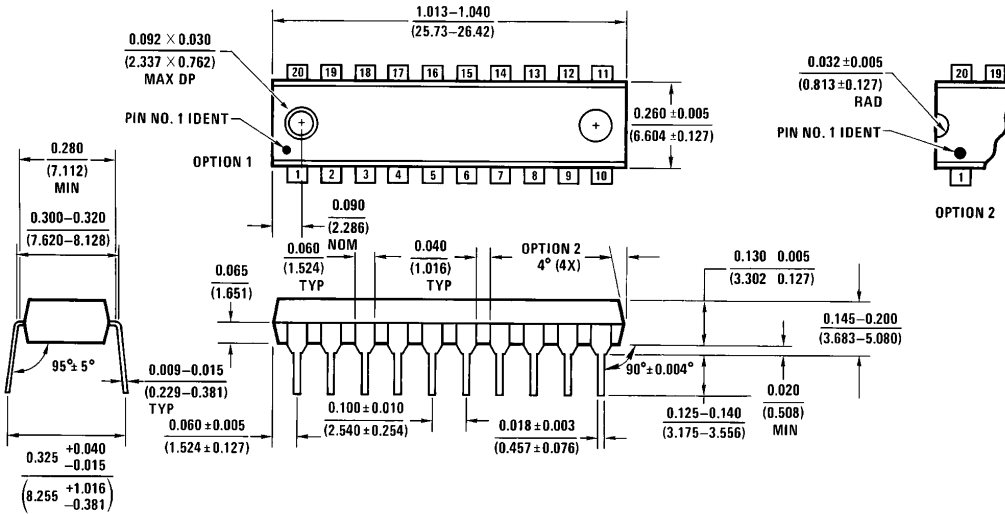**Order Number DAC0854CIJ or DAC0854CMJ/883**
NS Package Number J20A

Order Number DAC0854BIWM or DAC0854CIWM
NS Package Number M20B

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Physical Dimensions inches (millimeters) (Continued)

N20A (REV G)

Order Number DAC0854BIN or DAC0854CIN
NS Package Number N20A

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