Features

- 4.5V to 5.5V Read/Write
- Access Time - 70 ns
- Sector Erase Architecture
  - Thirty 32K Word (64K byte) Sectors with Individual Write Lockout
  - Eight 4K Word (8K byte) Sectors with Individual Write Lockout
  - Two 16K Word (32K byte) Sectors with Individual Write Lockout
- Fast Word Program Time - 10 µs
- Fast Sector Erase Time - 200 ms
- Dual Plane Organization, Permitting Concurrent Read while Program/Erase
  - Memory Plane A: Eight 4K Word, Two 16K Word and Six 32K Word Sectors
  - Memory Plane B: Twenty-Four 32K Word Sectors
- Erase Suspend Capability
  - Supports Reading/Programming Data from Any Sector by Suspending Erase of Any Different Sector
- Low Power Operation
  - 40 mA Active
  - 10 µA Standby
- Data Polling, Toggle Bit, Ready/Busy for End of Program Detection
- RESET Input for Device Initialization
- Sector Program Unlock Command
- TSOP, CBGA, and µBGA Package Options
- Top or Bottom Boot Block Configuration Available

Description

The AT49F16X4(T) is a 5.0 volt 16-megabit Flash memory organized as 1,048,576 words of 16 bits each or 2,097,152 bytes of 8 bits each. The x16 data appears on I/O0 - I/O15; the x8 data appears on I/O0 - I/O7. The memory is divided into 40 blocks for erase operations. The device is offered in 48-pin TSOP and 48-ball µBGA packages. The device has CE, and OE control signals to avoid any bus contention. This device can be read or reprogrammed using a single 5.0V power supply, making it ideally suited for in-system programming.

(continued)

Pin Configurations

Pin Name	Function
A0 - A19	Addresses
CE	Chip Enable
OE	Output Enable
WE	Write Enable
RESET	Reset
RDY/BUSY	READY/BUSY Output
I/O0 - I/O14	Data Inputs/Outputs
I/O15 (A-1)	I/O15 (Data Input/Output, Word Mode) A-1 (LSB Address Input, Byte Mode)
BYTE	Selects Byte or Word Mode
NC	No Connect
DC	Don't Connect

16-Megabit (1M x 16/2M x 8) 5-volt Only Flash Memory

AT49F1604
AT49F1604T
AT49F1614
AT49F1614T
Advance Information

Rev. 0977B–06/98

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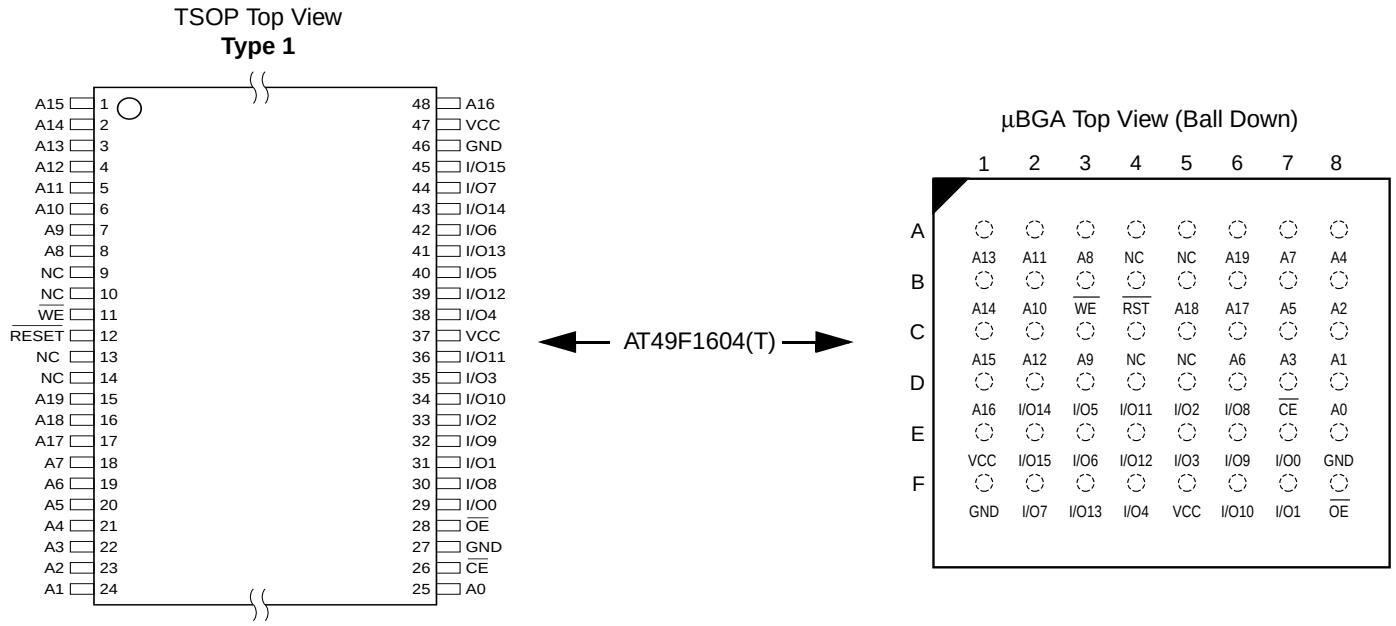

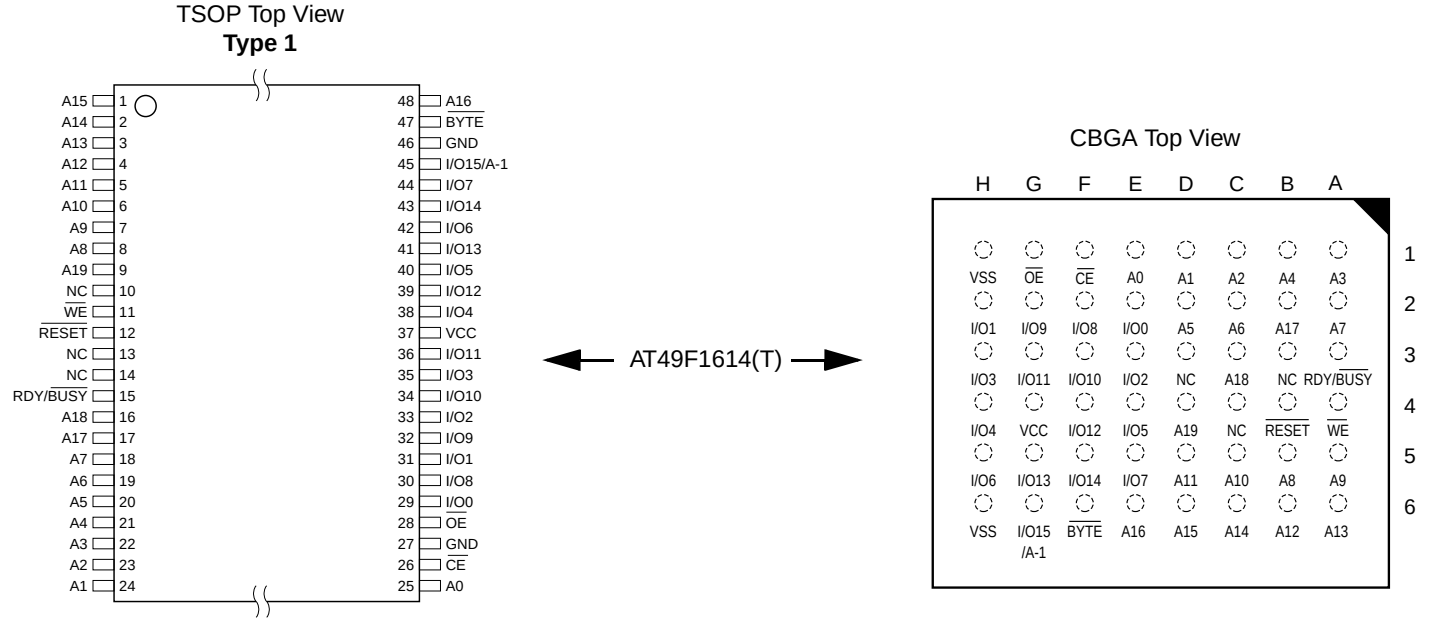

The device powers on in the read mode. Command sequences are used to place the device in other operation modes such as program and erase. The device has the capability to protect the data in any sector. Once the data protection for a given sector is enabled, the data in that sector cannot be changed using input levels between ground and V_{CC}.

The device is segmented into two memory planes. Reads from memory plane B may be performed even while program or erase functions are being executed in memory plane A and vice versa. This operation allows improved system performance by not requiring the system to wait for a program or erase operation to complete before a read is performed. To further increase the flexibility of the device, it contains an Erase Suspend feature. This feature will put the Erase on hold for any amount of time and let the user read data from or program data to any of the remaining sectors within the same memory plane. There is no reason to suspend the erase operation if the data to be read is in the other memory plane. The end of a program or an Erase cycle is detected by the Ready/Busy pin, Data polling, or by the toggle bit.

A six byte command (bypass unlock) sequence to remove the requirement of entering the three byte program sequence is offered to further improve programming time. After entering the six byte code, only single pulses on the write control lines are required for writing into the device. This mode (single pulse byte/word program) is exited by

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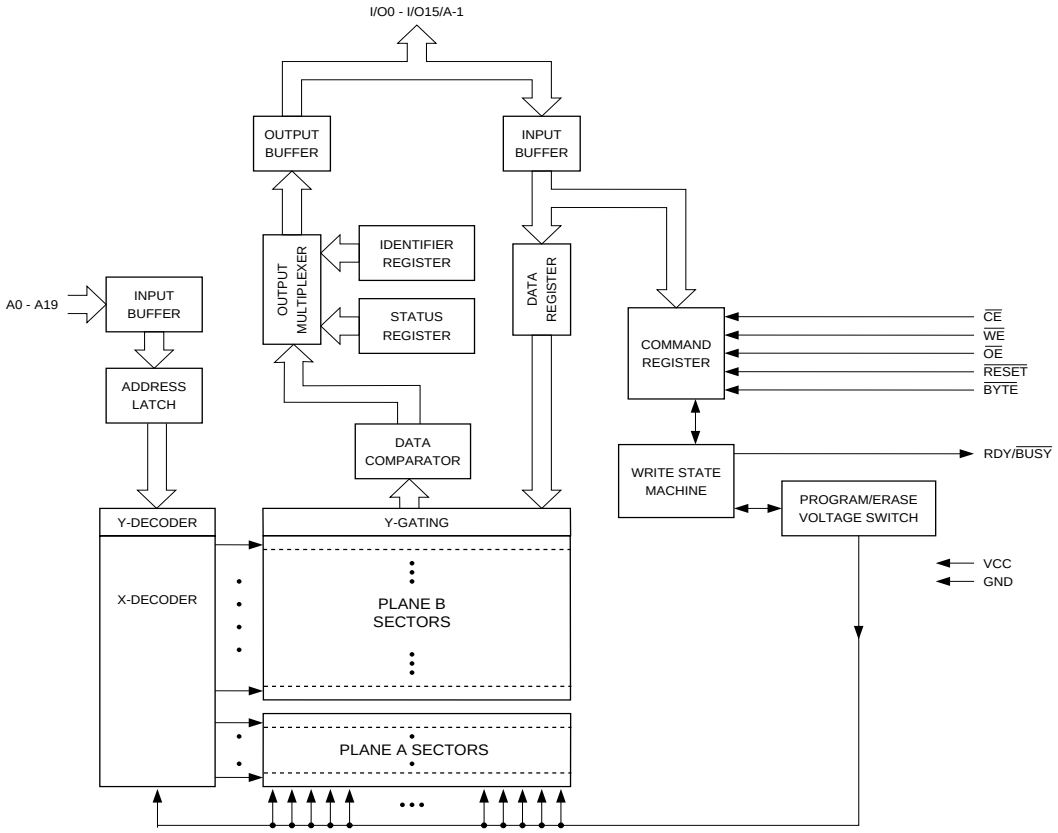
powering down the device, or by pulsing the $\overline{\text{RESET}}$ pin low and then bringing it back to V_{CC}. Erase and Erase Suspend/Resume commands will not work while in this mode; if entered they will result in data being programmed into the device. It is not recommended that the six byte code reside in the software of the final product but only exist in external programming code.

The $\overline{\text{BYTE}}$ pin controls whether the device data I/O pins operate in the byte or word configuration. If the $\overline{\text{BYTE}}$ pin is set at logic “1”, the device is in word configuration, I/O0-I/O15 are active and controlled by $\overline{\text{CE}}$ and $\overline{\text{OE}}$.

If the $\overline{\text{BYTE}}$ pin is set at logic “0”, the device is in byte configuration, and only data I/O pins I/O0-I/O7 are active and controlled by $\overline{\text{CE}}$ and $\overline{\text{OE}}$. The data I/O pins I/O8-I/O14 are tri-stated, and the I/O15 pin is used as an input for the LSB (A-1) address function.

Block Diagram



Device Operation

READ: The AT49F16X4(T) is accessed like an EPROM. When $\overline{\text{CE}}$ and $\overline{\text{OE}}$ are low and $\overline{\text{WE}}$ is high, the data stored at the memory location determined by the address pins are asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{\text{CE}}$ or $\overline{\text{OE}}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

COMMAND SEQUENCES: When the device is first powered on it will be reset to the read or standby mode depending upon the state of the control line inputs. In order to perform other device functions, a series of command sequences are entered into the device. The command sequences are shown in the Command Definitions table (I/O8 - I/O15 are don't care inputs for the command codes). The command sequences are written by applying a low pulse on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ input with $\overline{\text{CE}}$ or $\overline{\text{WE}}$ low (respectively) and $\overline{\text{OE}}$ high. The address is latched on the falling edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$, whichever occurs last. The data is latched by the first rising edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$. Standard microprocessor write timings are used. The address locations used in the command sequences are not affected by entering the command sequences.

RESET: A $\overline{\text{RESET}}$ input pin is provided to ease some system applications. When $\overline{\text{RESET}}$ is at a logic high level, the device is in its standard operating mode. A low level on the $\overline{\text{RESET}}$ input halts the present device operation and puts

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the outputs of the device in a high impedance state. When a high level is reasserted on the RESET pin, the device returns to the Read or Standby mode, depending upon the state of the control inputs. By applying a 12V ± 0.5V input signal to the RESET pin any sector can be reprogrammed even if the sector lockout feature has been enabled (see Sector Programming Lockout Override section).

ERASURE: Before a byte/word can be reprogrammed, it must be erased. The erased state of memory bits is a logical "1". The entire device can be erased by using the Chip Erase command or individual sectors can be erased by using the Sector Erase commands.

CHIP ERASE: The entire device can be erased at one time by using the 6-byte chip erase software code. After the chip erase has been initiated, the device will internally time the erase operation so that no external clocks are required. The maximum time to erase the chip is t_{EC}.

If the sector lockout has been enabled, the Chip Erase will not erase the data in the sector that has been locked; it will erase only the unprotected sectors. After the chip erase, the device will return to the read or standby mode.

SECTOR ERASE: As an alternative to a full chip erase, the device is organized into forty sectors (SA0 - SA39) that can be individually erased. The Sector Erase command is a six bus cycle operation. The sector address is latched on the falling WE edge of the sixth cycle while the 30H data input command is latched on the rising edge of WE. The sector erase starts after the rising edge of WE of the sixth cycle. The erase operation is internally controlled; it will automatically time to completion. The maximum time to erase a section is t_{SEC}. When the sector programming lockout feature is not enabled, the sector will erase (from the same sector erase command). Once a sector has been protected, data in the protected sectors cannot be changed unless the RESET pin is taken to 12V ± 0.5V. An attempt to erase a sector that has been protected will result in the operation terminating in 2 µs.

BYTE/WORD PROGRAMMING: Once a memory block is erased, it is programmed (to a logical "0") on a byte-by-byte or on a word-by-word basis. Programming is accomplished via the internal device command register and is a 4-bus cycle operation. The device will automatically generate the required internal program pulses.

Any commands written to the chip during the embedded programming cycle will be ignored. If a hardware reset happens during programming, the data at the location being programmed will be corrupted. Please note that a data "0" cannot be programmed back to a "1"; only erase operations can convert "0"s to "1"s. Programming is completed after the specified t_{BP} cycle time. The DATA polling feature or the toggle bit feature may be used to indicate the end of a program cycle.

SECTOR PROGRAMMING LOCKOUT: Each sector has a programming lockout feature. This feature prevents programming of data in the designated sectors once the feature has been enabled. These sectors can contain secure code that is used to bring up the system. Enabling the lockout feature will allow the boot code to stay in the device while data in the rest of the device is updated. This feature does not have to be activated; any sector's usage as a write protected region is optional to the user.

Once the feature is enabled, the data in the protected sectors can no longer be erased or programmed when input levels of 5.5V or less are used. Data in the remaining sectors can still be changed through the regular programming method. To activate the lockout feature, a series of six program commands to specific addresses with specific data must be performed. Please refer to the Command Definitions table.

SECTOR PROGRAMMING LOCKOUT OVERRIDE: The user can override the sector programming lockout by taking the RESET pin to 12V ± 0.5V. By doing this protected data can be altered through a chip erase, sector erase or byte/word programming. When the RESET pin is brought back to TTL levels the sector programming lockout feature is again active.

ERASE SUSPEND/ERASE RESUME: The erase suspend command allows the system to interrupt a sector erase operation and then program or read data from a different sector within the same plane. Since this device has a dual plane architecture, there is no need to use the erase suspend feature while erasing a sector when you want to read data from a sector in the other plane. After the erase suspend command is given, the device requires a maximum time of 15 µs to suspend the erase operation. After the erase operation has been suspended, the plane which contains the suspended sector enters the erase-suspend-read mode. The system can then read data or program data to any other sector within the device. An address is not required during the erase suspend command. During a sector erase suspend, another sector cannot be erased. To resume the sector erase operation, the system must write the erase resume command. The erase resume command is a one bus cycle command, which does require the plane address (determined by A18 and A19). The device also supports an erase suspend during a complete chip erase. While the chip erase is suspended, the user can read from any sector within the memory that is protected. The command sequence for a chip erase suspend and a sector erase suspend are the same.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product.

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For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

DATA POLLING: The AT49F16X4(T) features $\overline{\text{DATA}}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte/word loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. During a chip or sector erase operation, an attempt to read the device will give a "0" on I/O7. Once the program or erase cycle has completed, true data will be read from the device. $\overline{\text{DATA}}$ polling may begin at any time during the program cycle. Please see "Status Bit Table" for more details.

TOGGLE BIT: In addition to $\overline{\text{DATA}}$ polling the AT49F16X4(T) provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the same memory plane will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

An additional toggle bit is available on I/O2 which can be used in conjunction with the toggle bit which is available on I/O6. While a sector is erase suspended, a read or a program operation from the suspended sector will result in the I/O2 bit toggling. Please see "Status Bit Table" for more details.

RDY/$\overline{\text{BUSY}}$: An open drain READY/$\overline{\text{BUSY}}$ output pin provides another method of detecting the end of a program or erase operation. RDY/$\overline{\text{BUSY}}$ is actively pulled low during the internal program and erase cycles and is released at the completion of the cycle. The open drain connection allows for OR-tying of several devices to the same RDY/$\overline{\text{BUSY}}$ line.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT49F16X4(T) in the following ways: (a) V_{CC} sense: if V_{CC} is below 3.8V (typical), the program function is inhibited. (b) V_{CC} power on delay: once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 10 ms (typical) before programming. (c) Program inhibit: holding any one of $\overline{\text{OE}}$ low, $\overline{\text{CE}}$ high or $\overline{\text{WE}}$ high inhibits program cycles. (d) Noise filter: pulses of less than 15 ns (typical) on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ inputs will not initiate a program cycle.

INPUT LEVELS: While operating with a 4.5V to 5.5V power supply, the address inputs and control inputs ($\overline{\text{OE}}$, $\overline{\text{CE}}$, and $\overline{\text{WE}}$) may be driven from 0 to 5.5V without adversely affecting the operation of the device. The I/O lines can only be driven from 0 to V_{CC} + 0.6V.

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Command Definition in (Hex)[1]

Command Sequence	Bus Cycles	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	Addr	D_{OUT}										
Chip Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	10
Sector Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	SA[3][4]	30
Byte/Word Program	4	5555	AA	2AAA	55	5555	A0	Addr	D_{IN}				
Bypass Unlock	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	A0
Single Pulse Byte/Word Program	1	Addr	D_{IN}										
Sector Lockout	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	SA[3][4]	40
Erase Suspend	1	xxxx	B0										
Erase Resume	1	PA[5]	30										
Product ID Entry	3	5555	AA	2AAA	55	5555	90						
Product ID Exit[2]	3	5555	AA	2AAA	55	5555	F0						
Product ID Exit[2]	1	xxxx	F0										

Notes:
1. The DATA FORMAT in each bus cycle is as follows: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex).
   The ADDRESS FORMAT in each bus cycle is as follows: A15 - A0 (Hex), A-1, A14 - A19 (Don't Care).
2. Either one of the Product ID Exit commands can be used.
3. SA = sector address. Any byte/word address within a sector can be used to designate the sector address (see next four pages for details).
4. When the sector programming lockout feature is not enabled, the sector will erase (from the same sector erase command). Once the sector has been protected, data in the protected sectors cannot be changed unless the $\overline{\text{RESET}}$ pin is taken to 12V ± 0.5V.
5. PA is the plane address (A19 - A18).

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{\text{OE}}$ with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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Memory Plane A - Bottom Boot

Sector	Size (Bytes/Words)	x8 Address Range (A19 - A-1)	x16 Address Range (A19 - A0)
SA0	8K/4K	000000 - 001FFF	00000 - 00FFF
SA1	8K/4K	002000 - 003FFF	01000 - 01FFF
SA2	8K/4K	004000 - 005FFF	02000 - 02FFF
SA3	8K/4K	006000 - 007FFF	03000 - 03FFF
SA4	8K/4K	008000 - 009FFF	04000 - 04FFF
SA5	8K/4K	00A000 - 00BFFF	05000 - 05FFF
SA6	8K/4K	00C000 - 00DFFF	06000 - 06FFF
SA7	8K/4K	00E000 - 00FFFF	07000 - 07FFF
SA8	32K/16K	010000 - 017FFF	08000 - 0BFFF
SA9	32K/16K	018000 - 01FFFF	0C000 - 0FFFF
SA10	64K/32K	020000 - 02FFFF	10000 - 17FFF
SA11	64K/32K	030000 - 03FFFF	18000 - 1FFFF
SA12	64K/32K	040000 - 04FFFF	20000 - 27FFF
SA13	64K/32K	050000 - 05FFFF	28000 - 2FFFF
SA14	64K/32K	060000 - 06FFFF	30000 - 37FFF
SA15	64K/32K	070000 - 07FFFF	38000 - 3FFFF

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Memory Plane B - Bottom Boot

Sector	Size (Bytes/Words)	x8 Address Range (A19 - A-1)	x16 Address Range (A19 - A0)
SA16	64K/32K	080000 - 08FFFF	40000 - 47FFF
SA17	64K/32K	090000 - 09FFFF	48000 - 4FFFF
SA18	64K/32K	0A0000 - 0AFFFF	50000 - 57FFF
SA19	64K/32K	0B0000 - 0BFFFF	58000 - 5FFFF
SA20	64K/32K	0C0000 - 0CFFFF	60000 - 67FFF
SA21	64K/32K	0D0000 - 0DFFFF	68000 - 6FFFF
SA22	64K/32K	0E0000 - 0EFFFF	70000 - 77FFF
SA23	64K/32K	0F0000 - 0FFFFF	78000 - 7FFFF
SA24	64K/32K	100000 - 10FFFF	80000 - 87FFF
SA25	64K/32K	110000 - 11FFFF	88000 - 8FFFF
SA26	64K/32K	120000 - 12FFFF	90000 - 97FFF
SA27	64K/32K	130000 - 13FFFF	98000 - 9FFFF
SA28	64K/32K	140000 - 14FFFF	A0000 - A7FFF
SA29	64K/32K	150000 - 15FFFF	A8000 - AFFFF
SA30	64K/32K	160000 - 16FFFF	B0000 - B7FFF
SA31	64K/32K	170000 - 17FFFF	B8000 - BFFFF
SA32	64K/32K	180000 - 18FFFF	C0000 - C7FFF
SA33	64K/32K	190000 - 19FFFF	C8000 - CFFFF
SA34	64K/32K	1A0000 - 1AFFFF	D0000 - D7FFF
SA35	64K/32K	1B0000 - 1BFFFF	D8000 - DFFFF
SA36	64K/32K	1C0000 - 1CFFFF	E0000 - E7FFF
SA37	64K/32K	1D0000 - 1DFFFF	E8000 - EFFFF
SA38	64K/32K	1E0000 - 1EFFFF	F0000 - F7FFF
SA39	64K/32K	1F0000 - 1FFFFF	F8000 - FFFFF

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Memory Plane B - Top Boot

Sector	Size (Bytes/Words)	x8 Address Range (A19 - A-1)	x16 Address Range (A19 - A0)
SA0	64K/32K	000000 - 00FFFF	00000 - 07FFF
SA1	64K/32K	010000 - 01FFFF	08000 - 0FFFF
SA2	64K/32K	020000 - 02FFFF	10000 - 17FFF
SA3	64K/32K	030000 - 03FFFF	18000 - 1FFFF
SA4	64K/32K	040000 - 04FFFF	20000 - 27FFF
SA5	64K/32K	050000 - 05FFFF	28000 - 2FFFF
SA6	64K/32K	060000 - 06FFFF	30000 - 37FFF
SA7	64K/32K	070000 - 07FFFF	38000 - 3FFFF
SA8	64K/32K	080000 - 08FFFF	40000 - 47FFF
SA9	64K/32K	090000 - 09FFFF	48000 - 4FFFF
SA10	64K/32K	0A0000 - 0AFFFF	50000 - 57FFF
SA11	64K/32K	0B0000 - 0BFFFF	58000 - 5FFFF
SA12	64K/32K	0C0000 - 0CFFFF	60000 - 67FFF
SA13	64K/32K	0D0000 - 0DFFFF	68000 - 6FFFF
SA14	64K/32K	0E0000 - 0EFFFF	70000 - 77FFF
SA15	64K/32K	0F0000 - 0FFFFF	78000 - 7FFFF
SA16	64K/32K	100000 - 10FFFF	80000 - 87FFF
SA17	64K/32K	110000 - 11FFFF	88000 - 8FFFF
SA18	64K/32K	120000 - 12FFFF	90000 - 97FFF
SA19	64K/32K	130000 - 13FFFF	98000 - 9FFFF
SA20	64K/32K	140000 - 14FFFF	A0000 - A7FFF
SA21	64K/32K	150000 - 15FFFF	A8000 - AFFFF
SA22	64K/32K	160000 - 16FFFF	B0000 - B7FFF
SA23	64K/32K	170000 - 17FFFF	B8000 - BFFFF

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Memory Plane A - Top Boot

Sector	Size (Bytes/Words)	x8 Address Range (A19 - A-1)	x16 Address Range (A19 - A0)
SA24	64K/32K	180000 - 18FFFF	C0000 - C7FFF
SA25	64K/32K	190000 - 19FFFF	C8000 - CFFFF
SA26	64K/32K	1A0000 - 1AFFFF	D0000 - D7FFF
SA27	64K/32K	1B0000 - 1BFFFF	D8000 - DFFFF
SA28	64K/32K	1C0000 - 1CFFFF	E0000 - E7FFF
SA29	64K/32K	1D0000 - 1DFFFF	E8000 - EFFFF
SA30	32K/16K	1E0000 - 1E7FFF	F0000 - F3FFF
SA31	32K/16K	1E8000 - 1EFFFF	F4000 - F7FFF
SA32	8K/4K	1F0000 - 1F1FFF	F8000 - F8FFF
SA33	8K/4K	1F2000 - 1F3FFF	F9000 - F9FFF
SA34	8K/4K	1F4000 - 1F5FFF	FA000 - FAFFF
SA35	8K/4K	1F6000 - 1F7FFF	FB000 - FBFFF
SA36	8K/4K	1F8000 - 1F9FFF	FC000 - FCFFF
SA37	8K/4K	1FA000 - 1FBFFF	FD000 - FDFFF
SA38	8K/4K	1FC000 - 1FDFFF	FE000 - FEFFF
SA39	8K/4K	1FE000 - 1FFFFF	FF000 - FFFFF

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DC and AC Operating Range

		AT49F16X4(T)-70	AT49F16X4(T)-90
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		4.5V to 5.5V	4.5V to 5.5V

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RESET}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Ai	D_{OUT}
Program/Erase[2]	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Ai	D_{IN}
Standby/Program Inhibit	V_{IH}	X[1]	X	V_{IH}	X	High Z
Program Inhibit	X	X	V_{IH}	V_{IH}		
Program Inhibit	X	V_{IL}	X	V_{IH}		
Output Disable	X	V_{IH}	X	V_{IH}		High Z
Reset	X	X	X	V_{IL}	X	High Z
Product Identification						
Hardware	V_{IL}	V_{IL}	V_{IH}	V_{IH}	A1 - A19 = V_{IL}, A9 = V_H[3] A0 = V_{IL}	Manufacturer Code[4]
					A1 - A19 = V_{IL}, A9 = V_H[3] A0 = V_{IH}	Device Code[4]
Software[5]				V_{IH}	A0 = V_{IL}, A1 - A19 = V_{IL}	Manufacturer Code[4]
					A0 = V_{IH}, A1 - A19 = V_{IL}	Device Code[4]

Notes:
1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Waveforms.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code: 1FH (x8); 161F (x16), Device Code: C0H (x8)-AT49F16X4; 16CO (x16)-AT49F16X4; C2H (x8)-AT49F16X4T; 16C2 (x16)-AT49F16X4T.
5. See details under Software Product Identification Entry/Exit.

DC Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}		10	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}		1	mA
I_{CC} [1]	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		40	mA
I_{CCRW}	V_{CC} Read While Write Current	f = 5 MHz; I_{OUT} = 0 mA		60	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA	2.4		V

Note: 1. In the erase mode, I_{CC} is 50 mA.

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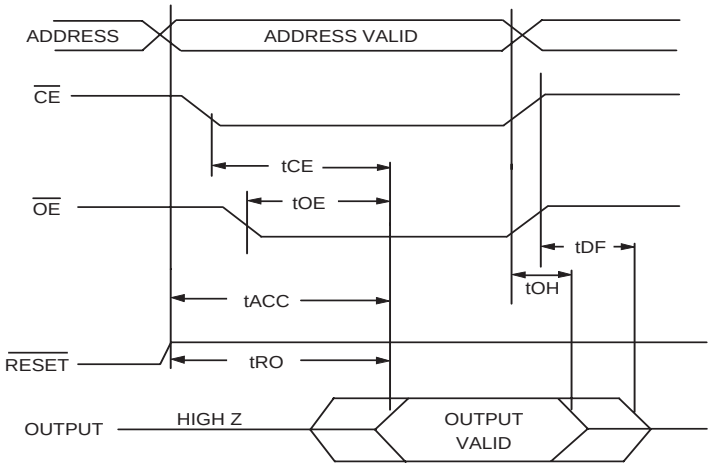
AC Read Characteristics

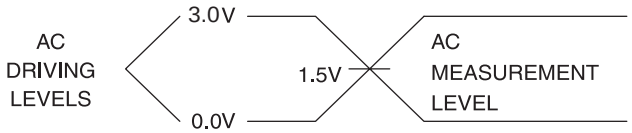
Symbol	Parameter	AT49F16X4(T)-70		AT49F16X4(T)-90		Units
		Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		70		90	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		70		90	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	35	0	40	ns
t_{DF}[3][4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	25	0	25	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		ns
t_{RO}	$\overline{RESET}$ to Output Delay		800		800	ns

AC Read Waveforms[1][2][3][4]



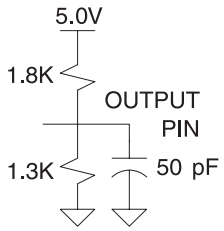
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (CL = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

Output Test Load



Pin Capacitance

f = 1 MHz, T = 25°C[1]

	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

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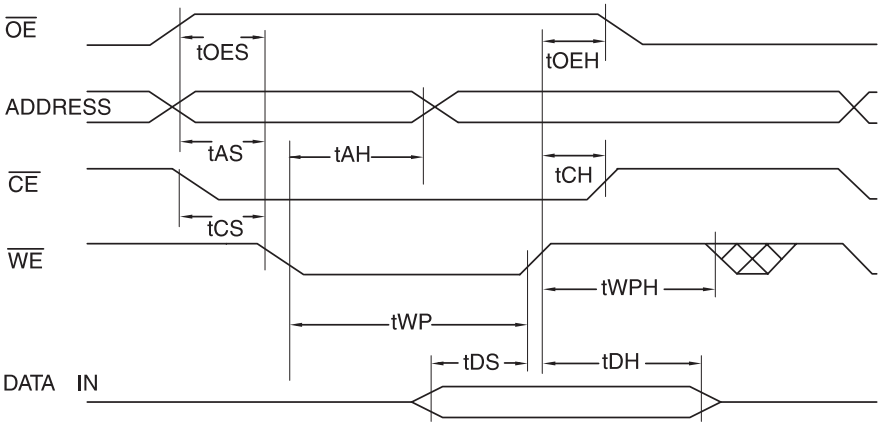
AC Byte/Word Load Characteristics

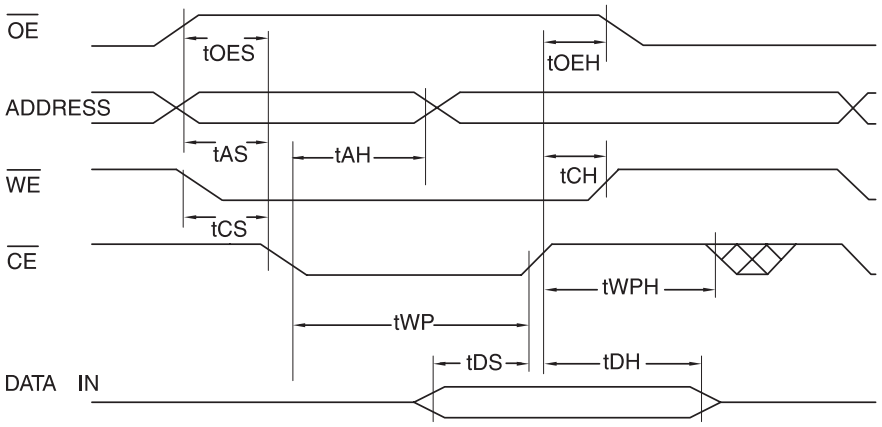
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{WPH}	Write Pulse Width High	50		ns

AC Byte/Word Load Waveforms

$\overline{WE}$ Controlled



$\overline{CE}$ Controlled



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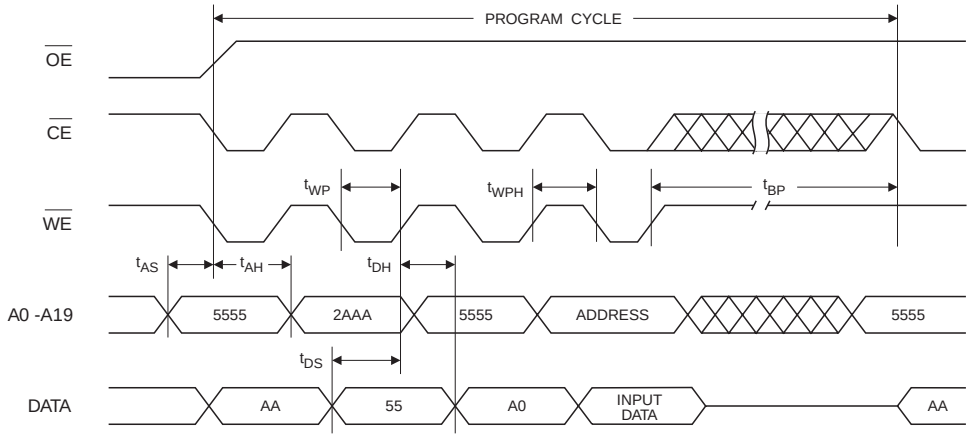
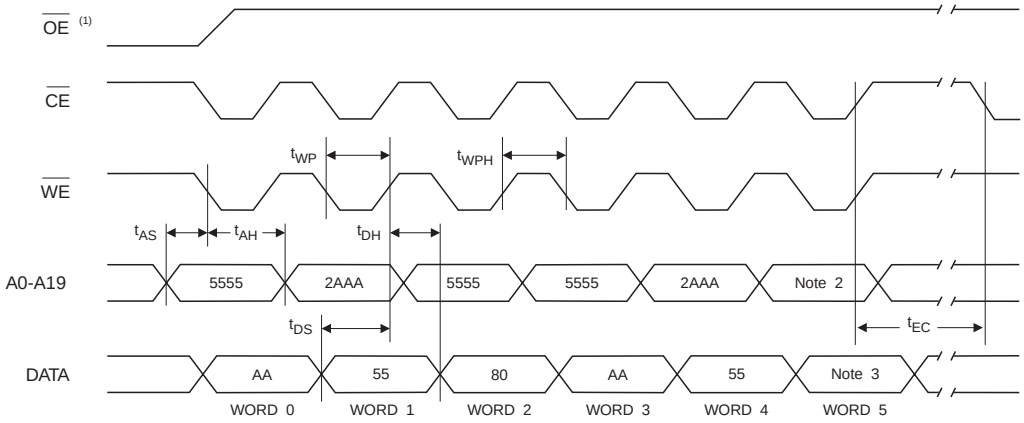
Program Cycle Characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{BP}	Byte/Word Programming Time		10	50	µs
t_{AS}	Address Set-up Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{DS}	Data Set-up Time	50			ns
t_{DH}	Data Hold Time	0			ns
t_{WP}	Write Pulse Width	100			ns
t_{WPH}	Write Pulse Width High	50			ns
t_{EC}	Chip Erase Cycle Time			10	seconds
t_{SEC}	Sector Erase Cycle Time		200		ms

Program Cycle Waveforms



Sector or Chip Erase Cycle Waveforms



Notes:
1. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.
2. For chip erase, the address should be 5555. For sector erase, the address depends on what sector is to be erased. (See note 3 under command definitions.)
3. For chip erase, the data should be 10H, and for sector erase, the data should be 30H.

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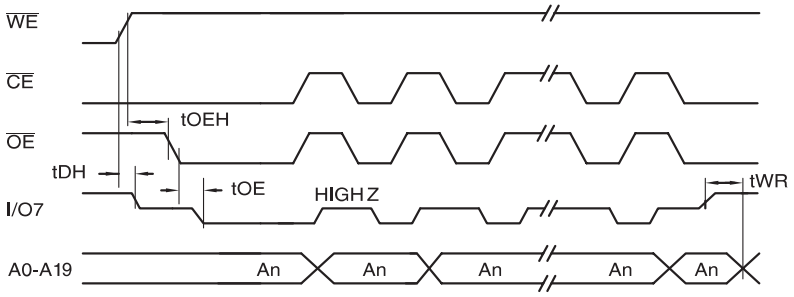
$\overline{\text{Data}}$ Polling Characteristics(1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay(2)				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

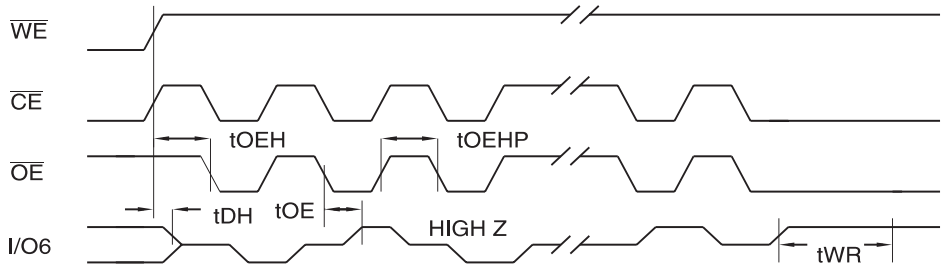


Toggle Bit Characteristics(1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay(2)				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Toggle Bit Waveforms(1)(2)(3)



Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
The t_{OEHP} specification must be met by the toggling input(s).
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

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Status Bit Table

	Status Bit					
	I/O 7		I/O 6		I/O 2	
Read Address In	**Plane A**	**Plane B**	**Plane A**	**Plane B**	**Plane A**	**Plane B**
While						
Programming in Plane A	$\overline{I/O7}$	DATA	TOGGLE	DATA	1	DATA
Programming in Plane B	DATA	$\overline{I/O7}$	DATA	TOGGLE	DATA	1
Erasing in Plane A	0	DATA	TOGGLE	DATA	TOGGLE	DATA
Erasing in Plane B	DATA	0	DATA	TOGGLE	DATA	TOGGLE
Erase Suspended & Read Erasing Sector	1	1	1	1	TOGGLE	TOGGLE
Erase Suspended & Read Non-Erasing Sector	DATA	DATA	DATA	DATA	DATA	DATA
Erase Suspended & Program Erasing Sector	1	1	1	1	TOGGLE	TOGGLE
Erase Suspended & Program Non-Erasing Sector in Plane A	$\overline{I/O7}$	DATA	TOGGLE	DATA	TOGGLE	DATA
Erase Suspended & Program Non-Erasing Sector in Plane B	DATA	$\overline{I/O7}$	DATA	TOGGLE	DATA	TOGGLE

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Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	40	0.01	AT49F1604-70TC AT49F1604-70UC	48T 48U	Commercial (0°C to 70°C)
			AT49F1614-70CC AT49F1614-70TC	48C2 48T	
	40	0.01	AT49F1604-70TI AT49F1604-70UI	48T 48U	Industrial (-40°C to 85°C)
			AT49F1614-70CI AT49F1614-70TI	48C2 48T	
90	40	0.01	AT49F1604-90TC AT49F1604-90UC	48T 48U	Commercial (0°C to 70°C)
			AT49F1614-90CC AT49F1614-90TC	48C2 48T	
	40	0.01	AT49F1604-90TI AT49F1604-90UI	48T 48U	Industrial (-40°C to 85°C)
			AT49F1614-90CI AT49F1614-90TI	48C2 48T	
70	40	0.01	AT49F1604T-70TC AT49F1604T-70UC	48T 48U	Commercial (0°C to 70°C)
			AT49F1614T-70CC AT49F1614T-70TC	48C2 48T	
	40	0.01	AT49F1604T-70TI AT49F1604T-70UI	48T 48U	Industrial (-40°C to 85°C)
			AT49F1614T-70CI AT49F1614T-70TI	48C2 48T	
90	40	0.01	AT49F1604T-90TC AT49F1604T-90UC	48T 48U	Commercial (0°C to 70°C)
			AT49F1614T-90CC AT49F1614T-90TC	48C2 48T	
	40	0.01	AT49F1604T-90TI AT49F1604T-90UI	48T 48U	Industrial (-40°C to 85°C)
			AT49F1614T-90CI AT49F1614T-90TI	48C2 48T	

Package Type	
48C2	48-Ball, Plastic Chip-Size Ball Grid Array Package (CBGA)
48T	48-Lead, Thin Small Outline Package (TSOP)
48U	48-Ball, Micro Ball Grid Array Package (µBGA)

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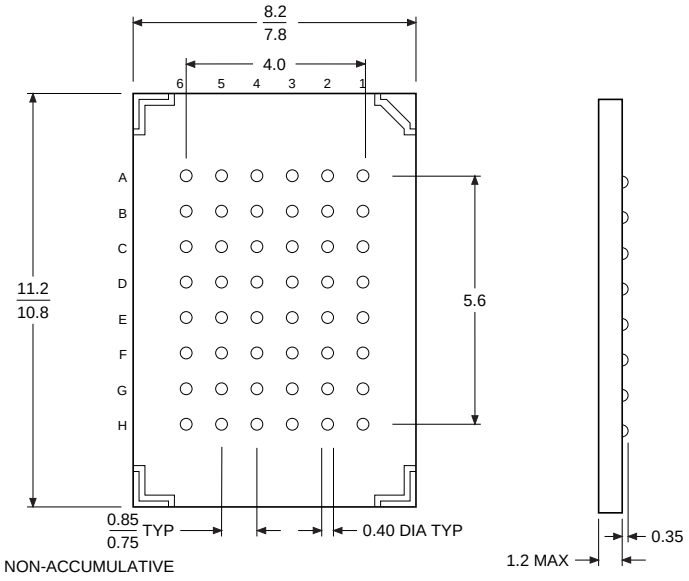
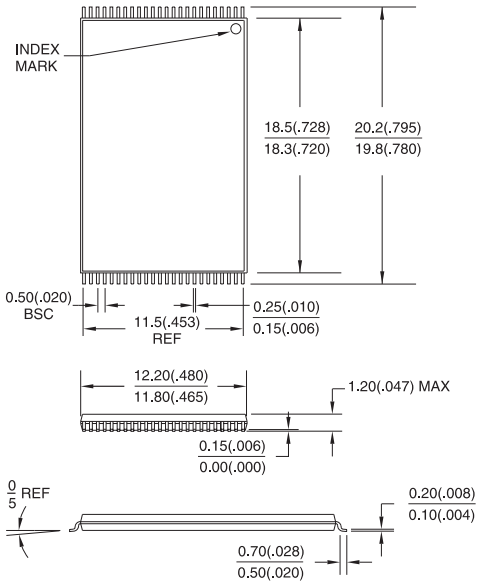
Packaging Information

48C2, 48-Ball, Plastic Chip-size Ball Grid Array Package (CBGA)



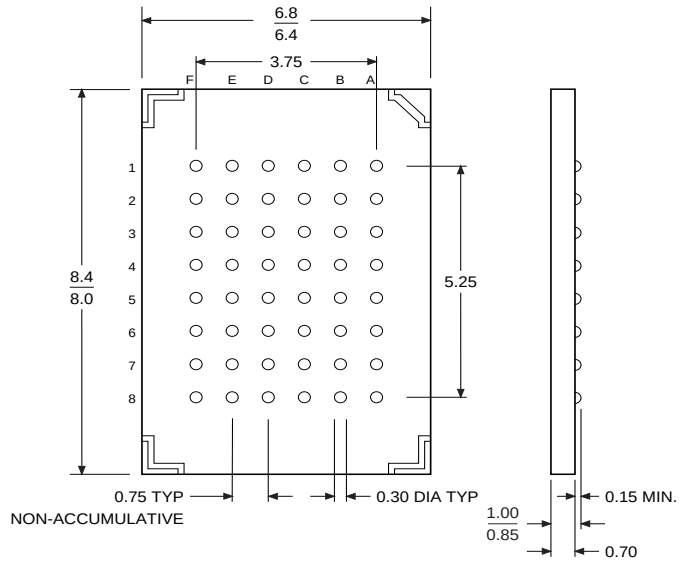
48T, 48-Lead, Plastic Thin Small Outline Package (TSOP) Dimensions in Millimeters and (Inches)*

JEDEC OUTLINE MO-142 DD



*Controlling dimension: millimeters

48U, 48-Ball, Micro Ball Grid Array Package (µBGA)



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