

Silicon Variable Capacitance Diode

Description

The 1T362A is a variable capacitance diode designed for electronic tuning of TV tuners and the super-miniature package allows the tuner miniaturization.

Features

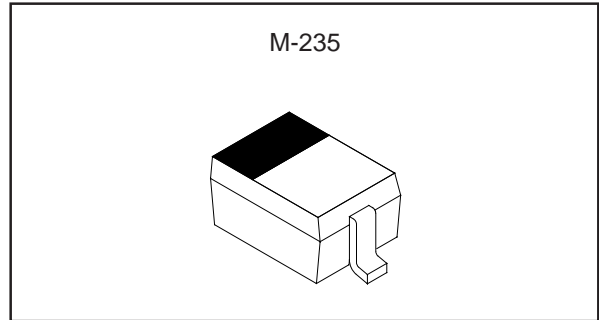
- Super miniature package
- Low series resistance 0.65 Ω Max. (f=470 MHz)
- Large capacitance ratio 6.5 Typ. (C<sub>2</sub>/C<sub>25</sub>)
- Small leakage current 10 nA Max. (V<sub>R</sub>=28 V)
- Capacitance deviation within 2 %

Applications

Electronic tuning of TV and CATV

Structure

Silicon epitaxial planar type diode



Absolute Maximum Ratings (Ta=25 °C)

- Reverse voltage V<sub>R</sub> 30 V
- Peak reverse voltage V<sub>RM</sub> 35 V (R<sub>L</sub>≥10 kΩ)
- Operating temperature Topr 85 °C
- Storage temperature Tstg -55 to +150 °C

Electrical Characteristics

(Ta=25 °C)

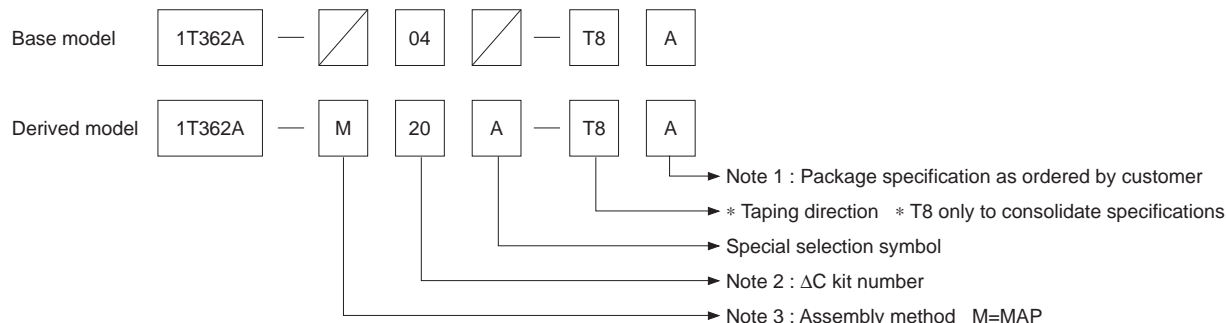
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Reverse current	I <sub>R</sub>	V <sub>R</sub> =28 V			10	nA
Diode capacitance	C <sub>2</sub>	V <sub>R</sub> =2 V, f=1 MHz	14.01	15.00	16.33	pF
	C <sub>25</sub>	V <sub>R</sub> =25 V, f=1 MHz	2.10	2.27	2.39	pF
Capacitance ratio	C <sub>2</sub> /C <sub>25</sub>	f=1 MHz		6.5		
Series resistance	r <sub>s</sub>	C <sub>D</sub> =14 pF, f=470 MHz		0.57	0.65	Ω
Capacitance deviation in a matching group	ΔC	V <sub>R</sub> =2 to 25 V, f=1 MHz			2	%

ΔC: The capacitance deviation of continuous 20 pcs of 1T362A is ranged within 2% in any place of the taping package.

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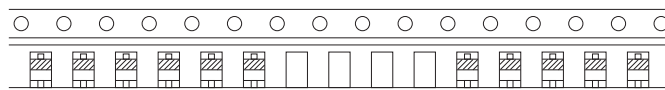
**Product Name and Package Specification for the 1T362A.**

According to the classification number for the combination of capacitance deviations (hereafter ΔC), assembly method and automatic mounting equipment section, the following product names are assigned.



**Note1)** In taping packaging of products groups according to the ΔC classification, products must be divided according to the group. If taping is performed without grouping into categories, products from two different groups may be mounted on the same tuner, so that ΔC cannot be assured during tuning, making tuning defective.

A: Panasert method; Sections are divided by four blank spaces on the carrier tape.



B: Sanyo method; Black tape is affixed to one blank space on the carrier tape to mark sections.



**Note 2) ΔC kit number**

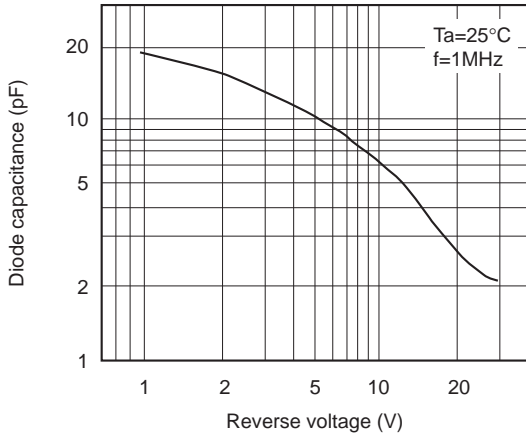
When taping each group, taping is performed in kit number multiples.

- 01; Incomplete kit (ΔC not guaranteed)
- 04; 4 kits
- 20; 20 kits
- Recommended kit number; 4 and 20

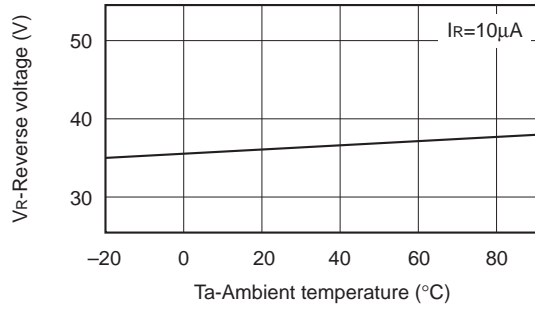
Other) Minimum number of kits per group is 240 (60 or more at the beginning of the carrier tape). Up to nine sections on one reel.

**Note 3)** "MAP" is the method where the neighboring chips are assembled continuously in order to enhance the concentration of the capacitance deviation in a matching group.

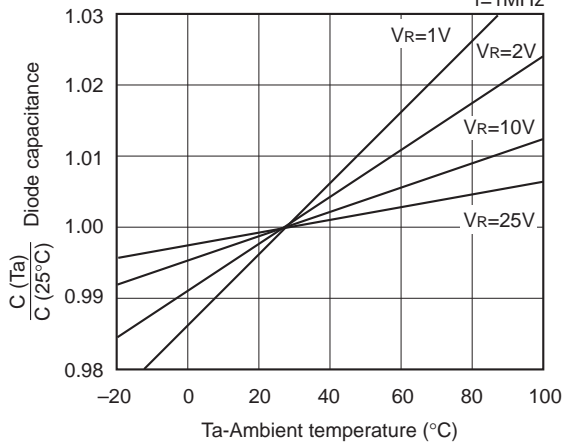
Diode capacitance vs. Reverse voltage



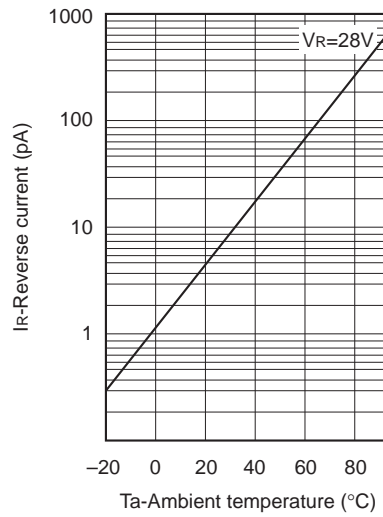
Reverse voltage vs. Ambient temperature



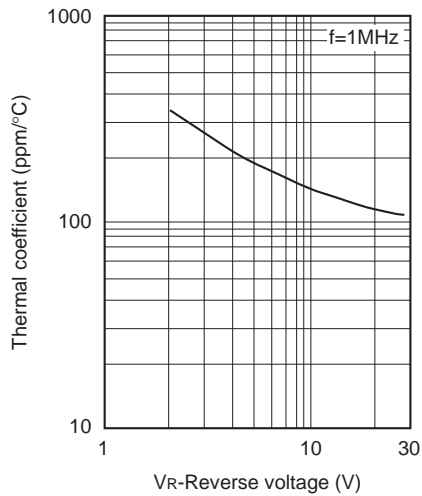
Diode capacitance vs. Ambient temperature  
f=1MHz



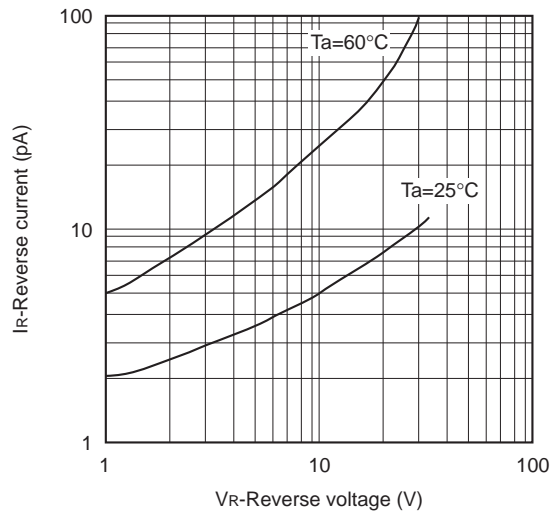
Reverse current vs. Ambient temperature



Thermal coefficient of diode capacitance

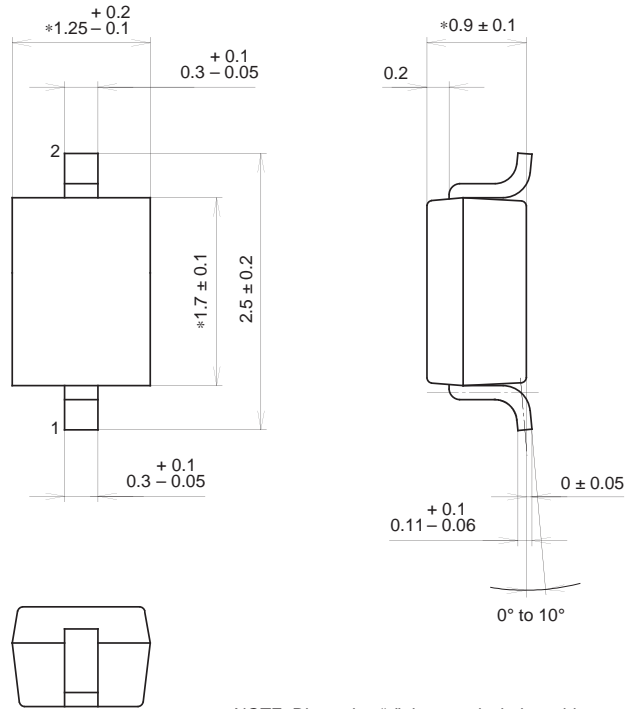


Reverse current vs. Reverse voltage



Package Outline Unit : mm

M-235

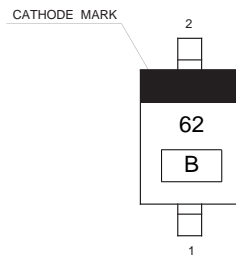


NOTE: Dimension "\*" does not include mold protrusion.

SONY CODE	M-235
EIAJ CODE	—
JEDEC CODE	—

PACKAGE WEIGHT	0.1g
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Marking



Notes

- 1) B:Lot No.(Year and Month of manufacture)  
Year;Last one digit  
Month;A,B,C(for Oct. to Dec.)  
1 to 9(for Jan.to Sept.)