The Wideband IC Line

RF LDMOS Wideband Integrated Power Amplifiers

The MW4IC2020M wideband integrated circuit is designed for base station applications. It uses Motorola's newest High Voltage (26 to 28 Volts) LDMOS IC technology and integrates a multi-stage structure. Its wideband On-Chip design makes it usable from 1600 to 2400 MHz. The linearity performances cover all modulations for cellular applications: GSM, GSM EDGE, TDMA, CDMA and W-CDMA.

Final Application

Typical Two-Tone Performance: V_{DD} = 26 Volts, I_{DQ1} = 80 mA, I_{DQ2} = 200 mA, I_{DQ3} = 300 mA, P_{out} = 20 Watts PEP, Full Frequency Band Power Gain — 29 dB IMD — -32 dBc

Drain Efficiency — 26% (at 1805 MHz) and 20% (at 1990 MHz)

Driver Applications

Typical GSM EDGE Performance: $V_{DD} = 26$ Volts, $I_{DQ1} = 80$ mA, $I_{DQ2} = 230$ mA, $I_{DQ3} = 230$ mA, $P_{out} = 5$ Watts Avg., Full Frequency Band Power Gain — 29 dB Spectral Regrowth @ 400 kHz Offset = -66 dBc Spectral Regrowth @ 600 kHz Offset = -77 dBc EVM — 1% rms

Typical CDMA Performance: V_{DD} = 26 Volts, I_{DQ1} = 80 mA, I_{DQ2} = 240 mA, I_{DQ3} = 250 mA, P_{out} = 1 Watt Avg., Full Frequency Band, IS-97 Pilot, Sync, Paging, Traffic Codes 8 through 13

Power Gain - 30 dB

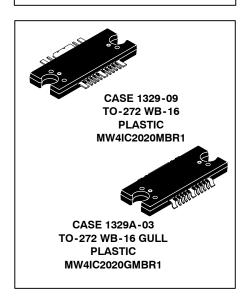
ACPR @ 885 kHz Offset = -61 dBc @ 30 kHz Bandwidth ALT1 @ 1.25 MHz Offset = -69 dBc @ 12.5 kHz Bandwidth ALT2 @ 2.25 MHz Offset = -59 dBc @ 1 MHz Bandwidth

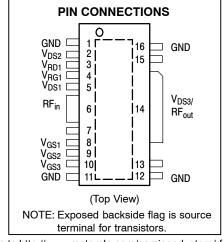
- Capable of Handling 3:1 VSWR, @ 26 Vdc, 1990 MHz, 8 Watts CW Output Power
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- On-Chip Matching (50 Ohm Input, DC Blocked, >5 Ohm Output)
- Integrated Temperature Compensation with Enable/Disable Function
- On-Chip Current Mirror g_m Reference FET for Self Biasing Application (1)
- Integrated ESD Protection
- Also Available in Gull Wing for Surface Mount
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel

V_{RG1} V_{DS2} V_{DS1} RF_{in} V_{DS3}/RF_{out} V_{DS3}/RF_{out} V_{GS1} V_{GS2} V_{GS3} V_{GS2} V_{GS3} Functional Block Diagram

MW4IC2020MBR1 MW4IC2020GMBR1

1805-1990 MHz, 20 W, 26 V GSM/GSM EDGE, CDMA RF LDMOS WIDEBAND INTEGRATED POWER AMPLIFIERS





(1) Refer to AN1987/D, Quiescent Current Control for the RF Integrated Circuit Device Family. Go to https://www.motorola.com/semiconductors/rf. Select Documentation/Application Notes - AN1987.

REV 4





MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	65	Vdc
Gate-Source Voltage	V _{GS}	-0.5, +15	Vdc
Storage Temperature Range	T _{stg}	-65 to +175	°C
Operating Junction Temperature	TJ	175	°C
Input Power	P _{in}	20	dBm

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value (1)	Unit
Thermal Resistance, Junction to Case	$R_{ heta JC}$		°C/W
Stage 1		10.5	
Stage 2		5.1	
Stage 3		2.3	

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)
Charge Device Model	C5 (Minimum)

MOISTURE SENSITIVITY LEVEL

Test Methodology	Rating
Per JESD 22-A113	3

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Тур	Max	Unit
_	•		•		

FUNCTIONAL TESTS (In Motorola Wideband 1805-1990 MHz Test Fixture, 50 ohm system) V_{DD} = 26 Vdc, I_{DQ1} = 80 mA, I_{DQ2} = 200 mA, I_{DQ3} = 300 mA, P_{out} = 20 W PEP, f1 = 1990 MHz, f2 = 1990.1 MHz and f1 = 1805 MHz, f2 = 1805.1 MHz, Two-Tone CW

Power Gain		G _{ps}	27	29	_	dB
Drain Efficiency	f1 = 1805 MHz, f2 = 1805.1 MHz f1 = 1990 MHz, f2 = 1990.1 MHz	η _D	24 18	26 20	_	%
Input Return Loss		IRL	_	_	-10	dB
Intermodulation Distortion		IMD	_	-32	-27	dBc
Stability (100 mW <p<sub>out<8 W CW, Lo</p<sub>	oad VSWR = 3:1, All Phase Angles)		No Spurious > -60 dBc			

TYPICAL PERFORMANCES (In Motorola Test Fixture, 50 ohm system) V_{DD} = 26 Vdc, I_{DQ1} = 80 mA, I_{DQ2} = 200 mA, I_{DQ3} = 300 mA, 1805 MHz<Frequency<1990 MHz, 1-Tone

Saturated Pulsed Output Power (f = 1 kHz, Duty Cycle 10%)	P _{sat}	_	33	_	Watts
Quiescent Current Accuracy over Temperature (-10 to 85°C)		_	±5	_	%
Gain Flatness in 30 MHz Bandwidth @ Pout = 1 W CW	G _F	_	0.15	_	dB
Deviation from Linear Phase in 30 MHz Bandwidth @ P _{out} = 1 W CW 1805-1880 MHz 1930-1990 MHz	Φ	_	±0.5 ±0.2	_	٥
Delay @ P _{out} = 1 W CW Including Output Matching	Delay	_	1.8	=	ns
Part to Part Phase Variation @ Pout = 1 W CW	ΦΔ	_	±10	_	0

⁽¹⁾ MTTF calculator available at http://www.motorola.com/semiconductors/rf. Select Tools/Software/Application Software/Calculators to access the MTTF calculators by product.

(continued)

ELECTRICAL CHARACTERISTICS — **continued** (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Тур	Max	Unit
TYPICAL CDMA PERFORMANCES (In Modified CDMA Test Fixture, 50 oh		nn = 26 Vdc	DO1 = 80 mA	Ipon = 240 r	mA Inos =

250 mA, Pout = 1 W Avg., I1930 MHz<Frequency<1990 MHz, 1-Tone, 9 Channel Forward Model (Pilot, Paging, Sync, Traffic Codes 8 through 13). Peak/Avg. Ratio 9.8 dB @ 0.01% Probability on CCDF.

Power Gain	G _{ps}	_	30	_	dB
Drain Efficiency		_	5	_	%
Adjacent Channel Power Ratio (±885 kHz @ 30 kHz Bandwidth)	ACPR	_	-61	_	dBc
Alternate 1 Channel Power Ratio (±1.25 MHz @ 12.5 kHz Bandwidth)	ALT1	_	-69	_	dBc
Alternate 2 Channel Power Ratio (±2.25 MHz @ 1 MHz Bandwidth)	ALT2	_	-59	=	dBc

TYPICAL GSM EDGE PERFORMANCES (In Modified GSM EDGE Test Fixture, 50 ohm system) $V_{DD} = 26 \text{ Vdc}$, $I_{DQ1} = 80 \text{ mA}$, $I_{DQ2} = 230$ mA, $I_{DQ3} = 230$ mA, $P_{out} = 5$ W Avg., 1805 MHz<Frequency<1990 MHz

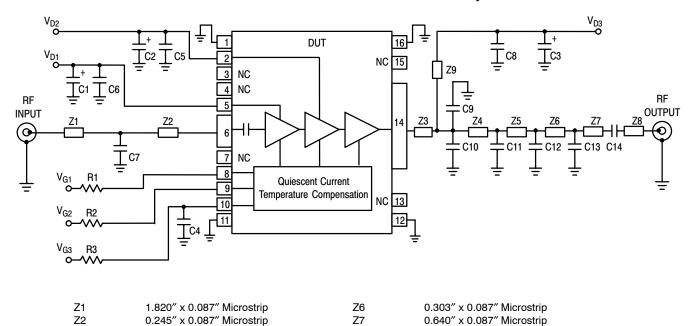
Power Gain	G _{ps}	_	29	_	dB
Drain Efficiency	η_{D}	_	15	_	%
Error Vector Magnitude	EVM	_	1	_	% rms
Spectral Regrowth at 400 kHz Offset	SR1	_	-66	_	dBc
Spectral Regrowth at 600 kHz Offset	SR2	_	-77	_	dBc

Z3

Ζ4

Z5

Freescale Semiconductor, Inc.



0.334" x 0.087" Microstrip 0.345" x 0.236" Microstrip 0.327" x 0.087" Microstrip Z9 1.231" x 0.043" Microstrip PCB 0.271" x 0.087" Microstrip Taconic TLX8-0300, 0.030", $\varepsilon_r = 2.55$

Z8

Figure 1. MW4IC2020MBR1(GMBR1) Test Circuit Schematic

Table 1. MW4IC2020MBR1(GMBR1) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C3	10 μF, 35 V Tantalum Capacitors	TAJE226M035	AVX
C4	220 nF Chip Capacitor (1206)	12065C224K28	AVX
C5, C6, C8	6.8 pF 100B Chip Capacitors	100B6R8CW	ATC
C7	0.5 pF 100B Chip Capacitor	100B0R5BW	ATC
C9, C11	1.8 pF 100B Chip Capacitors	100B1R8BW	ATC
C10	2.2 pF 100B Chip Capacitor	100B2R2BW	ATC
C12	1 pF 100B Chip Capacitor	100B1R0BW	ATC
C13	0.3 pF 100B Chip Capacitor	100B0R3BW	ATC
C14	10 pF 100B Chip Capacitor	100B100GW	ATC
R1, R2, R3	1.8 kΩ Chip Resistors (1206)		

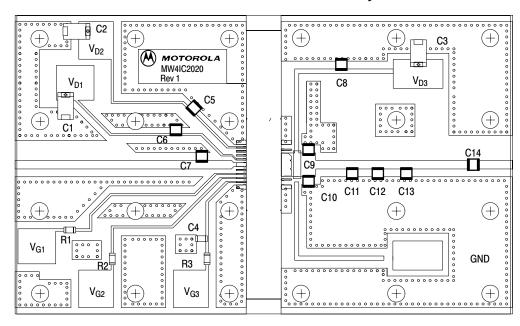


Figure 2. MW4IC2020MBR1(GMBR1) Test Circuit Component Layout

TYPICAL CHARACTERISTICS

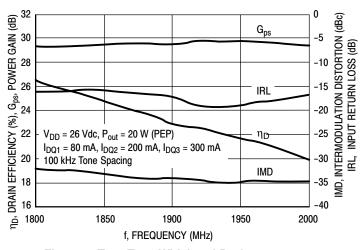


Figure 3. Two-Tone Wideband Performance

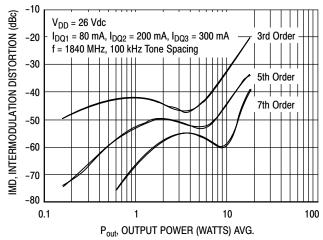


Figure 4. Intermodulation Distortion Products versus Output Power

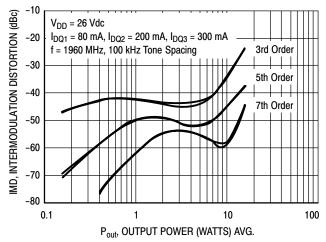


Figure 5. Intermodulation Distortion Products versus Output Power

-30°C

85°C

18

DRAIN EFFICIENCY

JD,

3

0

10

25°C

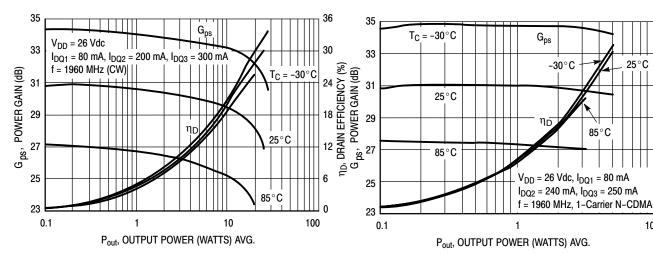


Figure 6. Power Gain and Drain Efficiency versus Output Power

Figure 7. Power Gain and Drain Efficiency versus Output Power

TYPICAL CHARACTERISTICS

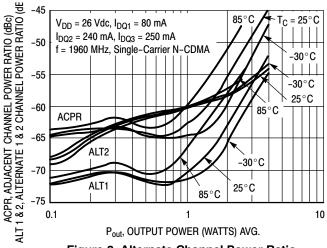


Figure 8. Alternate Channel Power Ratio, Alternate 1 and 2 Channel Power Ratio versus Output Power

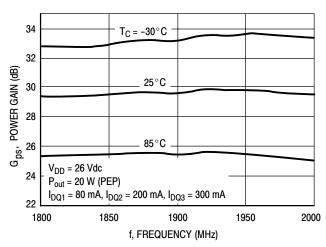


Figure 9. Power Gain versus Frequency

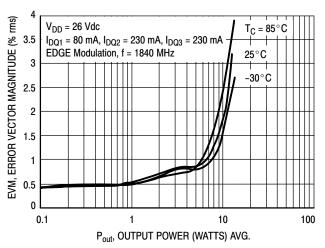


Figure 10. Error Vector Magnitude versus **Output Power**

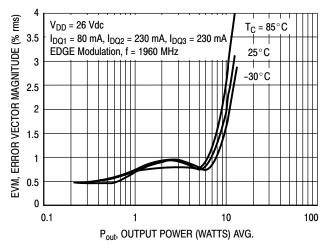


Figure 11. Error Vector Magnitude versus **Output Power**

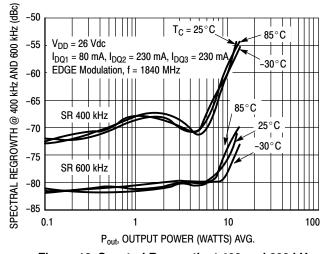


Figure 12. Spectral Regrowth at 400 and 600 kHz versus Output Power

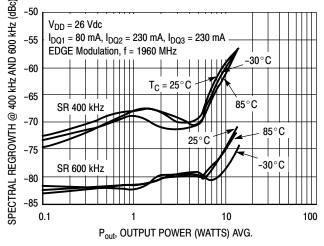
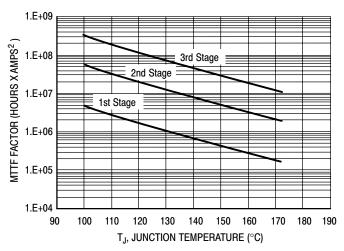


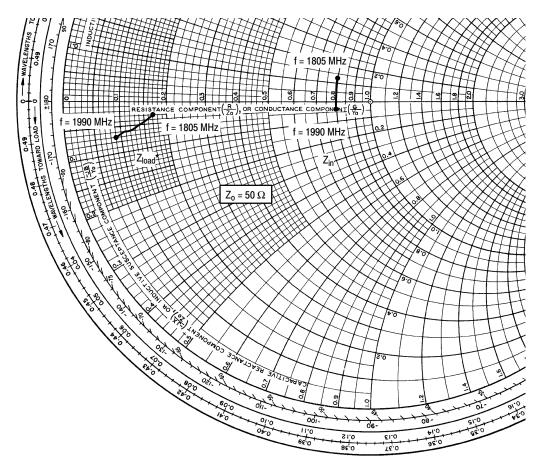
Figure 13. Spectral Regrowth at 400 and 600 kHz versus Output Power

TYPICAL CHARACTERISTICS



This above graph displays calculated MTTF in hours x ampere 2 drain current. Life tests at elevated temperatures have correlated to better than $\pm 10\%$ of the theoretical prediction for metal failure. Divide MTTF factor by $l_D{}^2$ for MTTF in a particular application.

Figure 14. MTTF Factor versus Junction Temperature



 $\rm V_{DD} = 26~V, \, I_{DQ1} = 80~mA, \, I_{DQ2} = 200~mA, \, I_{DQ1} = 300~mA, \, P_{out} = 20~W~PEP~Two-Tone~CW$

f MHz	$\mathbf{Z_{in}}_{\Omega}$	$\mathbf{Z_{load}}_{\Omega}$
1805	40.00 + j6.50	8.75 - j1.42
1842	40.00 + j2.00	7.00 - j2.70
1880	40.00 - j1.50	5.90 - j2.97
1930	40.00 - j1.80	5.46 - j3.20
1960	40.00 - j2.10	4.30 - j3.35
1990	40.00 - j2.60	4.45 - j3.30

 Z_{in} Device input impedance as measured from gate to ground.

Test circuit impedance as measured Z_{load} = from drain to ground.

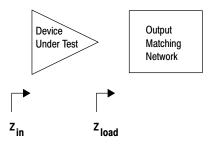
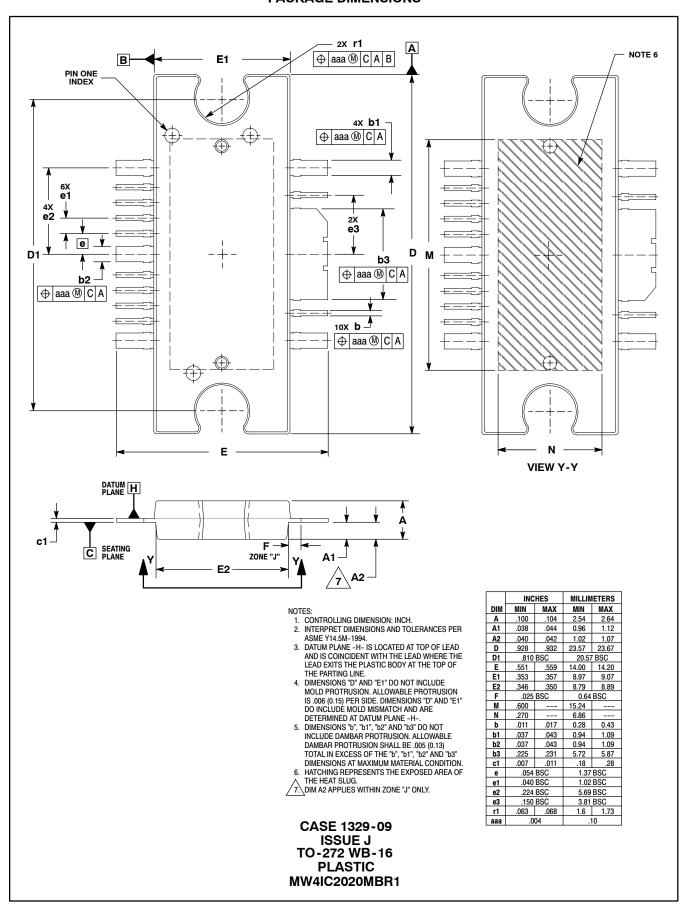
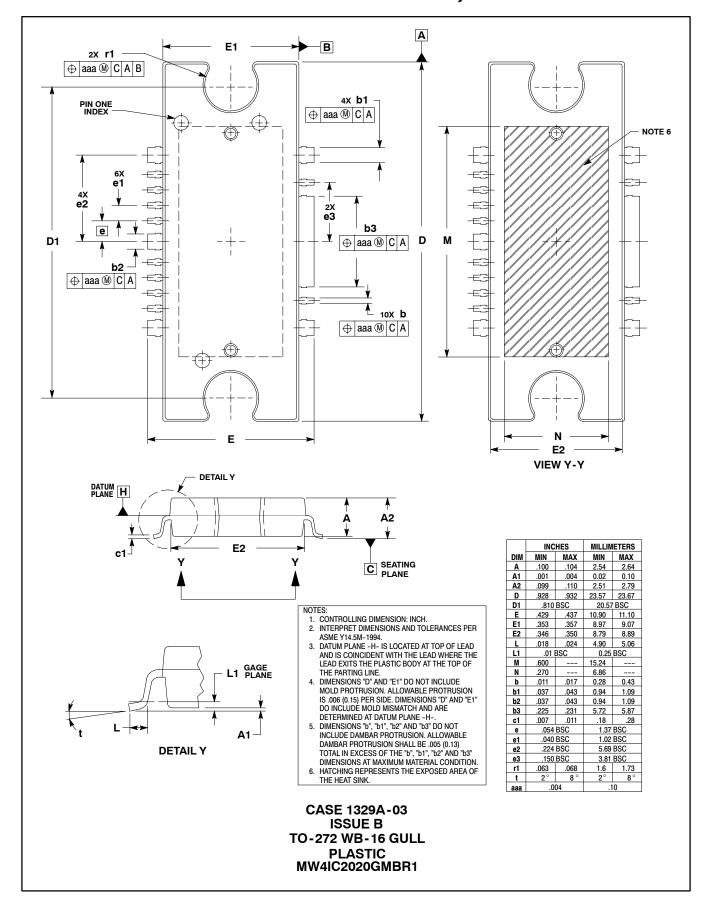


Figure 15. Series Equivalent Output Impedance

PACKAGE DIMENSIONS





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