5-V Voltage Regulator

TLE 4287 G

Features

- Output voltage tolerance ≤ ± 2%
- Very low standby current consumption
- Input voltage up to 42 V
- Reset function down to 1 V output voltage
- ESD protection up to 2000 V
- Adjustable reset time
- On/Off logic
- Overtemperature protection
- Reverse polarity protection
- Short-circuit proof
- Very wide temperature range
- Very small output capacitor

P-DSO-14-8

Type	Ordering Code	Package
▼ TLE 4287 G	Q67006-A9286	P-DSO-14-8 (SMD)

▼ New type

Functional Description

The **TLE 4287 G** is a monolithic integrated 5 V voltage regulator in **P-DSO-14-8** package. It supplies an output current I_Q > 250 mA. The IC is short circuit proof and incorporates temperature protection which turns off the device at overtemperature.

The input voltage V_I is regulated in the range of 7.5 V < V_I < 40 V to $V_{Q,nom}$ = 5 V. Therefore a reference voltage, which is kept highly accurate by resistance adjustment, is compared via a control amplifier to a voltage that is proportional to the output voltage. The control amplifier drives the base of the series transistor by a buffer.

A comparator in the reset-generator block compares a reference voltage that is independent of the input voltage to the scaled-down output voltage. In the case of an output voltage V_Q < 4.5 V the reset delay capacitor is discharged and a reset signal is generated by setting the reset output LOW. The reset delay time can be set by choosing the external capacitor over a wide range. When the output voltage rises above V_Q ≥ 4.5 V the reset delay capacitor is charged again. As soon as the delay capacitor voltage reaches the upper switching threshold the reset output pin is set HIGH again.

The device has two logic inputs, *EN* and *H*. It is turned ON by a voltage > 4 V at *EN*, for example by the ignition and remains active in case *H* is set LOW, even if the voltage at *EN* goes LOW. This makes it possible to implement a self-holding circuit without external components. When the device is turned OFF, the output voltage drops to 0 V and current consumption tends towards 0 µA. (Please see following truth table).

Design Notes for External Components

The input capacitor C_I is necessary for compensation line influences. The resonant circuit consisting of lead inductance and input capacitance can be damped by a resistor of approx. 1 Ω in series with C_I. The output capacitor is necessary for the stability of the regulating circuit. Stability is guaranteed for $C_Q \geq 100$ nF within the operating temperature range.

State Table for Turn-On/Turn-Off Logic

Nr.	Enable *EN*	Hold *H*	V_Q	Remarks
1	L	X	0 V	Initial state
2	H	X	5 V	Regulator switched on via pin 6, by ignition for example
3	H	L	5 V	Pin 9 clamped active to GND by controller while pin 6 is still HIGH
4	X	L	5 V	Previous state remains, even ignition is shut off: self-holding state
5	L	L	5 V	Ignition shut off while regulator is in self-holding state
6	L	H	0 V	Regulator shut down by releasing of pin 9 while pin 6 remains LOW, final state. No active clamping required by external self-holding circuit (µC) to keep regulator shut off

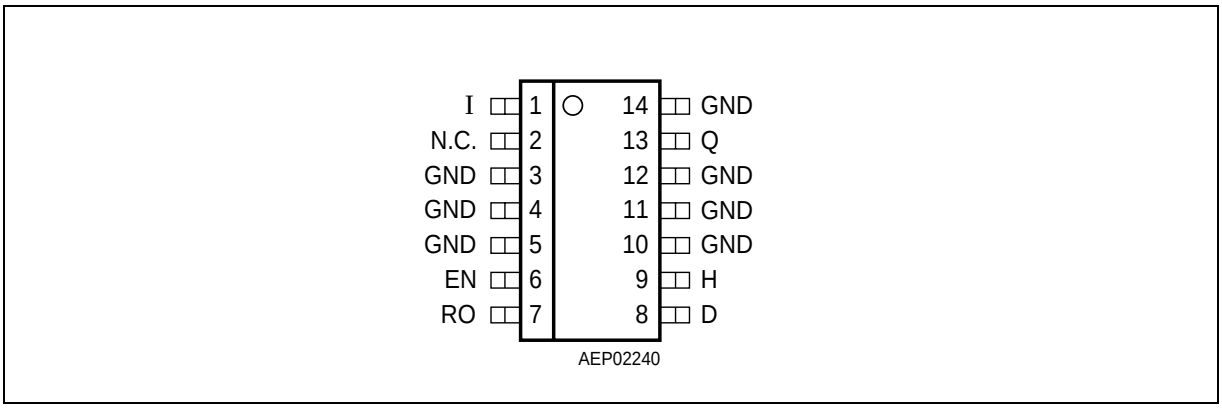


Figure 1 Pin Configuration (top view)

Pin Definitions and Functions

Pin No.	Symbol	Function
1	I	**Input**; block to ground directly at the IC by a ceramic capacitor
2	N.C.	Not connected
3, 4, 5, 10, 11, 12, 14	GND	**Ground**
6	EN	**Enable**; active high, device is turned ON by HIGH signal at this pin, internally connected to GND via pull-down resistor of 100 kΩ
7	RO	**Reset Output**; open-collector output, internally connected to Q via a pull-up resistor of 30 kΩ
8	D	**Reset Delay**; connect to GND via external delay capacitor for setting delay time
9	H	**Hold** and release; active low, see truth table above for function, connected to Q via a pull-up resistor of 50 kΩ
13	Q	**Output**; block to GND with a capacitor $C_Q \geq 100$ nF

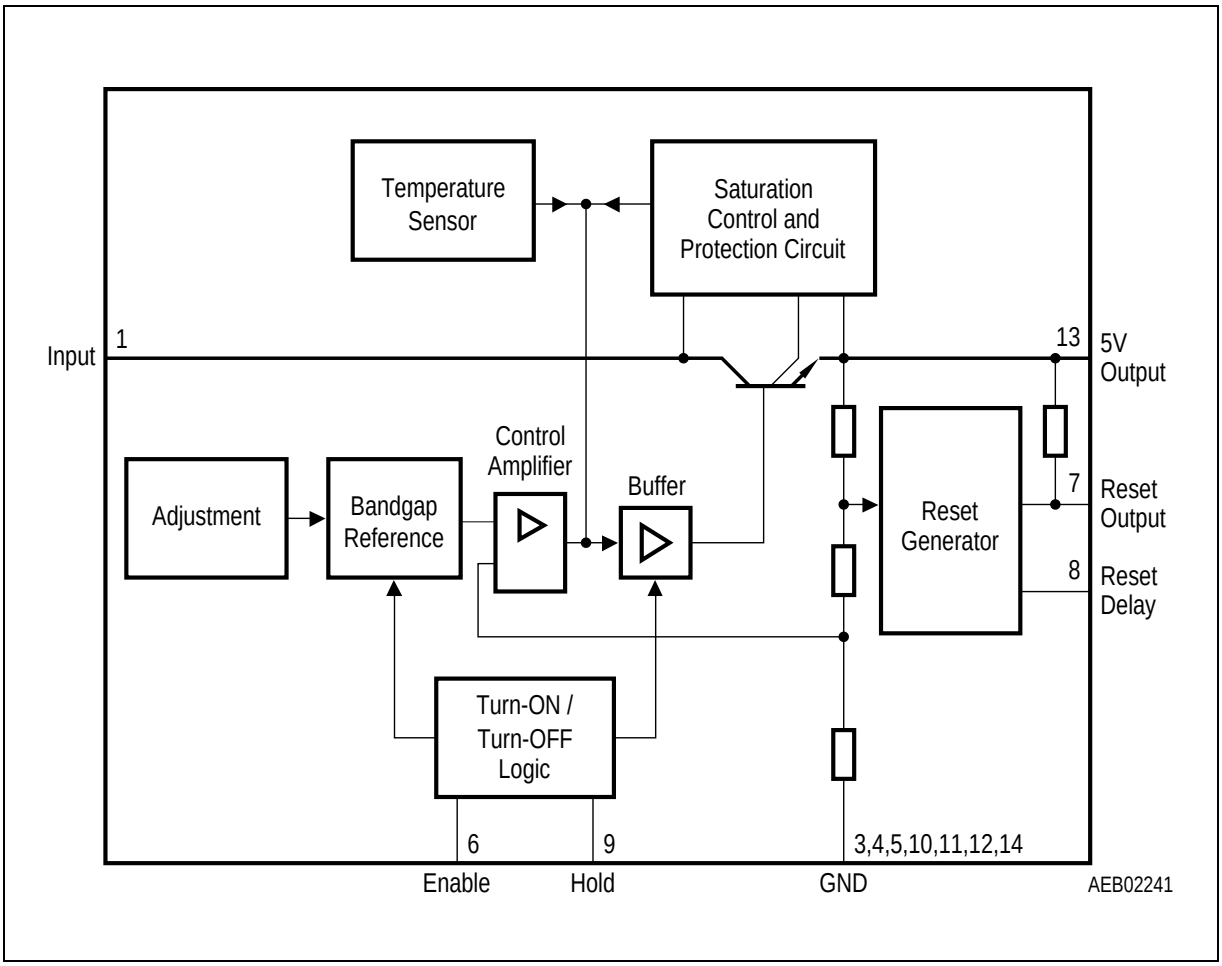


Figure 2 Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Input I					
Voltage	V_I	– 0.5	42	V	–
Current	I_I	–	–	mA	internally limited
Output Q					
Voltage	V_Q	– 0.3	7	V	–
Current	I_Q	–	–	–	internally limited
Reset Output RO					
Voltage	V_R	– 0.3	7	V	–
Current	I_R	–	–	–	internally limited
Reset Delay D					
Voltage	V_D	– 0.3	42	V	–
Current	I_D	–	–	–	–
Enable EN					
Voltage	V_{EN}	– 42	42	V	–
Current	I_{EN}	– 5	5	mA	$t \leq 400$ ms
Hold H					
Voltage	V_H	– 2	7	V	–
Current	I_H	–	–	–	internally limited

Absolute Maximum Ratings (cont'd)

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Ground GND					
Current	I_{GND}	– 0.5	–	A	–
Temperatures					
Junction temperature	T_j	– 40	165	°C	–
Junction temperature	T_j	– 40	175	°C	max. 15 min
Storage temperature	T_{stg}	– 50	150	°C	–

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Input voltage	V_I	7.5	42	V	–
Junction temperature	T_j	– 40	165	°C	–

Thermal Resistances

Junction pin	$R_{thj\text{-}pin}$	–	32	K/W	measured to pin 4
Junction ambient	$R_{thj\text{-}a}$	–	112	K/W	1)

1) Package mounted on PCB 80 × 80 × 1.5 mm³; 35µ Cu; 5µ Sn; Footprint only; zero airflow.

Note: ESD-Protection according to MIL Std. 883: 2 kV.

Electrical Characteristics

7.5 V ≤ V_I ≤ 40 V; – 40 °C < T_j < 150 °C; V_{EN} > 4 V (unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output voltage	V_Q	4.90	5.0	5.10	V	5 mA < I_Q < 200 mA 7.5 V < V_I < 22 V
Output voltage	V_Q	4.90	5.0	5.10	V	5 mA < I_Q < 80 mA 7.5 V < V_I < 36 V
Output current limitation	I_Q	250	–	–	mA	V_I < 22 V
Drop voltage	V_{DR}	–	1.8	2.5	V	I_Q = 200 mA[1)]
Current consumption $I_q = I_I - I_Q$	I_q	–	–	50	µA	Regulator OFF: V_{EN} = 0 V, H = open
Current consumption $I_q = I_I - I_Q$	I_q	–	1.0	10	µA	T_j = 25 °C, V_{EN} = 0 V, H = open
Current consumption $I_q = I_I - I_Q$	I_q	–	2.3	5	mA	5 mA < I_Q <200 mA, V_I = 16 V
Load regulation	$\Delta V_{Q.lo}$	– 25	–	+ 25	mV	5 mA < I_Q < 200 mA
Line regulation	$\Delta V_{Q,li}$	– 25	–	+ 25	V	7.5 V < V_I < 22 V I_Q = 20 mA
Power-Supply-Ripple-Rejection	PSRR	–	55	–	dB	f_r = 100 Hz; V_r = 0.5 V_{SS}
Temperature output voltage drift	$\Delta V_Q / \Delta T$	–	0.5	–	mV/K	–
Output capacitance	C_Q	100	–	–	nF	–

Reset Generator

Reset switching threshold	$V_{Q,rt}$	4.50	4.65	4.80	V	–
Reset output low voltage	V_{RL}	–	0.1	0.4	V	R_{ext} = 4.7 kΩ to V_Q[2)]
Reset output high voltage	V_{RH}	4.5	–	5.05	V	R_{ext} = ∞
Reset pull up resistor	R_R	20	30	40	kΩ	internally connected to Q
Reset charging current	$I_{D,c}$	10	15	38	µA	V_D = 1.5 V
Upper timing threshold	V_{DU}	2.2	3	3.6	V	–
Lower timing threshold	V_{DL}	0.1	0.43	0.8	V	–

Electrical Characteristics (cont'd)

7.5 V ≤ V_I ≤ 40 V; – 40 °C < T_j < 150 °C; V_{EN} > 4 V (unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Delay saturation voltage	$V_{D,sat}$	–	50	–	mV	$V_Q < V_{Q,rt}$
Reset delay time	t_{rd}	7.5	20	30	ms	C_D = 100 nF
Reset reaction time	t_{rr}	0.5	2.0	4.0	µs	C_D = 100 nF
Enable *EN*, Hold *H*						
Enable turn-ON voltage	V_{EN}	2.3	3.0	4.0	V	IC turned-ON
Enable turn-OFF voltage	V_{EN}	2.0	2.5	3.5	V	IC turned-OFF
Enable pull-down resistor	R_{EN}	50	100	200	kΩ	internally connected to GND
Enable hysteresis	ΔV_{EN}	0.2	0.4	0.8	V	–
Enable input current	I_{EN}	–	35	100	µA	V_{EN} = 4 V
Hold keep on voltage	V_H	30	35	50	%	referred to V_Q; V_Q > 4.5 V
Hold release voltage	V_H	60	70	80	%	referred to V_Q; V_Q > 4.5 V
Hold pull-up resistor	R_H	20	50	100	kΩ	internally connected to Q

1) Measured when the output voltage V_Q has dropped 100 mV from the nominal value.
2) The reset output is LOW between V_Q = 1 V and V_{rt}.

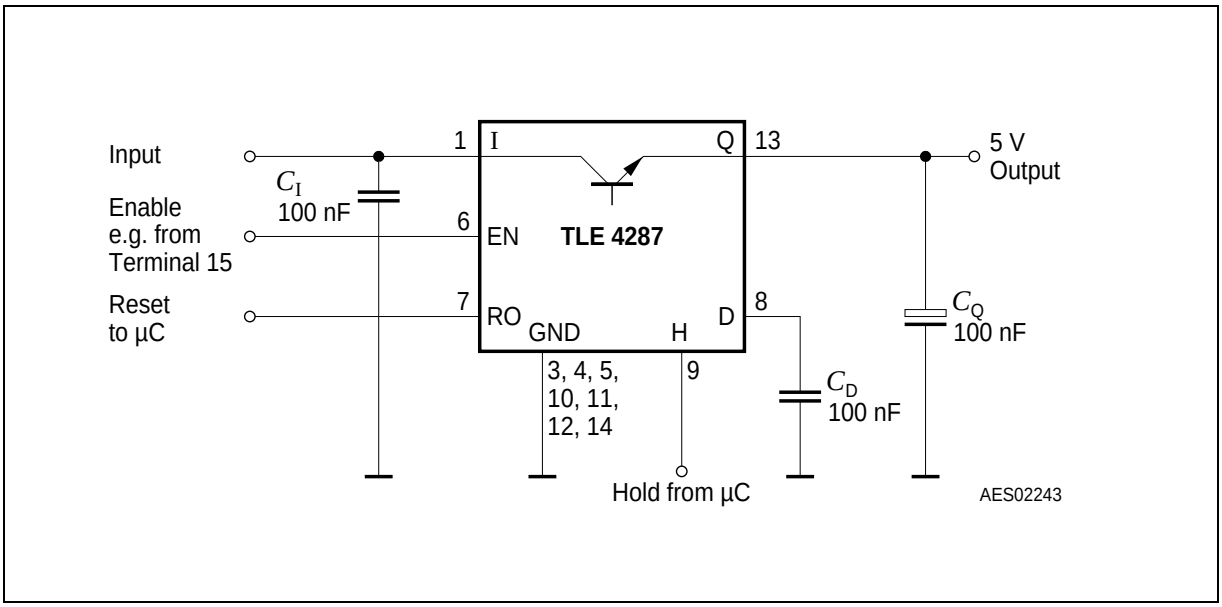


Figure 3 Application Circuit

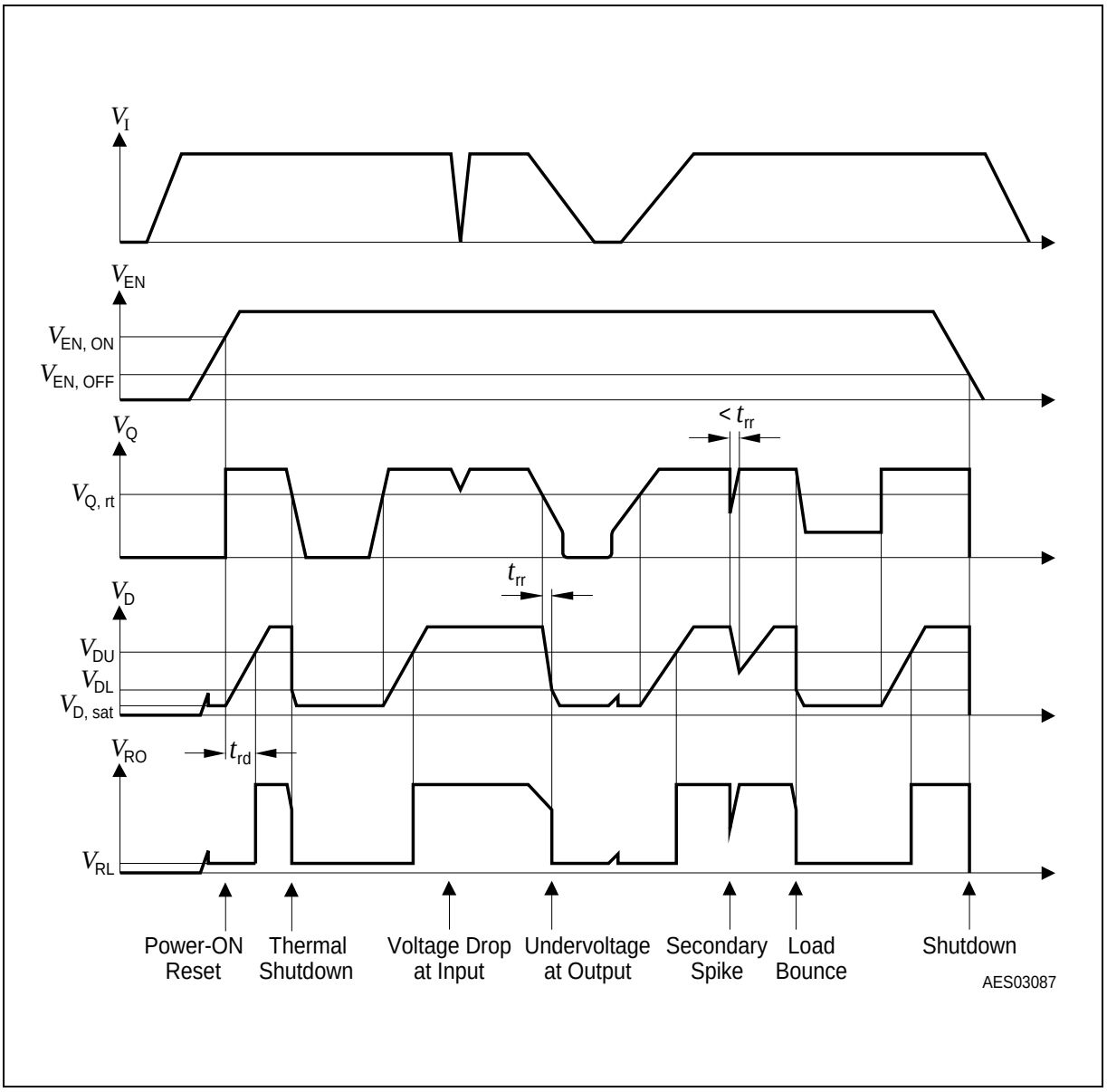
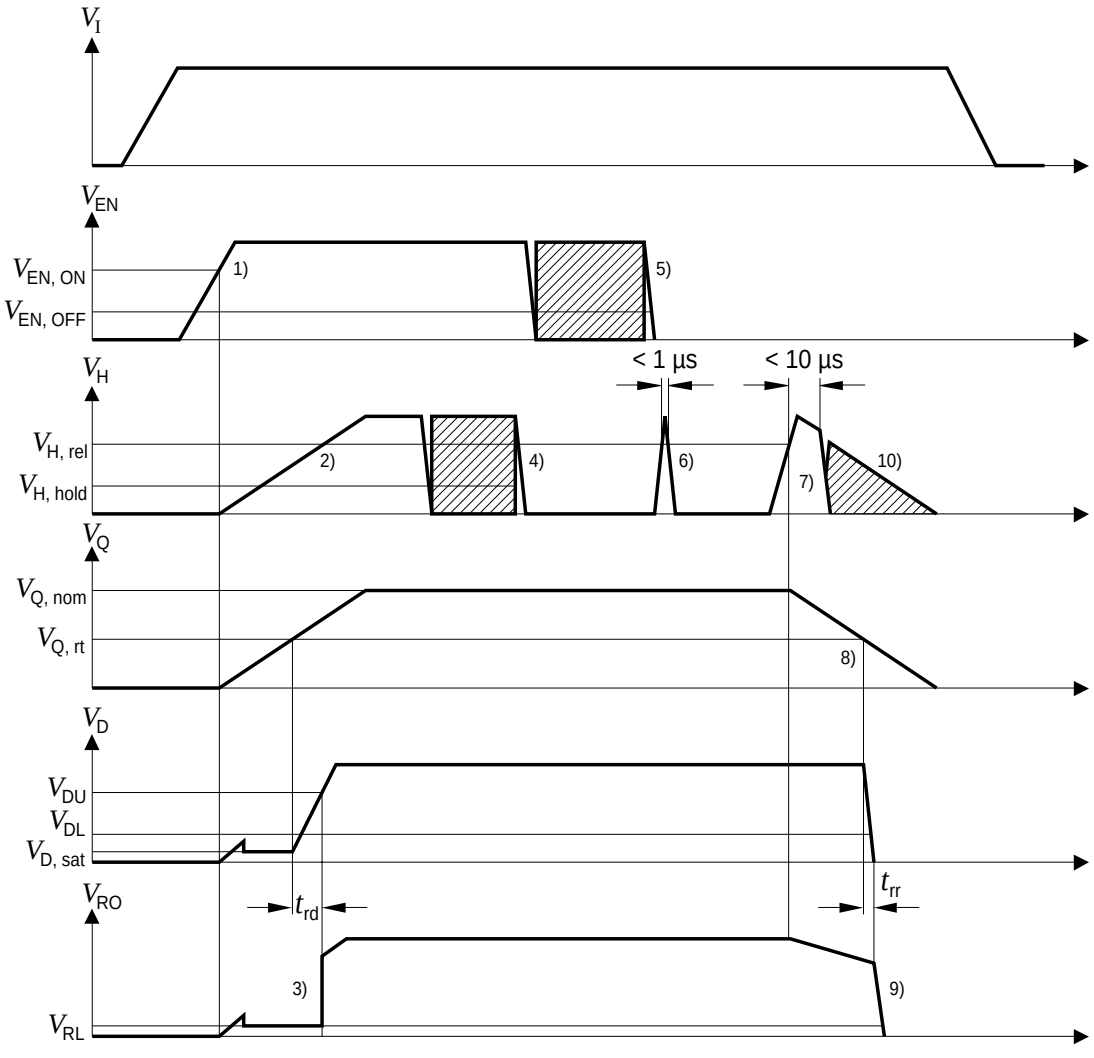


Figure 4 Time Response



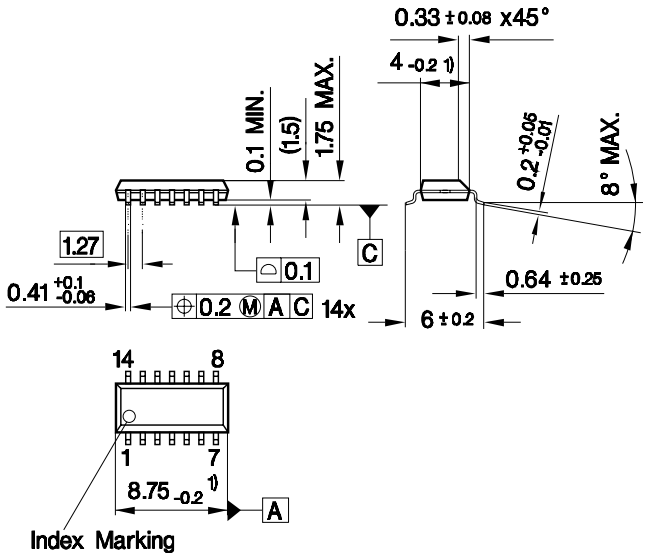
1) Enable active
2) Hold inactive, pulled up by V_Q
3) Power-ON Reset
4) Hold active, clamped to GND by external MC
5) Enable inactive, clamped by int, pull-down resistor
6) Pulse width smaller than 1 µs
7) Hold inactive, released by MC
8) Voltage Controller shutdown
9) Output-low reset
10) No switch on via V_{E6} possible after E6 was released to $V_{E6} > V_{E6, rel}$ for more than 4 µs

AES03088

Figure 5 Enable and Hold Behavior

Package Outlines

P-DSO-14-8
(Plastic Dual Small Outline)



1) Does not include plastic or metal protrusion of 0.15 max. per side

GPS05093

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

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