SIEMENS

TV Stereo Tone Control IC with Quasi-Stereo Section, Channel 1/2 Switch, SCART Input, and I²C Bus Control

TDA 6200

Preliminary Data

Bipolar IC

Features

- Treble, bass, balance, and volume control by means of an integrated digital-to-analog converter
- Quasi-stereo circuit during mono operation
- Stereo basewidth expansion during stereo operation
- Physiological volume control
- Channel 1/2 switch-over during dual audio transmission
- SCART connection
- Control of all functions via the I²C bus and the bidirectional 4 level line of the TDA 6600-2 (stereo demodulator IC)
- LED driver
- Volume control range 80 dB
- Treble, bass control ± 12 dB
- Channel separation min. 60 dB, cross-talk rejection min. 60 dB
- Parasitic voltage spacing up to 78 dB

Type	Ordering Code	Package
TDA 6200	Q67000-A2461	P-DIP-28

The TDA 6200 is comprised of a SCART switch-over, channel 1/2 switch-over, quasi-stereo circuit, stereo basewidth expansion, physiological volume control, a treble, bass, and volume control of the injected AF signals as well as an LED driver. The IC is controlled by means of an I²C bus serial interface as well as by the bidirectional 4 level line from the TDA 6600-2. The component is used for AF sound signal processing in stereo TV sets.

Circuit Description

The monolithically integrated circuit is comprised of three sections:

1. AF input analog switch for SCART and channel 1/2 switch-over
2. Sound and volume control with quasi-stereo, physiology and stereo basewidth expansion section
3. Control section including the I^2C bus, 4 level line and digital-to-analog converter

1. A two-channel AF analog switch is used to switch from standard TV operation to the SCART playback mode. An additional analog switch is applied for the channel 1/2 switch-over during multichannel transmission. During standard TV operations, this switch will be functional during two-channel transmission and/or SCART playback if the Kbit has been set accordingly.

2. The quasi-stereo section in the signal path is applied to generate an acoustic sound impression similar to stereo during the mono signal. This circuitry section is comprised of one op amplifier per channel. While one amplifier is provided with an internally regulated gain factor of – 1, the second amplifier can be switched between a gain factor of – 1 and a freely selectable gain factor provided by means of external components. The quasi-stereo effect is achieved by forwarding two different types of signals to the input of the second amplifier. While a standard phase AF signal is forwarded via an external band stop filter, a phase inverted signal is forwarded via an external band filter. The attenuation of these networks is compensated by the op amplifier. The result is the generation of a largely amplitude-linear signal, however, turned by 180° in its phase during medium frequencies. This section of the circuit can be switched off.
   The sound and volume control section is comprised per stereo channel of 3 op amplifiers with electronic potentiometers and/or switches. By using one external capacitor each for the bass and treble control, 31 different levels for emphasis and deemphasis can be set for the bass and treble control during low and/or high frequencies. The subsequent stage enables a switch-controlled expansion of the basewidth. When the basewidth expansion has been switched on, an anti-phase cross-talk of approx. 60% will occur at an input frequency of approx. 300 Hz. The frequency to be applied as well as the percentage of cross-talk are determined by an external RC combination. The volume control, separate for each channel, is comprised of 64 stages each. As a result, the balance control can be realized by using different settings for the channels.

   A physiological volume characteristics is achieved by connecting the volume setting with the treble/bass control. For this purpose, the mean value of the two volume control settings is used. The physiology section can be switched off.

   Subsequent to the connection of the supply voltage, the AF output voltage will be delayed by a delay circuit until all voltages are stabilized. In this manner, interfering crackling noises are prevented.

3. The integrated circuit is controlled by means of an I²C bus interface and a 4 level line from the stereo decoder TDA 6600-2. Via this line the evaluation circuit of the TDA 6600-2 provides the necessary information with respect to the 3 modes mono, dual audio, and stereo by means of three different DC voltage levels. For a compulsory (manual) mono mode, a fourth DC voltage level in opposite direction can be used by the TDA 6600-2. This DC voltage level is programmed via the I²C bus interface of the TDA 6200. The system clock for the input SCL of the I²C bus interface is provided by the processor. Pin SDA functions as data input. It can also supply the setting of the identification signal decoder established via the 4 level output and/or an acknowledge message.

   The data forwarded by the processor are controlled by the I²C bus and subsequently filed in registers according to their functions (latch 1-6).

   If the bus is free (t off time), both lines will be in the marking state (SDA, SCL are HIGH). Each message begins with the start conditions of SDA returning into LOW, while SCL remains HIGH. All additional information transfer takes place during SCL = LOW, and the data is forwarded to the control with the positive clock edge. However, if SDA returns to HIGH, while SCL is in HIGH, the message is ended since the circuit acknowledges a stop condition.

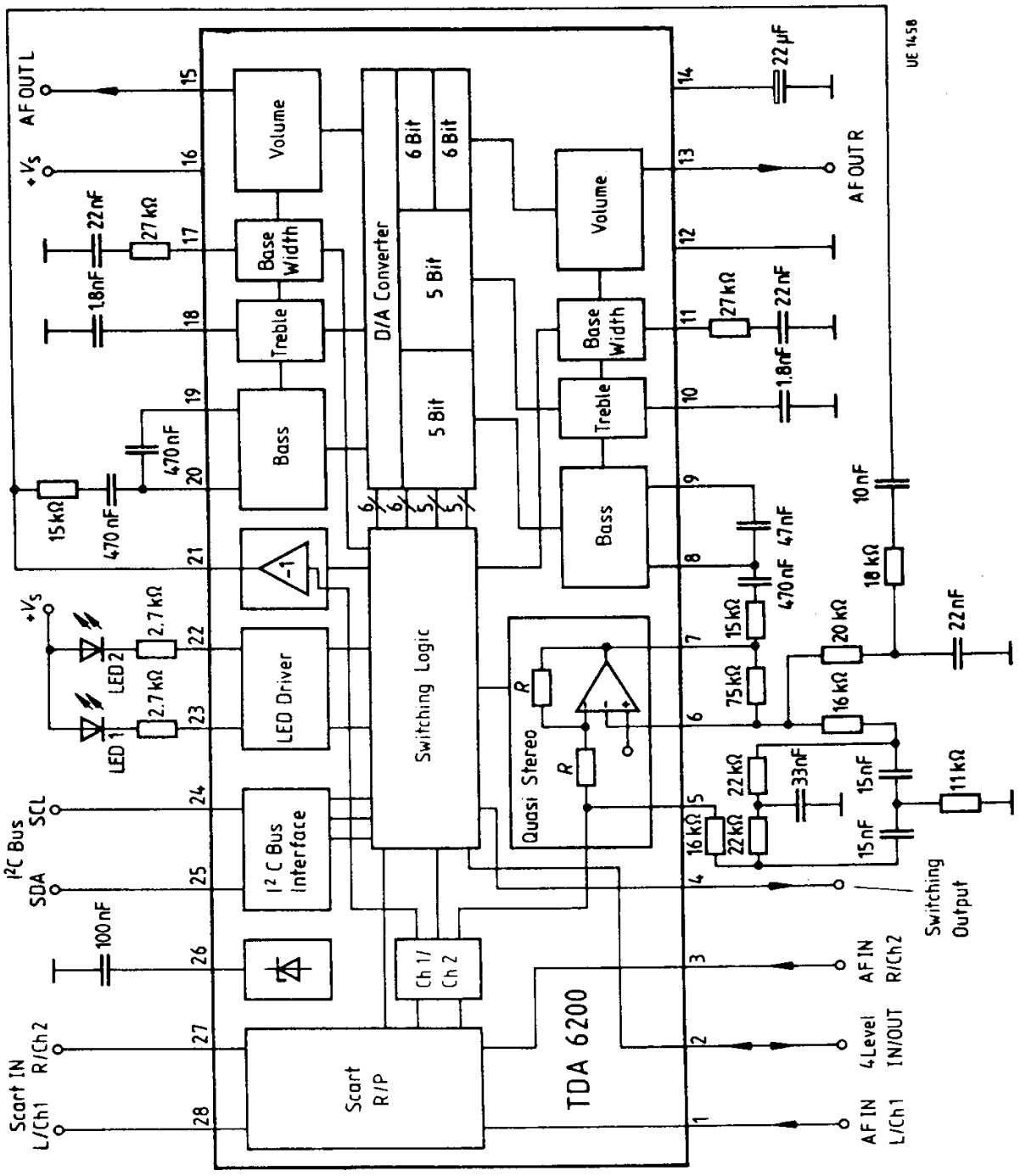
   The logic functions according to the tables on pages 643-645 . All messages are transmitted byte-by-byte, followed by a 9th clock pulse, while the control returns the SDA line to LOW (acknowledge condition). In the read mode, the processor transmits the acknowledge bit (will not be checked by the tone control). The first byte is comprised of 7 address bits used by the processor to select the tone control among several peripheral components (chip select). The 8. bit establishes the direction of the subsequent data flow (read/write bit). The 1. and 2. bit of the data bytes determine which latch will be called up (sub-address).

   The volume information is set with 6 bits (64 positions); the treble and bass control with 5 bits of which the 1. bit (4. bit of the byte) is the sign bit. The 4 bits of the digital-to-analog converter provide 31 different setting levels. The two volume bytes (left, right) and/or treble and bass bytes have to be transmitted in successive order, since they have the same sub-address. The two bytes for the switching function are subdivided into an AF setting byte and a byte for the operation of the SCART jack.

   If the R/W bit = 1 is set during chip addressing, the I²C bus operates in the transmission mode. The momentary position of the stereo decoder (corresponds with the status of the 4 level line) is transmitted.

   The two LED driver outputs enable the display of stereo, mono or dual audio transmission and/or the SCART playback mode.

Block Diagram



Pin Functions

Pin No.	Function
1	AF input for signal from matrix section of TDA 6600-2
2	Bidirectional 4 level control line between TDA 6200 and TDA 6600 used to transmit information with respect to dual audio, mono, stereo and compulsory mono mode
3	AF input for signal from matrix section of TDA 6600-2
4	Switching output to control additional functions (open collector), in turn controlled via I²C bus
5	Low-impedance output to control the quasi-stereo network
6	Inverted input of the quasi-stereo op
7	Low-impedance output of quasi-stereo op, controls bass control
8, 9	Connections for external capacitor for right bass control $f_{-3\,dB} \sim 1/C_{8,9}$
10	Connection for external capacitor for right treble control $f_{-3\,dB} \sim 1/C_{10}$
11	Connection for network of stereo basewidth expansion percentage of cross- talk $\sim 1/R_{11}$ $f_{-3\,dB} = \frac{1}{2\,\pi\,C_{11}\,(R_{11} + 1\,k\Omega)}$
12	GND
13	AF output right (emitter follower)
14	Decoupling for internal DC operation points. Capacitor also determines the duration of the switch-on delay when connecting V_{16}.
15	AF output left (emitter follower)
16	Supply voltage
17	Connection for network of stereo basewidth expansion percentage of cross- talk $\sim 1/R_{17}$ $f_{-3\,dB} = \frac{1}{2\,\pi\,C_{17}\,(R_{17} + 1\,k\Omega)}$
18	Connection for external capacitor of left treble control $f_{-3\,dB} \sim 1/C_{18}$
19, 20	Connections for external capacitor of left bass control $f_{-3\,dB} \sim 1/C_{19,20}$
21	Low-impedance output to control the quasi-stereo network and the left bass control
22	LED driver output for LED 2 (open collector with current limiter)
23	LED driver output for LED 1 (open collector with current limiter)
24	Clock frequency input of I²C bus control (Inter-IC)
25	Data input/output of I²C bus control
26	Reference voltage of typ. 6 V
27	AF input of SCART interface
28	AF input of SCART interface

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_S	0	16	V
Reference current	I_{26}	0	2	mA
DC voltage	$V_{1, 2, 3}$	0	V_S	V
DC voltage	$V_{6, 8, 9}$	0	V_S	V
DC voltage	$V_{10, 14, 18}$	0	V_S	V
DC voltage	$V_{19, 20, 22}$	0	V_S	V
DC voltage	$V_{23, 24, 25}$	0	V_S	V
DC voltage	$V_{27, 28}$	0	V_S	V
DC current	$I_{4, 5, 7}$	0	2	mA
DC current	$I_{11, 13, 15}$	0	2	mA
DC current	$I_{17, 21}$	0	2	mA
Junction temperature	T_j		150	°C
Storage temperature range	T_{stg}	– 40	125	°C
Thermal resistance (system-air)	$R_{th\ SA}$		60	K/W

Operating Range

Supply voltage	V_S	8	15.75	V
Ambient temperature	T_A	0	70	°C
Input frequency	f_i	0	20	kHz

Characteristics

V_S = 15 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current consumption	I_{16}		55	80	mA	LEDs OFF
Reference voltage	V_{26}	5.4	6	6.6	V	
Max. gain AF input/AF output L byte = BF; KL[2] byte = C0	G_{max}	– 2	0	2	dB	SC = 0; phys = 0; RK[1] = 0; Q-S/Bw = 0
SCART input/ AF output L byte = BF; KL byte = C0	G_{max}	– 2	0	2	dB	SC = 1; phys = 0; RK = 0; Q-S/Bw = 0
Min. gain AF input/AF output L byte = 80; KL byte = C0	G_{min}			– 80	dB	SC = 0; phys = 0; RK = 0; Q-S/Bw = 0
SCART input/ AF output L byte = 80; KL byte = C0	G_{min}			– 80	dB	SC = 1; phys = 0; RK = 0; Q-S/Bw = 0
Wow and Flutter L-R	$\Delta a_{L\text{-}R}$			– 2	dB	
Bass emphasis*) KL byte = C0 + DF	$G_{B\,max}$	9	12		dB	f_i = 40 Hz
Bass deemphasis KL byte = C0 + CF	$G_{B\,min}$		– 12	– 10	dB	f_i = 40 Hz
Treble emphasis*) KL byte = DF + C0	$G_{T\,max}$	8.5	12		dB	f_i = 15 Hz
Treble deemphasis KL byte = CF + C0	$G_{T\,min}$		– 12	– 10	dB	f_i = 15 Hz
Input voltage*) SCART, AF	$V_{I\,rms}$	1			V	any KL byte
Input voltage*) SCART, AF	$V_{I\,rms}$	3.5			V	KL byte = CX
Permissible gain quasi-stereo op	$G_{7/6}$			30	dB	Q-S/Bw = 1
Channel separation	$a_{L\text{-}R}$	60			dB	Q-S/Bw = 0; RK = 0
Antiphased cross talk with basewidth ON	$CT_{L\text{-}R}$	45	60	75	%	stereo; RK = 1

*) refer to page 641

[1]) RK ≡ room accustics

[2]) KL ≡ tone

Characteristics (cont,d)
V_S = 15 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Cross-talk rejection SCART switch	$a_{AF/SF}$	60			dB	V_I rms = 2 V
Ch1/Ch2 switch	$a_{CH\ 1/2}$	60			dB	V_I rms = 2 V; dual audio
Total harmonic distortion	$THD_{13/15}$			1	%	any KL[1] byte V_I rms = 1 V
Total harmonic distortion DIN 45 500*)	$THD_{13/15}$		0.3	0.6	%	KL byte = CX; V_I rms = 1 V
Disturbance voltage spacing f_i = 20 Hz – 20 kHz	$a_{S/N}$			78	dB	DIN 45 405; V_I rms = 1 V L byte = BF; KL byte = C0
Disturbance voltage at output f = 20 Hz – 20 kHz	$a_{S/N}$		120	150	µV	L byte = BF; KL byte = C0
				50	µV	L byte = AC; KL byte = C0
			10	20	µV	L byte = 94; KL byte = C0
Noise voltage CCIR DIN 45 405	V_n			650	µV	L byte = BF KL byte = DF + C0
Deviation in amplitude when tone control is in linear position	ΔG		± 0.5	± 1.5	dB	KL byte = C0 f_i = 40 Hz – 15 kHz
Volume decontrol for max. phys.	V_Q/V_I		– 30		dB	phys = 1
Attenuation during MUTE mode	a_{MUTE}	80			dB	M1 = 1
Switching output	$V_{4\ ON}$			0.5	V	I_L = 1 mA
	$I_{4\ OFFI}$			1	µA	
LED driver	$I_{22,\ 23}$			7.5	mA	LED ON
	$V_{22,\ 23}$			1.5	V	$I_{22/23}$ = 7.5 mA
	$I_{22,\ 23}$			50	µA	LED OFF
4 level line Input voltage	V_{I2}	0		1.8	V	recognizes mono
	V_{I2}	2.4		3.9	V	recognizes dual
	V_{I2}	5.2		6.6	V	recognizes stereo
Input current	V_{I2}			3	µA	
Compulsory mono	V_{Q2}			0.2	V	M2 = 1; I_2 = 1 mA

*) refer next page

1) KL ≡ tone

Characteristics (cont,d)
V_S = 15 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
I²C Bus (SCL, SDA)					
SCL, SDA Edges					
Rise time	t_R			1	µs
Fall time	t_F			0.3	µs
Shift Register Clock Pulse SCL					
Frequency	f_{SCL}	0		100	kHz
H-pulse width	t_{HIGH}	4			µs
L-pulse width	t_{LOW}	4			µs
Start					
Set-up time	t_{SUSTA}	4			µs
Hold time	t_{HDSTA}	4			µs
Stop					
Set-up time	t_{SUSTO}	4			µs
Bus free time	t_{BUF}	4			µs
DataTransfer					
Set-up time	t_{SUDAT}	1			µs
Hold time	t_{HDDAT}	1			µs
Inputs SCL, SDA					
Input voltage	V_{IH} V_{IL}	2.4 0.3		5.5 1	V V
Input current	I_{IH} I_{IL}			50 100	µA µA
Output SDA (open collector)					
Output voltage R_L = 2.5 kΩ; I_{QL} = 2 mA	V_{QH} V_{QL}			5.5 0.4	V V

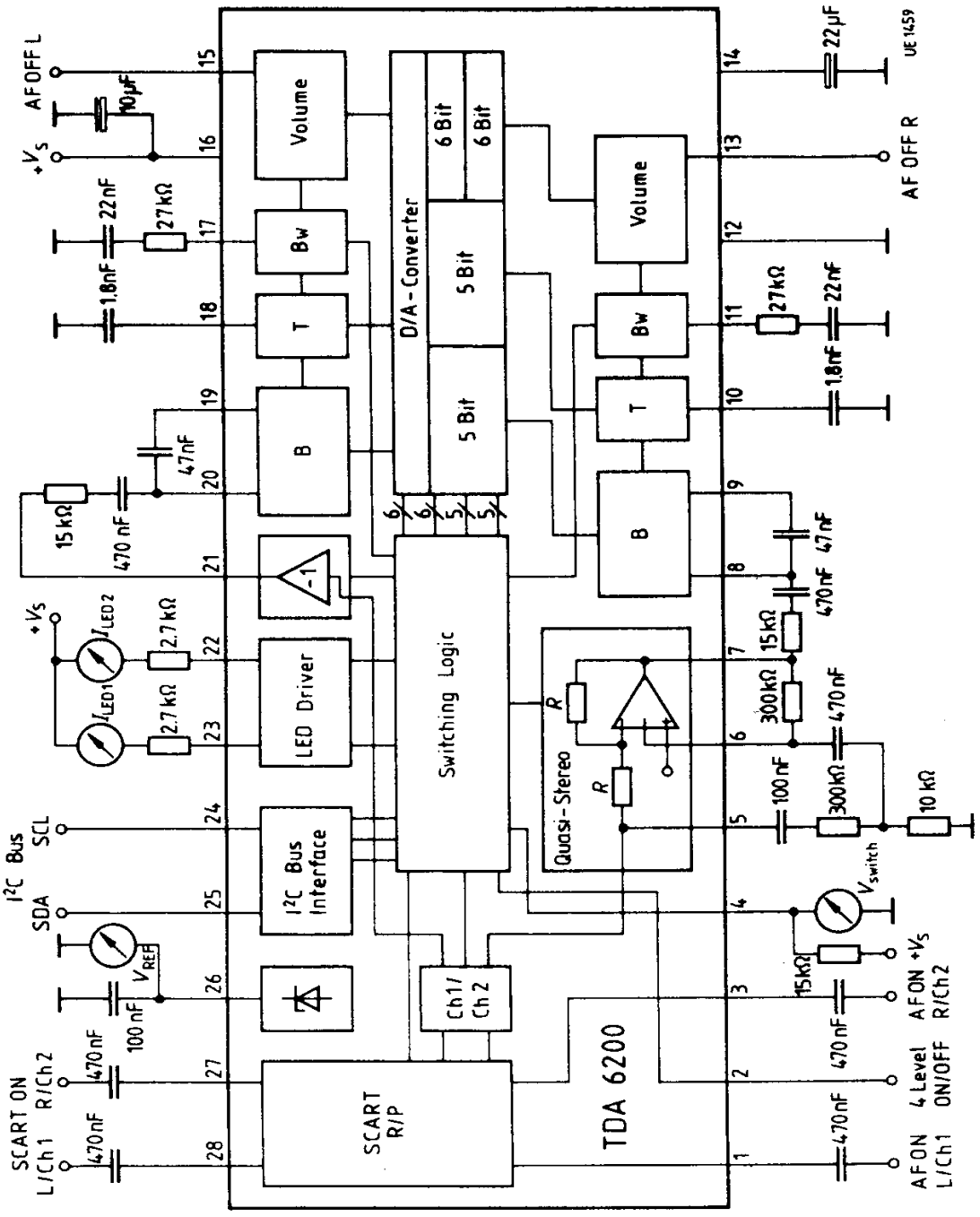
The data marked with an asterisk*) depend on the supply voltage.
With lower V_S the input voltage decreases accordingly.

Characteristics

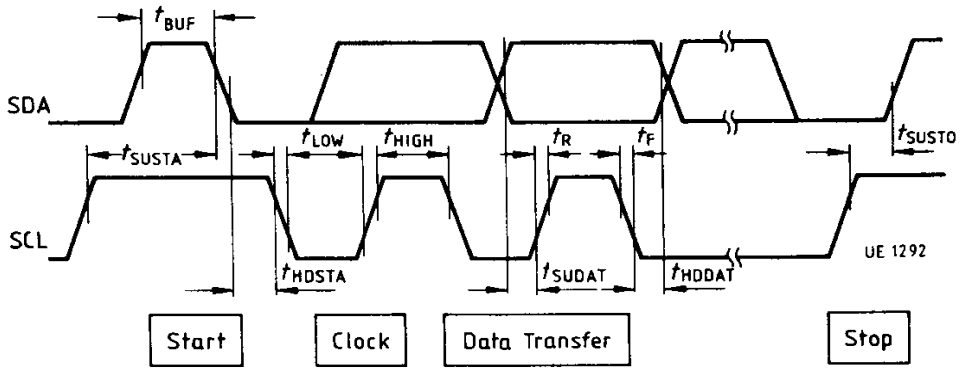
V_S = 15 V; T_A = 25 °C

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Design-Related Characteristics					
Input impedance SCART	$R_{I\,27,\,28}$	35			kΩ
Input impedance AF	$R_{I\,1,\,3}$	35			kΩ
Output impedance	$R_{Q\,5,\,7,\,21}$			200	Ω
Output impedance AF output	$R_{Q\,13,\,15}$			200	Ω
Internal resistance Bw	$R_{I\,11,\,17}$			1	kΩ

Measurement Circuit



I²C Bus Timing Diagram



t_{SUSTA}	Set-up time (start)
t_{HDSTA}	Hold time (start)
t_{HIGH}	Pulse width (clock)
t_{LOW}	Pulse width (clock)
t_{SUDAT}	Set-up time (data transfer)
t_{HDDAT}	Hold time (data transfer)
t_{SUSTO}	Set-up time (stop)
t_{BUF}	Bus free time
t_F	Fall time
t_R	Rise time

The listed times are referenced to the V_{IH} and V_{IL} values.

Software

The following data format is used:

1) **Chip Address**

MSB							LSB	
1	0	0	0	0	0	0	R/W	ack.

MSB will be transmitted first
R/W = 0 IC in the receiving mode

2) **Data Bytes with Sub-Addresses**

a) Volume

MSB							LSB	
1	0	V05	V04	V03	V02	V01	V00	(left) +
1	0	V15	V14	V13	V12	V11	V10	(right)

The two bytes are always transmitted in successive order
V × 5 = MSB
V × 0 = LSB

1	0	0	0	0	0	0	0	min. volume
1	0	1	1	1	1	1	1	max. volume

b) Tone

MSB							LSB	
1	1	X	HV	H3	H2	H1	H0	+
1	1	X	TV	T3	T2	T1	T0	

The two bytes are always transmitted in successive order
HV or TV are sign bits
H3 or T3 = MSB
H0 or T0 = LSB

1	1	X	0	1	1	1	1	min. treble or bass
1	1	X	X	0	0	0	0	linear treble or bass
1	1	X	1	1	1	1	1	max. treble or bass

Software

c) AF set byte

MSB							LSB
0	0	M1	M2	Ch1/2	RK	Phys	Q-S/Bw

M1	= 1	Muting for AF output
M1	= 0	AF ON
M2	= 1	Compulsory mono (via 4 level line)
M2	= 0	Standard operation for identification signal decoder
Ch1/2	= 0	During dual audio mode, channel 1 at AF output
Ch1/2	= 1	During dual audio mode, channel 2 at AF output (only active with dual audio via 4 level line or during SCART playback and Kbit = 1)
RK	= 1	Space sound ON; TV operating mode: Quasi-stereo during mono and dual audio or stereo basewidth expansion during stereo transmission – automatic switch–over via 4 level line SCART playback mode: stereo basewidth expansion ON
RK	= 0	Stereo basewidth expansion and quasi-stereo OFF
Phys	= 1	Physiological volume control ON
Phys	= 0	Physiological volume control OFF
Q-S/Bw	= 1	TV operating mode: Quasi-stereo and stereo basewidth expansion ON SCART playback mode: stereo basewidth expansion ON
Q-S/Bw	= 0	Quasi-stereo and stereo basewidth expansion OFF

d) SCART set byte

MSB							LSB
0	1	SC	Sch	Ch	X	X	X

SC	= 1	SCART playback mode; SCART input connected with AF output
SC	= 0	Standard operation
Sch	= 1	Switching output ON (open collector)
Sch	= 0	Switching output OFF (output can e.g. be used for switch–over from recording to playback mode in the video section)
Ch	= 1	Playback of SCART dual transmission; channel selection via Ch1/2 bit for AF output
Ch	= 0	AF output operates in stereo mode. Playback of SCART stereo (mono) transmission.

Note:

The AF section is automatically controlled by the 4 level line. Compulsory mono M2 is given priority. After Power-ON-Reset all latches are set at 0 (volume min., tone linear, . . .); only the function Q-S/Bw is set at 1.

Software

3) Transmission Mode

requires new chip addressing with R/W bit = 1.

MSB							LSB
St	D	X	X	X	X	X	X

St	D	
1	1	Decoder recognizes mono
0	1	Decoder recognizes stereo
1	0	Decoder recognizes dual
0	0	Does not occur (internally suppressed)

The transmission function is not required for the operation of the IC. Instead this function is used to inform the µC about the status of the identification signal decoder to enable additional functions.

LED Driver

TV operating mode:

4 level line	Ch1/2 bit	LED 1	LED 2
Mono	X	OFF	OFF
Stereo	X	ON	ON
Dual	0	ON	OFF
Dual	1	OFF	ON

SCART playback mode:

SC bit	Ch bit	Ch 1/2 bit	LED 1	LED 2
1	0	X	ON	ON
1	1	0	ON	OFF
1	1	1	OFF	ON

Application Circuit

Stereo Decoder, Matrix and Tone Control