R2A20111SP/DD

Power Factor Correction Controller IC

REJ03F0231-0100
Rev.1.00
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Description

The R2A20111 is a power-factor correction (PFC) controller IC.

This IC adopts continuous conduction mode as PFC operation.

Various functions such as constant power limit, overvoltage detection, overcurrent detection, soft start, feedback-loop disconnection detection, and holding function of PFC operation through momentary outage (PFC hold function) are incorporated in a single chip. These functions reduce external circuitry.

The constant power limit function allows to eliminate a significant amount of coil noise which is generated due to overcurrent detection operation in case of conventional overload.

The PFC hold function enables quick recovery by continuing PFC operation after momentary outage. The hold time can be adjusted by an external capacitance.

Overcurrent detection pin is separately provided.

Latch mode shutdown function is incorporated.

A soft-start control pin provides for the easy adjustment of soft-start operation, and can be used to prevent overshooting of the output voltage.

Features

- Maximum ratings
  - Power-supply voltage Vcc: 24 V
  - Operating junction temperature Tjopr: – 40 to 125°C
- Electrical characteristics
  - VREF output voltage VREF: 5.0 V ± 3%
  - UVLO operation start voltage VH: 10.5 ± 0.9 V
  - UVLO operation stop voltage VL: 9.0 ± 0.7 V
  - PFC output maximum ON duty Dmax-out: 95% (typ.)
- Functions
  - Constant power limit function
  - Continuous conduction mode
  - Hold function of PFC operation on momentary outage (PFC hold function)
  - Overvoltage detection
  - Overcurrent detection
  - Soft start
  - Feedback loop disconnection detection
  - IC shutdown function
  - Package lineup: SOP-16 and DILP-16

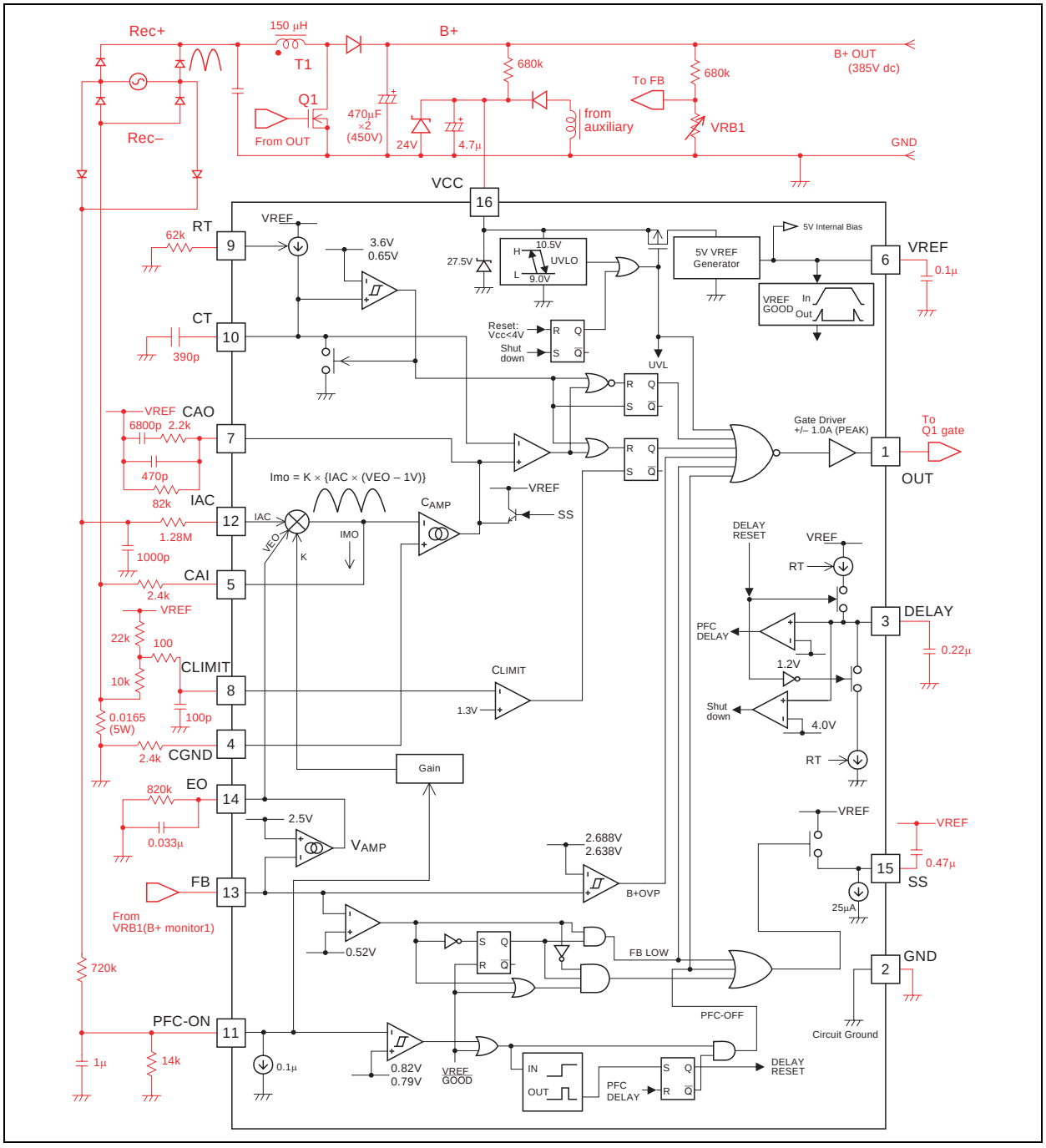
Applications

- Flat panel display
- Projector
- Desktop PC
- White goods

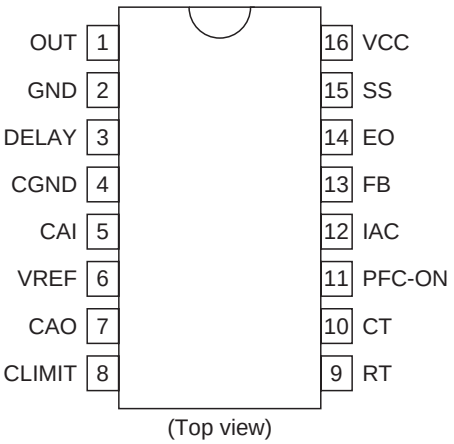
Ordering Information

Part No.	Package Name	Package Code	Taping Spec.
R2A20111SPW0	FP-16DAV	PRSP0016DH-B	2000 pcs./one taping product
R2A20111DDU0	DP-16FV	PRDP0016AE-B	—

System Diagram



Pin Arrangement



Pin Description

Pin No.	Pin Name	I/O	Function
1	OUT	Output	Power MOS FET gate driver output
2	GND	—	Ground
3	DELAY	Input/Output	Hold time adjust and IC shutdown
4	CGND	Input	Non-inverting input of current amplifier
5	CAI	Input/Output	Inverting input of current amplifier and Current output for PFC control
6	VREF	Output	Reference voltage output
7	CAO	Output	Current amplifier output
8	CLIMIT	Input	Overcurrent detection
9	RT	Input/Output	Timing resistor for settings of operational frequency, and the maximum CAI pin and DELAY pin current
10	CT	Output	Timing capacitor for operational frequency adjust
11	PFC-ON	Input	Detection of input AC voltage level
12	IAC	Input	Detection of input AC waveform
13	FB	Input	Voltage amplifier input
14	EO	Output	Voltage amplifier output
15	SS	Output	Timing capacitor for soft-start time adjust
16	VCC	Input	Power supply voltage input

Description of Pin Functions

OUT Pin:

The power MOS FET gate-drive signal is output from this pin, and takes the form of a rectangular waveform with an amplitude of VCC-GND.

GND Pin:

The ground terminal.

DELAY Pin:

This pin has two functions; (1) setting the PFC function hold time for cases of momentary outage and (2) IC shutdown. Current that flows through the DELAY pin is in inverse proportion to the RT pin resistance. Source current is 4.7/RT [A] and sink current is 42.3/RT [A]. Normal operation is in the state that sink current flows.

(1) Setting the PFC function hold time for momentary outage

When the PFC-ON pin is driven below 0.79 V (typ.) due to a momentary outage, the delay pin functions as source current. PFC operation continues until the capacitor is charged to 1.2 V (typ.). After the voltage on the delay pin reaches 1.2 V (typ.), the pin functions as sink current, and PFC operation terminates. The PFC function hold time can be set by the value of the external capacitor.

(2) Shutdown

When this pin is pulled up to 4 V (typ.) or higher, the IC enters the shutdown state. Accordingly, the VREF signal becomes low and the operating current becomes several hundred μA. The IC does not resume operation until Vcc falls to 4 V (max.) or below.

CGND Pin:

This pin is the non-inverting input to the current amplifier.

CAI Pin:

This pin is the inverting input to the current amplifier and functions as source current for PFC control. AC current is controlled to be proportional to the source current and the power factor is corrected.

VREF Pin:

Temperature-compensated voltage with an accuracy of 5 V ± 3% is output from this pin. The pin should supply no more than 5 mA (max.) source current. This pin has no sink capabilities.

CAO Pin:

This pin is the current amplifier output, and is connected to the phase-compensation circuit of the current amplifier. The result of comparison of the voltage on this pin and the CT pin produces the pulse output from the OUT pin. The pulse is limited when the voltage on the CAO pin rises.

CLIMIT Pin:

This pin is for detecting overcurrent. When the voltage on this pin drops to 1.3 V (typ.) or below, OUT pin is stopped.

RT Pin:

This pin is for frequency adjustment of the oscillator and connected to GND via resistor. The IC operating frequency is determined by this resistance value and the CT pin capacitance value.

Additionally, this resistance value determines the maximum current on the CAI pin and the current on the DELAY pin.

CT Pin:

This pin is for frequency adjustment of the oscillator and connected to GND via capacitor. The IC operating frequency is determined by this capacitance value and the resistance value of the RT pin.

PFC-ON Pin:

This pin is applied smoothing voltage of rectified AC voltage and detects the input AC voltage level. When 0.82 V (typ.) or more is applied to this pin, PFC operation starts. When the voltage is 0.79 V (typ.) or lower, the PFC operation stops after the PFC operation hold time (refer to the description of DELAY pin operation).

IAC Pin:

This pin is for detecting waveform of the input AC voltage.

FB Pin:

This pin is the input to the voltage amplifier. This pin is applied to voltage divided PFC output with resistors. The feedback loop is intended to keep 2.5 V (typ.).

When output voltage rises up and the voltage of this pin is higher than 2.688 V (typ.) or more, the OUT pin is stopped. Moreover, when this voltage of this pin is 0.52 V (typ.) or lower, the OUT pin is also stopped. These functions detect overvoltage, low voltage, and feedback-loop disconnection.

EO Pin:

This pin is the output of the voltage amplifier. This pin is connected to the phase-compensation circuit of the voltage amplifier.

SS Pin:

This pin is connected to GND or VREF via a capacitor. This pin is pulled up to the voltage on the VREF pin until PFC operation starts. When the voltage on the PFC-ON pin has reached 0.82 V (typ.), PFC operation starts and this pin flows 25 μA source current. Operation of the CAO pin is affected by that of the SS pin, the pulse width of the OUT pin is limited, and this prevents overshooting when start up.

VCC Pin:

This pin is for the IC power supply. The IC starts up at 10.5 V (typ.), and stops at 9 V (typ.).

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit	Note
Supply voltage	VCC	24	V	
OUT peak current	Ipk-out	±1.0	A	3
OUT DC current	Idc-out	±0.1	A	
Terminal voltage	Vi-group1	–0.3 to Vcc	V	4
	Vi-group2	–0.3 to Vref	V	5
CAO voltage	Vcao	–0.3 to Vcaoh	V	
EO voltage	Veo	–0.3 to Veoh	V	
DELAY voltage	Vdelay	–0.3 to +6.5	V	
CAI voltage	Vi-cs	–1.5 to +0.3	V	
RT current	Irt	–200	μA	
IAC current	Iiac	0.6	mA	
VREF current	Io-ref	–5	mA	
Power dissipation	Pt	1	W	6
Operating junction temperature	Tj-opr	–40 to +125	°C	
Storage temperature	Tstg	–55 to +150	°C	

Notes: 1. Rated voltages are with reference to the GND pin.
2. For rated currents, inflow to the IC is indicated by (+), and outflow by (–).
3. The transient current when driving capacitive load.
4. This is the rated voltage for the following pin:
OUT.
5. This is the rated voltage for the following pins:
CGND, VREF, CLIMIT, RT, CT, PFC-ON, IAC, FB, SS
6. Thermal resistance of packages

Package	θja	θjc	Note
DIP16	120°C/W	50°C/W	—
SOP16	120°C/W	—	40 × 40 × 1.6 [mm], Mounted on a glass epoxy printed board with 10% wiring density
	—	35°C/W	Infinite heat sink

Electrical Characteristics

(Ta = 25°C, VCC = 12 V, RT = 27 kΩ, CT = 1000 pF)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Supply	Start threshold	VH	9.6	10.5	11.4	V	
	Shutdown threshold	VL	8.3	9.0	9.7	V	
	UVLO hysteresis	dVUVL	1.0	1.5	2.0	V	
	Startup current	Is	140	200	260	µA	VCC = 9.5 V
	Is temperature stability	dIs/dTa	—	–0.3	—	%/°C	*1
	Operating current	Icc	3.45	4.5	6.45	mA	IAC = 0 A, CL = 0 F
VREF	Output voltage	Vref	4.85	5.00	5.15	V	Isource = 1 mA
	Line regulation	Vref-line	—	5	20	mV	Isource = 1 mA, VCC = 12 V to 23 V
	Load regulation	Vref-load	—	5	20	mV	Isource = 1 mA to 5 mA
	Temperature stability	dVref	—	±80	—	ppm/°C	Ta = –40 to 125°C *1
Oscillator	Initial accuracy	fout	58.5	65	71.5	kHz	Measured pin: OUT
	fout temperature stability	dfout/dTa	—	±0.1	—	%/°C	Ta = –40 to 125°C *1
	fout voltage stability	fout-line	–1.5	0.5	1.5	%	VCC = 12 V to 18 V
	CT peak voltage	Vct-H	—	3.6	4.0	V	*1
	Ramp valley voltage	Vct-L	—	0.65	—	V	*1
	RT voltage	Vrt	1.17	1.25	1.33	V	
Soft start	Sink current	Iss	15.0	25.0	35.0	µA	SS = 2 V
Current limit	Threshold voltage	VCL	1.222	1.3	1.378	V	
	Delay to output	td-CL	—	100	200	ns	CLIMIT = 2 to 0 V
V_{AMP}	Feedback voltage	Vfb	2.40	2.50	2.60	V	FB-EO Short
	Input bias current	Ifb	–0.3	0	0.3	µA	Measured pin: FB
	Open loop gain	Av-v	—	53	—	dB	*1
	High voltage	Veoh	5.2	5.7	6.2	V	FB = 2.3 V, EO: Open
	Low voltage	Veol	—	0.1	0.3	V	FB = 2.7 V, EO: Open
	Source current	Isrc-eo	–180	–120	–90	µA	FB = 1.0 V, EO = 2.5 V
	Sink current	Isnk-eo	90	120	180	µA	FB = 4.0 V, EO = 2.5 V
	Transconductance	Gm-v	150	200	290	µA/V	FB = 2.5 V, EO = 2.5 V

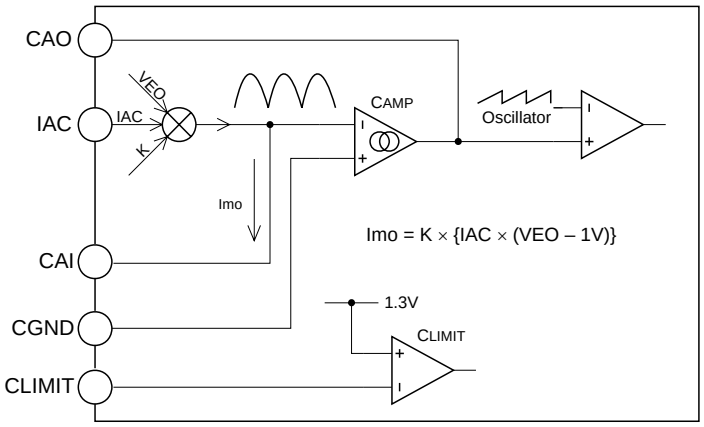
Note: 1. Design spec.

Electrical Characteristics (cont.)

(Ta = 25°C, VCC = 12 V, RT = 27 kΩ, CT = 1000 pF)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
C_{AMP}	Input offset voltage	Vio-ca	—	(–10)	0	mV	*1
	Open loop gain	Av-ca	—	68	—	dB	*1
	High voltage	Vcaoh	5.2	5.7	6.2	V	
	Low voltage	Vcaol	—	0.1	0.3	V	
	Source current	Isrc-ca	–135	–90	–67	μA	CAO = 2.5 V
	Sink current	Isnk-ca	67	90	135	μA	CAO = 2.5 V
	Transconductance	Gm-c	530	700	1000	μA/V	*1
IAC/ Multiplier	IAC pin voltage	Viac	1.6	2.3	3.0	V	IAC = 100 μA
	Imo current 1	Imo1	–61.3	–51.5	–41	μA	EO = 2.5 V, IAC = 150 μA PFC-ON = 1.2 V
	Imo current 2	Imo2	–197.9	–165	–131.5	μA	EO = Vcaoh, IAC = 150 μA PFC-ON = 1.2 V
	Imo current 3	Imo3	–32.8	–27	–21.2	μA	EO = 2.5 V, IAC = 375 μA PFC-ON = 2.5 V
	Imo current 4	Imo4	–110.4	–92	–73.6	μA	EO = Vcaoh, IAC = 375 μA PFC-ON = 2.5 V
OUT	Minimum duty cycle	Dmin-out	—	—	0	%	CAO = 4.0 V
	Maximum duty cycle	Dmax-out	90	95	98	%	CAO = 0 V
	Rise time	tr-out	—	30	100	ns	CL = 1000 pF
	Fall time	tf-out	—	30	100	ns	CL = 1000 pF
	Low voltage	Vol1-out	—	0.05	0.2	V	Iout = 20 mA
		Vol2-out	—	0.5	2.0	V	Iout = 200 mA (Pulse test)
		Vol3-out	—	0.03	0.7	V	Iout = 10 mA, VCC = 5 V
	High voltage	Voh1-out	11.5	11.9	—	V	Iout = –20 mA
		Voh2-out	10.0	11.0	—	V	Iout = –200 mA (Pulse test)
Shut down	Shut down voltage	Vshut	3.30	4.00	4.70	V	Input: DELAY
	Reset voltage	Vres	—	—	4.0	V	Input: Vcc
	Shut down current	Ishut	120	190	260	μA	VCC = 9 V

Note: 1. Design spec.

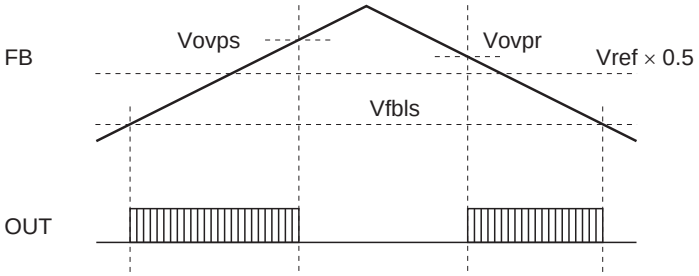


Electrical Characteristics (cont.)

(Ta = 25°C, VCC = 12 V, RT = 27 kΩ, CT = 1000 pF)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Supervisor	PFC enable voltage	Von-pfc	0.74	0.82	0.9	V	Input pin: PFC-ON
	PFC disable voltage	Voff-pfc	0.71	0.79	0.86	V	Input pin: PFC-ON
	PFC disable delay threshold voltage	Vd-pfc	1.05	1.20	1.30	V	Input pin: DELAY
	Input current	Ipfc-on	–1.0	–0.2	1	µA	PFC-ON = 2 V
	B+ OVP set voltage	dVovps	0.125	0.188	0.250	V	Input pin: FB *1
	B+ OVP reset voltage	dVovpr	0.075	0.138	0.200	V	Input pin: FB *1
	FB low set voltage	Vfbls	0.425	0.52	0.615	V	Input pin: FB
	DELAY source current	Isrc-delay	–47.5	–42.5	–38	µA	DELAY = 1 V RT = 27 kΩ
	DELAY sink current	Isnk-delay	—	770	—	µA	DELAY = 1 V RT = 27 kΩ *2

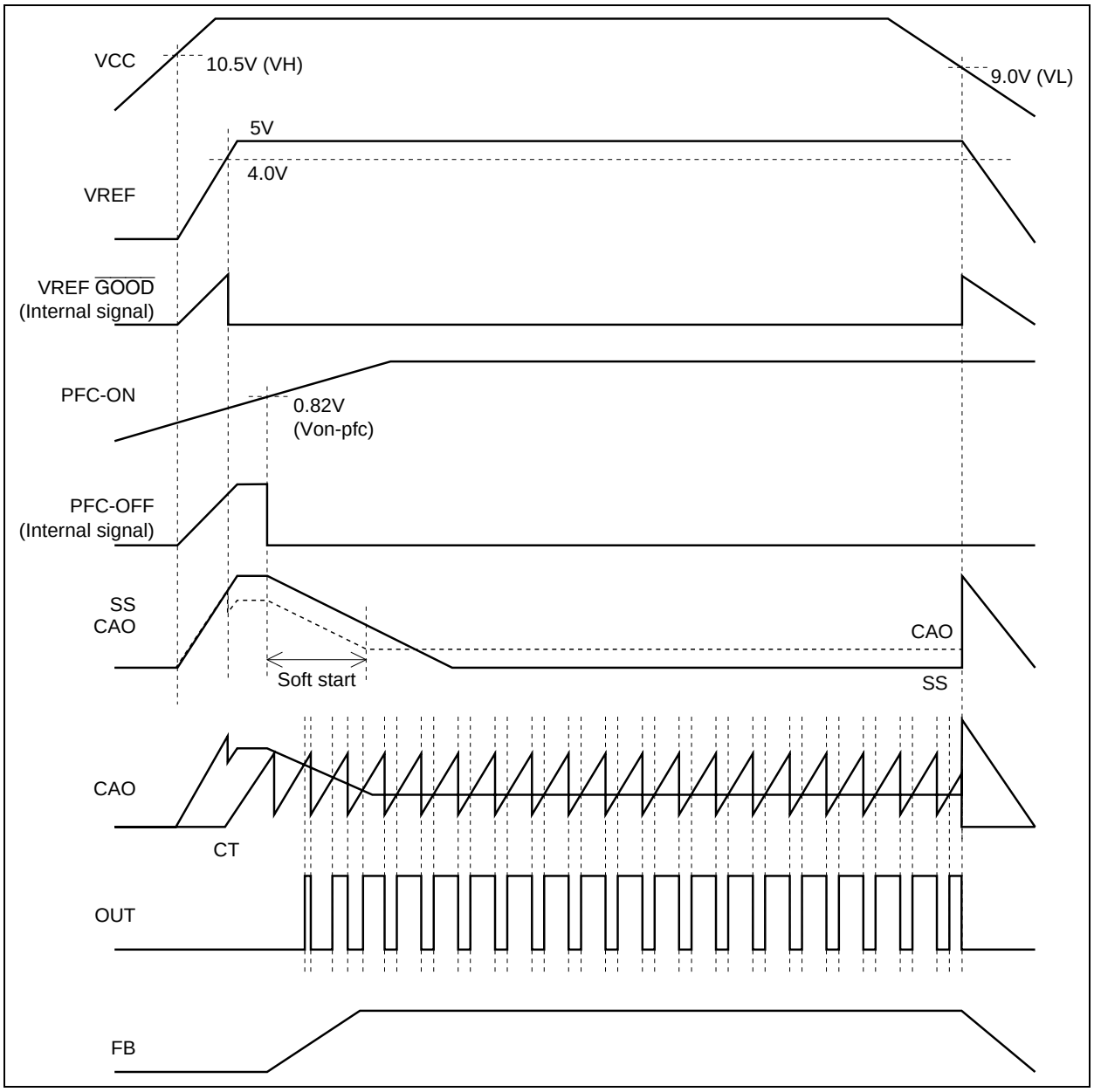
Note: 1. dVovps = Vovps – Vref × 0.5
dVovpr = Vovpr – Vref × 0.5



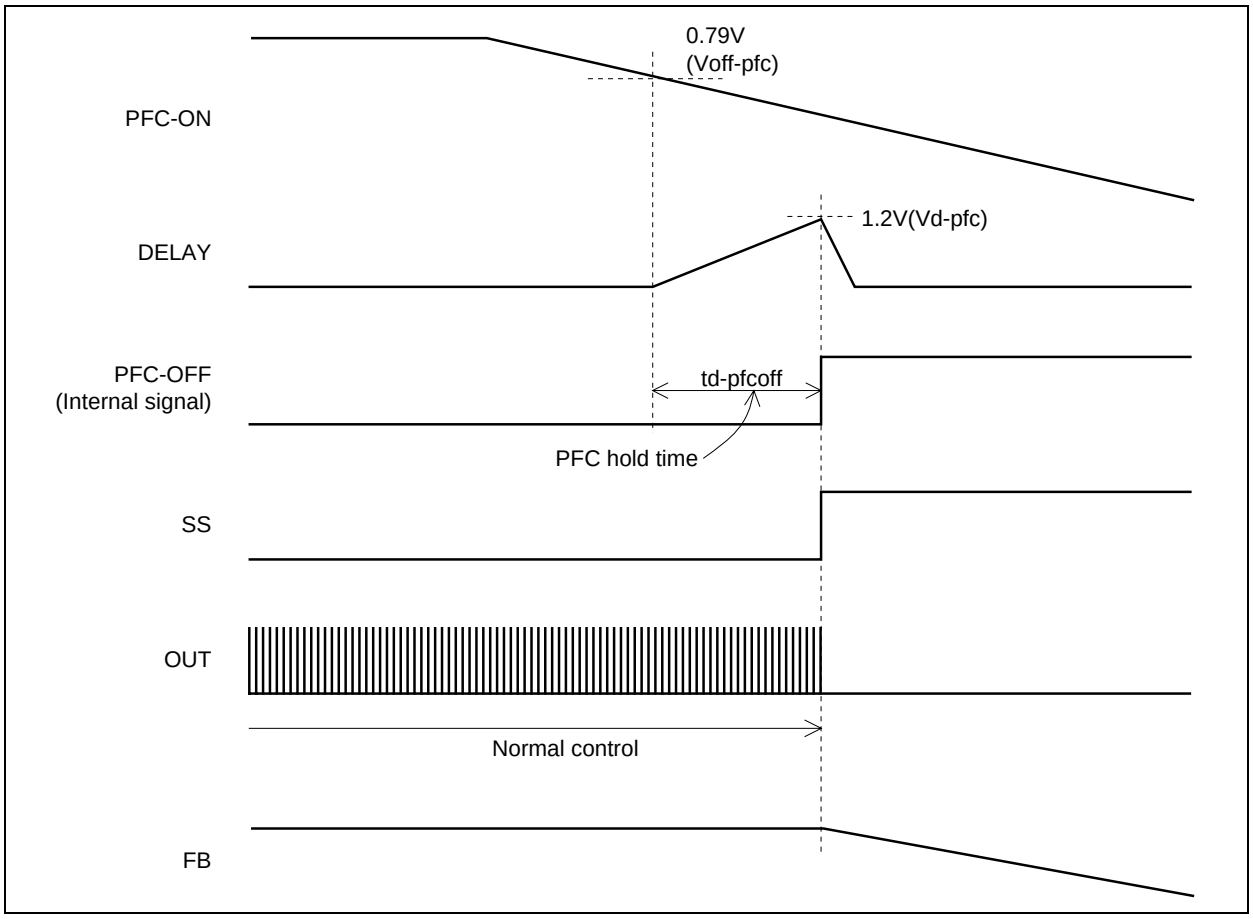
2. Design spec.

Timing Chart

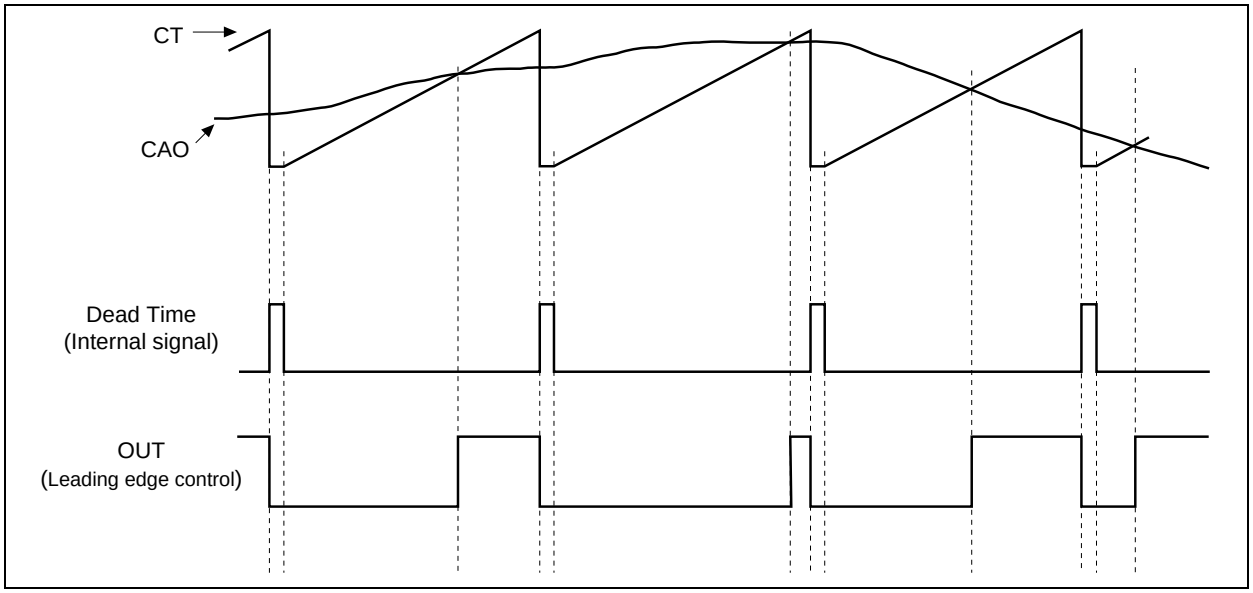
1. Startup and Stop Timing



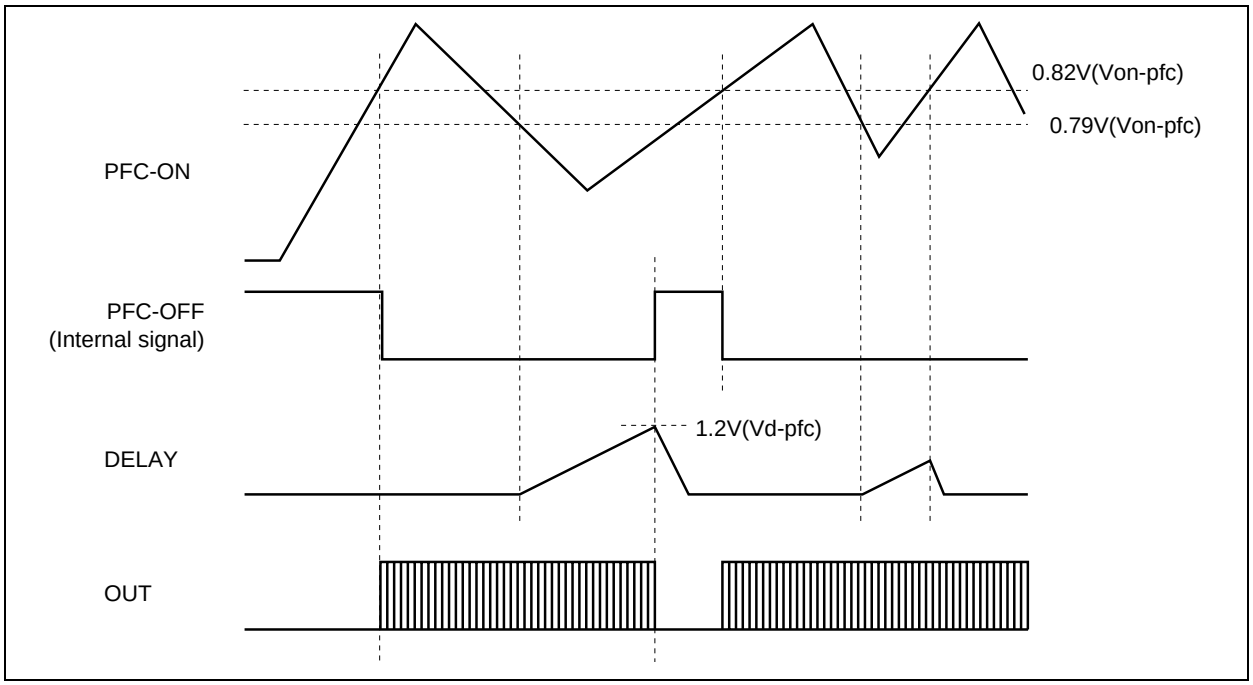
2. Stop Timing by PFC-ON Pin



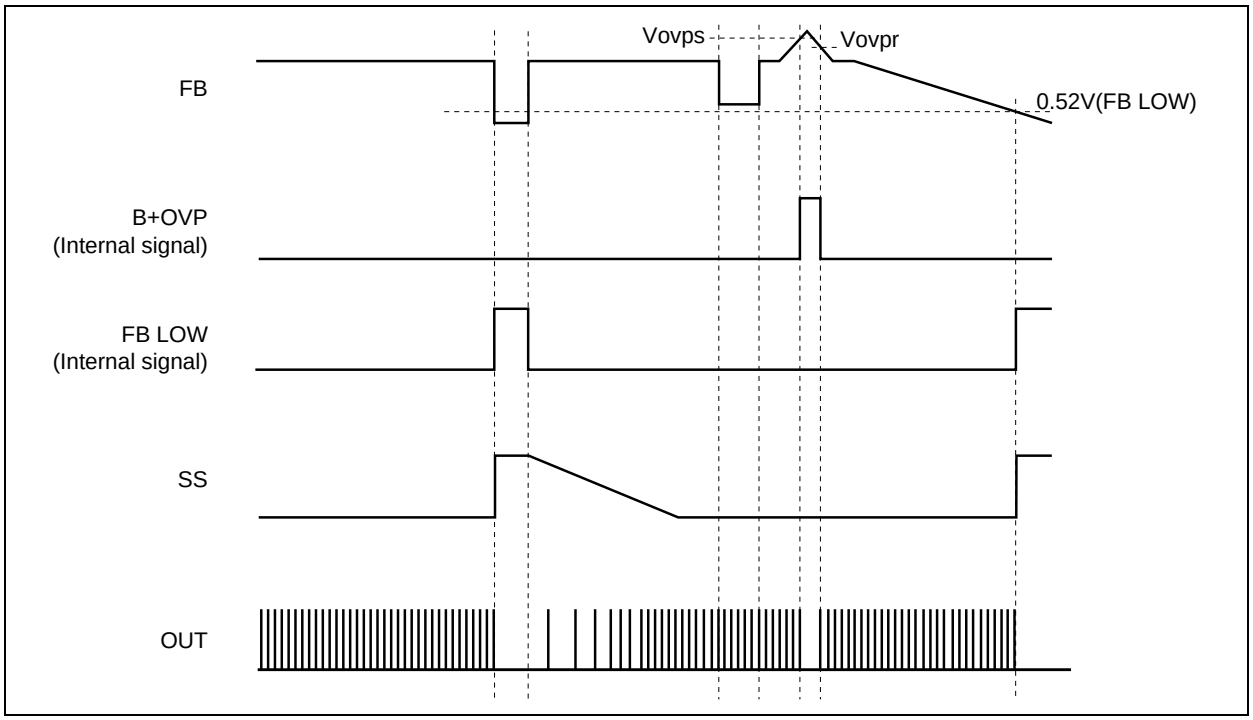
3. Oscillator, Gate Drive Output



4. PFC Operation On/Off



5. FB Supervisor



Description of Functions

1. UVL Circuit

The UVL circuit monitors the Vcc voltage. When the voltage is lower than 9.0 V, the IC is stopped. When the voltage is higher than 10.5 V, the IC is started.

When operation of the IC is stopped by the UVL circuit, the driver circuit output is fixed low, and output of VREF and the oscillator are stopped.

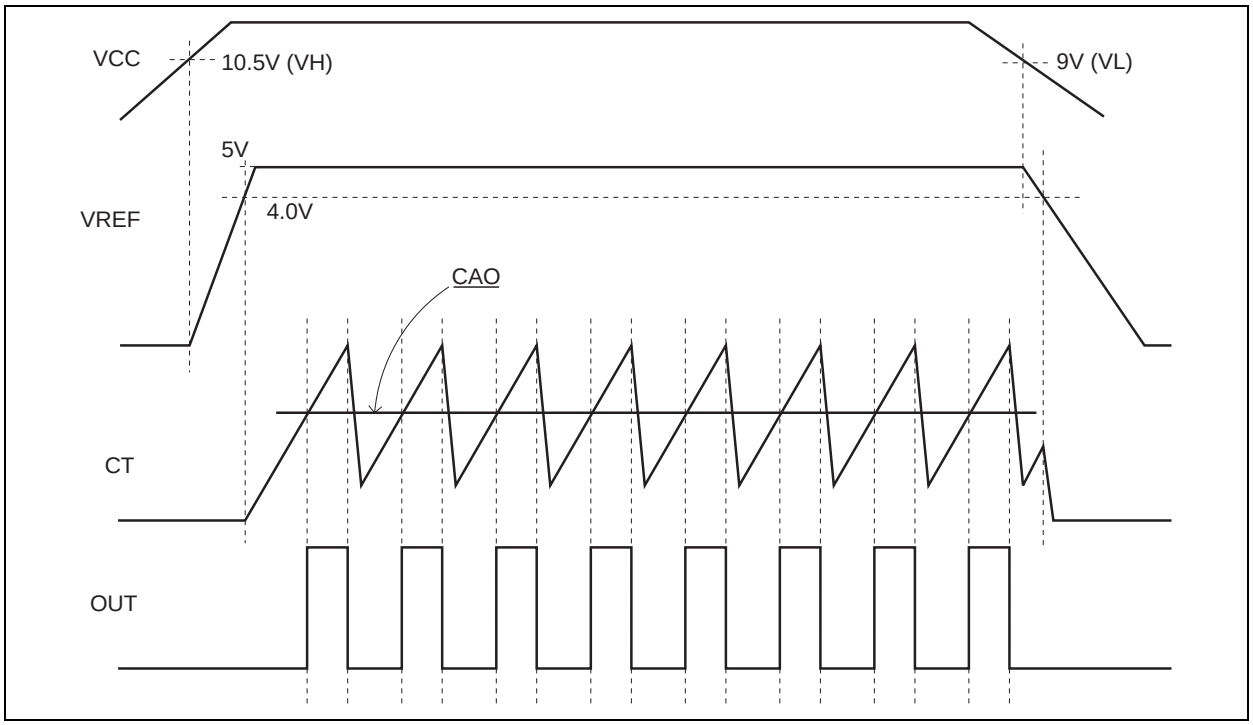


Figure 1 UVL Operation

2. Operating Frequency

The R2A20111 operating frequency fosc is determined by adjusting the timing resistor Rt (the RT pin, pin 9) and the timing capacitance Ct (the CT pin, pin 10). The operating frequency is approximated by the following expression:

$$fosc = \frac{1.755 \times 10^6}{Rt\ (k\Omega) \times Ct\ (pF)}\ (kHz)$$

Make sure to use a 7 kΩ or more resistance because of the maximum rating of the RT-pin. Meanwhile, as the resistance increases, the IC will become more susceptible to noise, etc. The resistance, therefore, should be up to about 100 kΩ. Also, use a 100 pF or more for the timing capacitance to reduce effects from parasitic capacitance and noise.

When the IC is operated at high frequencies, the expression becomes less accurate due to the IC internal delay time, etc. Please confirm operation the value with the actually mounted IC. The maximum operating frequency is 400 kHz. As a reference, the operating frequency data when the timing resistor and the timing capacitance are changed is shown in the figure below.

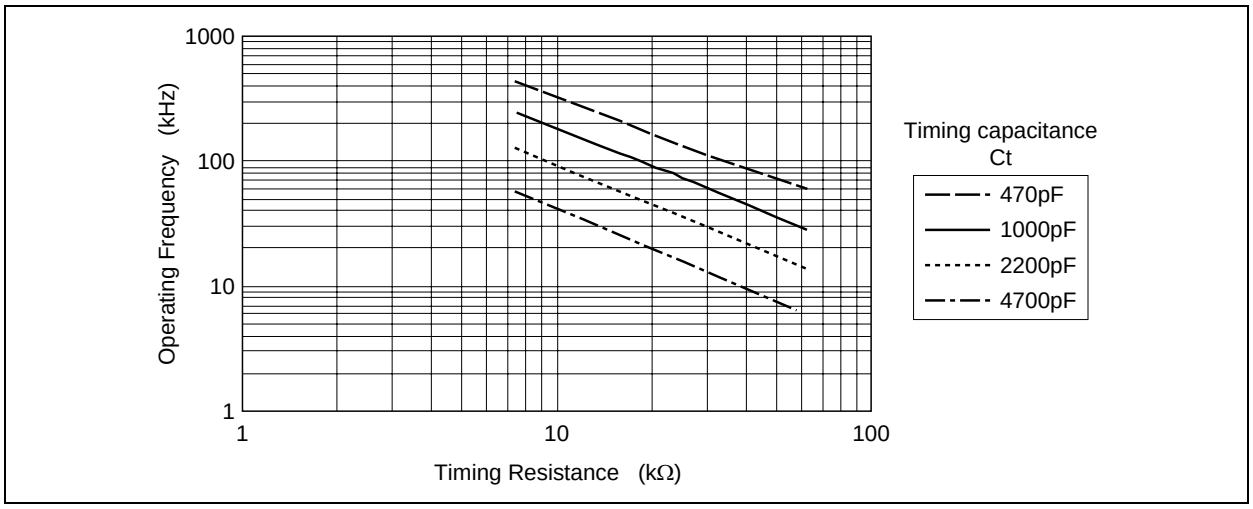


Figure 2 Operating Frequency Characteristics

3. Soft Start

This function gradually increases the pulse width of the OUT pin from a 0% duty cycle at the startup. By preventing a sudden increase of the pulse width, potential problems such as transient stress on the external parts, overshoot of the PFC output voltage (B+ voltage), or coil noise generated due to overcurrent will be prevented. Although the duty cycle is controlled by the CAO signal, operation of the CAO pin is affected by the voltage on the SS pin during the soft start. When the voltage on the CAO pin reaches the required voltage level, the soft start ends and operation transfers to the normal control.

The soft-start time can be set by an external capacity.

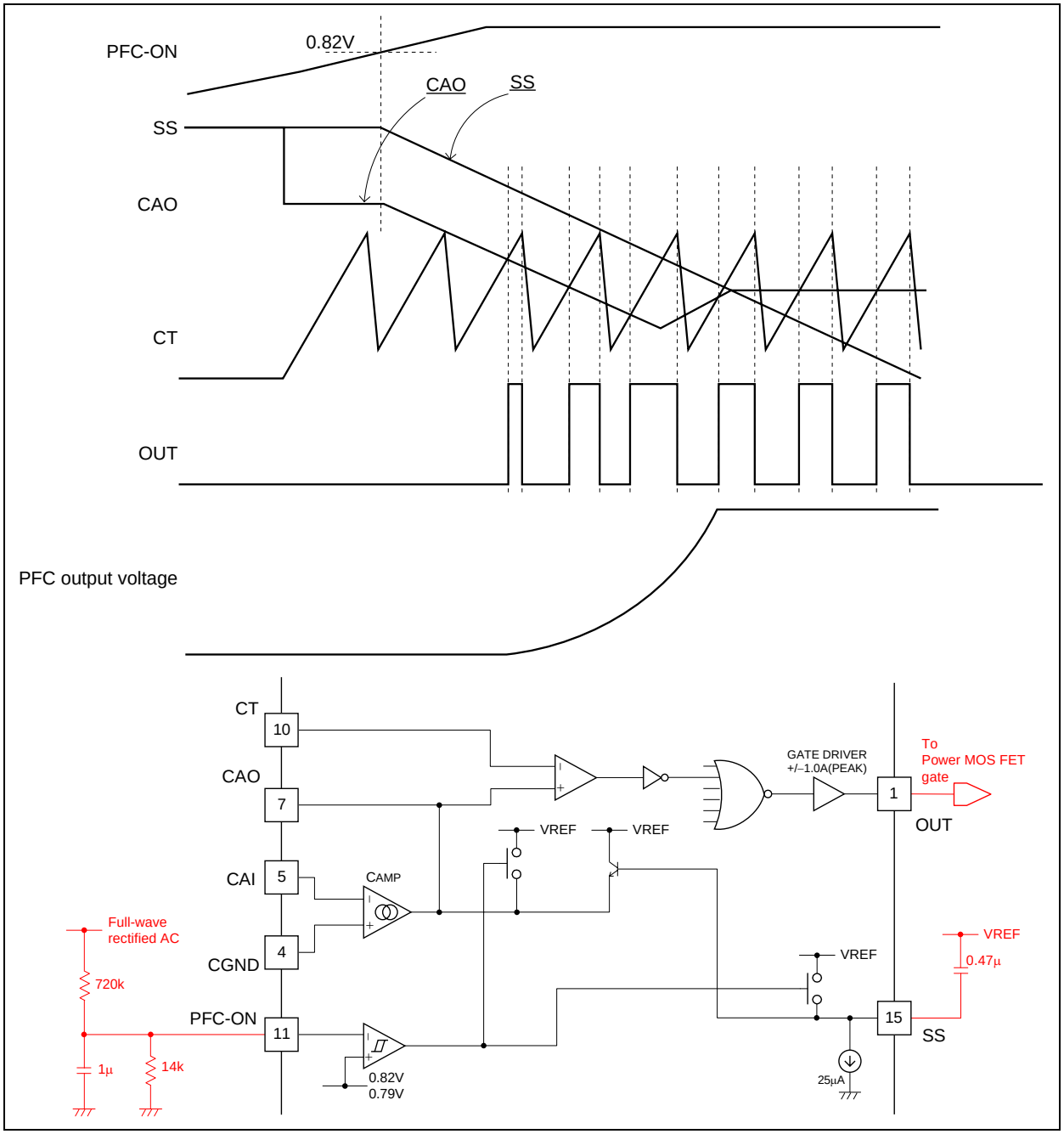


Figure 3 Soft-Start Operation Waveform

4. PFC-ON Pin Function

The PFC-ON pin is applied smoothing voltage of rectified AC voltage. Accordingly, the AC voltage state is detected and each function depending on the power-supply state is operated. Details of their operation are given below. Note, however, that the functions do not operate when VREF voltage is lower than 4 V as UVL operation and shutdown state.

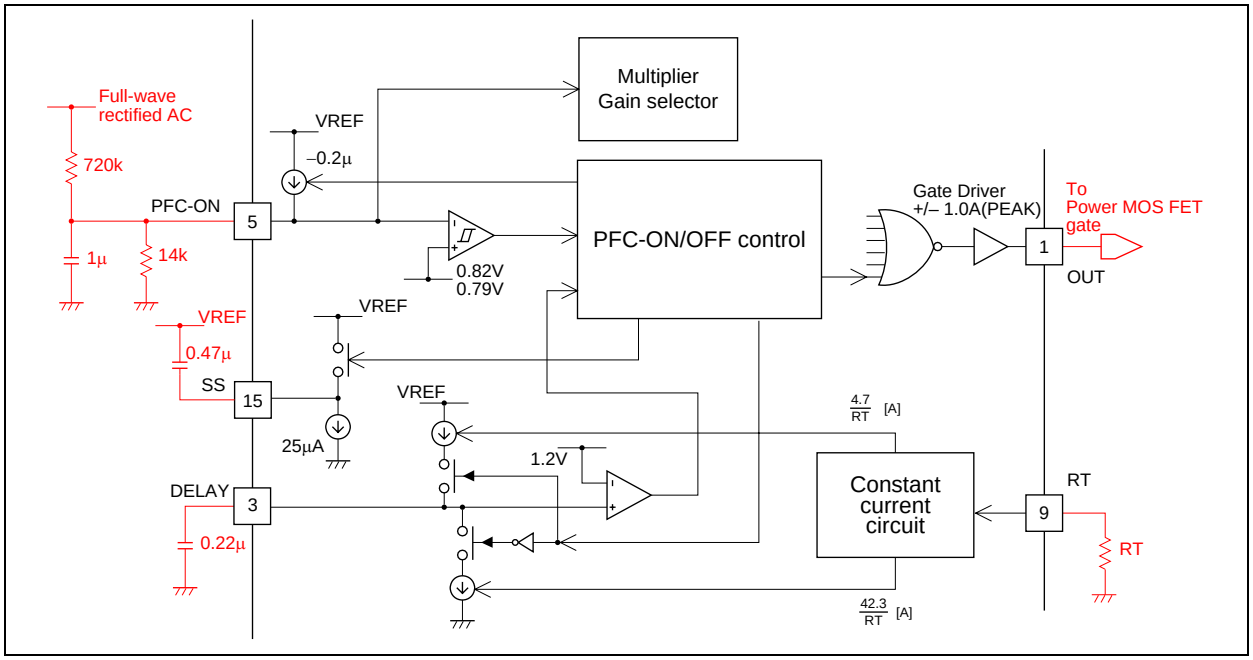


Figure 4 Internal Circuits Connected to the PFC-ON Pin

4-1. Power-Supply Startup Operation

When the AC voltage is applied, the voltage on the PFC-ON pin rises and the PFC output voltage is charged to about $\sqrt{2}$ × AC voltage. After the voltage on the PFC-ON pin exceeds 0.82 V, the voltage of the SS pin starts to be discharged and PFC operation starts. Once the PFC operation starts, the PFC output voltage is boosted to the prescribed voltage.

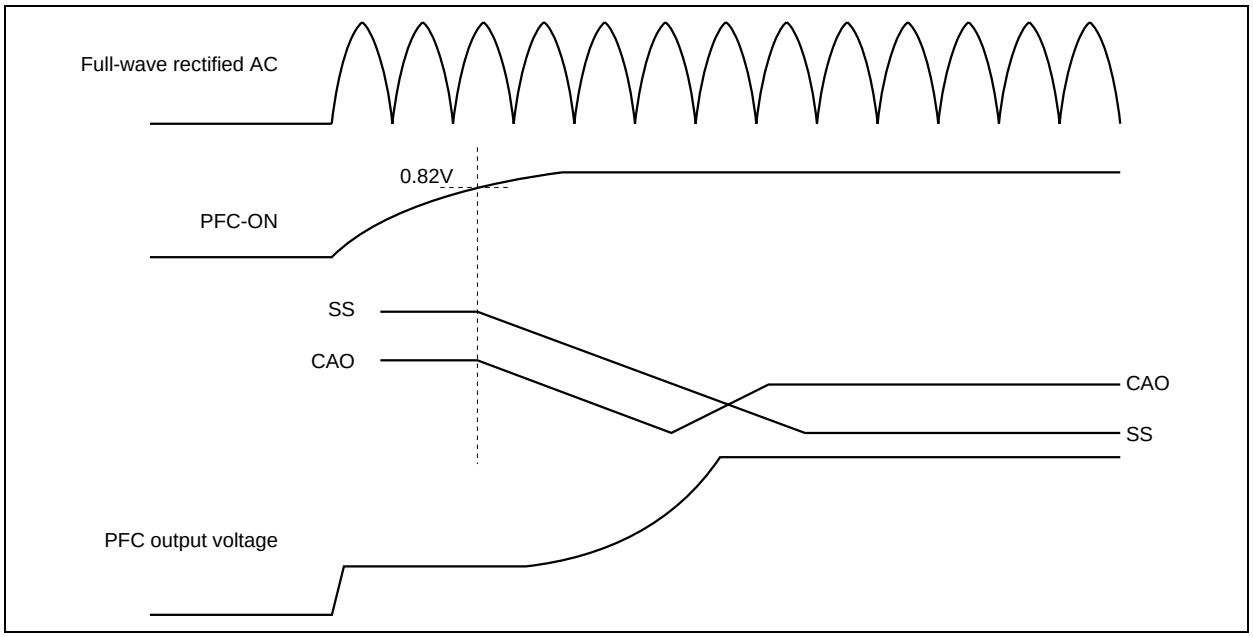


Figure 5 Waveform in Operations in Startup

4-2. Multiplier Gain Switching

Multiplier gain is switched according to the input AC voltage.

4-3. Operation on a Momentary Outage (PFC operation hold on momentary outage: PFC hold function)

(1) When the Momentary Outage is Short

During a momentary outage, the voltage on the PFC-ON pin is discharged. When it reaches 0.79 V, charging of the capacitor on the DELAY pin starts. When AC-voltage input is resumed, and the voltage on the DELAY pin doesn't reach 1.2 V before the voltage on the PFC-ON pin rises above 0.82 V, The PFC output voltage resumes quickly since the soft-start function is not operated.

When the voltage on the PFC-ON pin falls below 0.6 V during a momentary outage, the source current of the PFC-ON pin starts to increase. As the voltage on the PFC-ON pin becomes low, the amount of current increases. Since the external resistor is connected to GND, the voltage on the PFC-ON pin is balanced between the source current and the voltage determined by the resistance. This function prevents increase of AC current right after AC-voltage input is resumed.

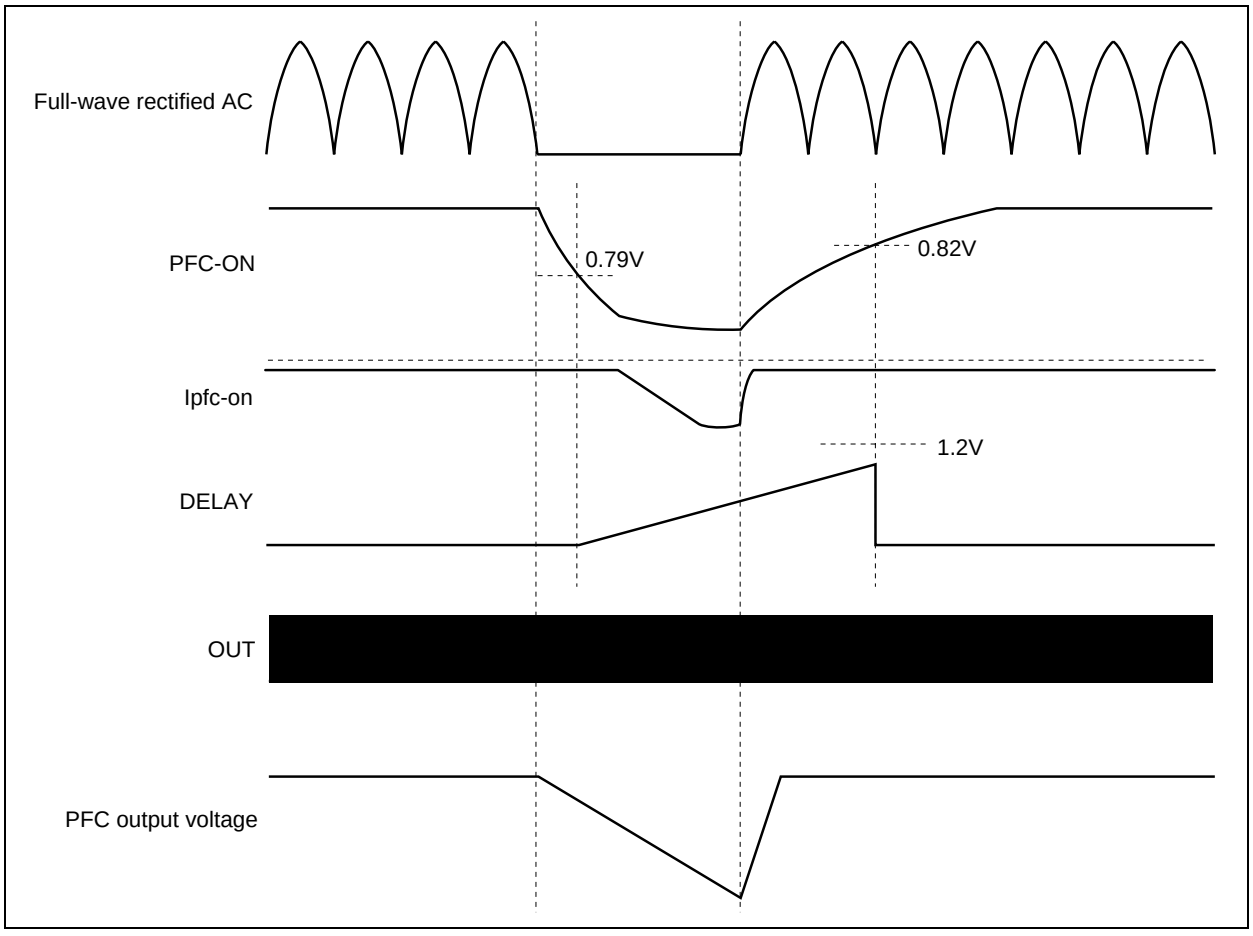


Figure 6 PFC Hold Function Operation Waveform 1

The hold time for PFC operation is adjusted by the value of the capacitance on the DELAY pin. Note, however, that if VCC voltage of the IC is not normally supplied during a momentary outage, the PFC-ON hold function does not operate.

(2) When the Momentary Outage is Long

When the momentary outage is long enough that the DELAY pin voltage reaches 1.2 V, OUT is stopped and SS is reset, then PFC operation is stopped. The current on the PFC-ON pin switches from source current to sink current and the voltage on the PFC-ON pin falls. When the supply of AC voltage resumes, the IC is restarted in a soft-start operation.

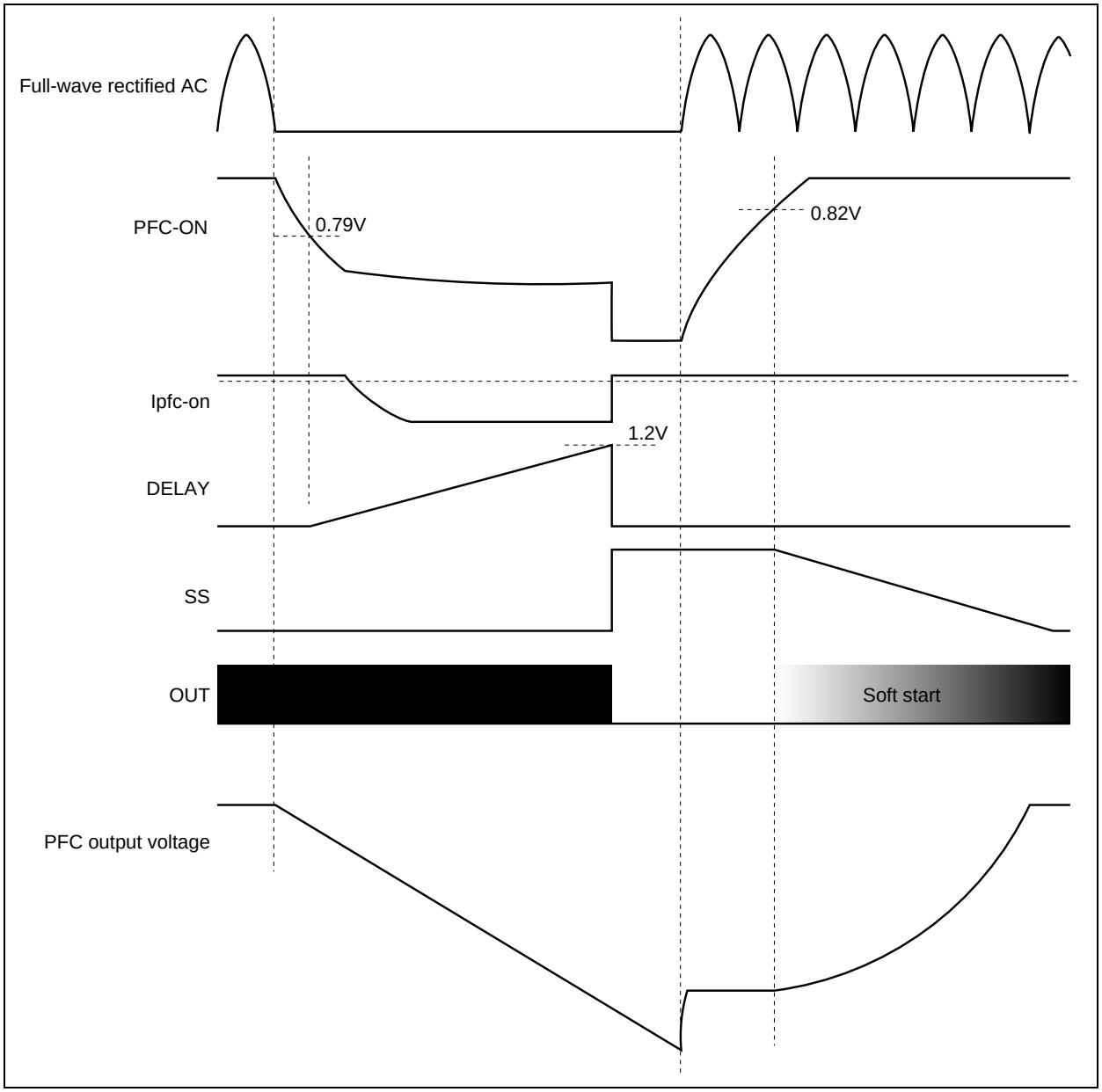


Figure 7 PFC Hold Function Operation Waveform 2

Note: When the PFC output voltage is driving a heavy load, the PFC output voltage falls rapidly, and the FB pin may fall below 0.52 V before the DELAY pin reaches 1.2 V. Here, the OUT pin is stopped, and the SS pin is reset by the FB pin low-voltage detection circuit.

5. FB Pin Function

The FB pin is a feedback input for the PFC output voltage. This pin is applied to voltage divided PFC output with resistors. The PFC output voltage is controlled so that the voltage on FB becomes 2.5 V. The FB pin function provides protection against abnormal PFC output voltages. The protective functions include overvoltage detection and low-voltage detection. These functions do not operate when VREF voltage is lower than 4 V as UVL operation and shutdown state.

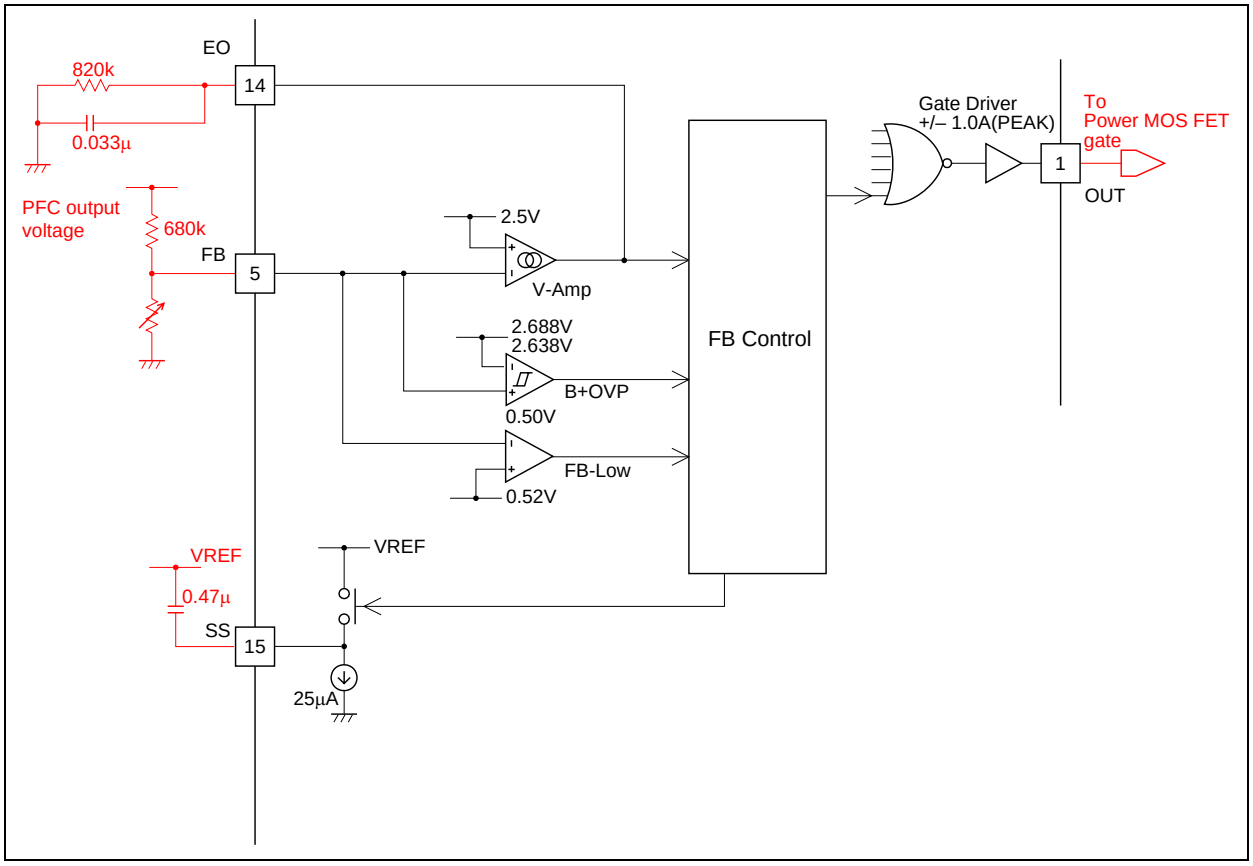


Figure 8 Internal Circuits Connected to the FB Pin

5-1. Power-Supply Startup Operation

When the AC voltage is applied, the PFC-ON pin voltage starts to rise up. After it has reached 0.82 V, the voltage on the SS pin starts to be discharged and PFC operation is started with the soft-start function. Once the PFC operation is started, the voltage on the FB pin rises and is controlled so that it reaches 2.5 V.

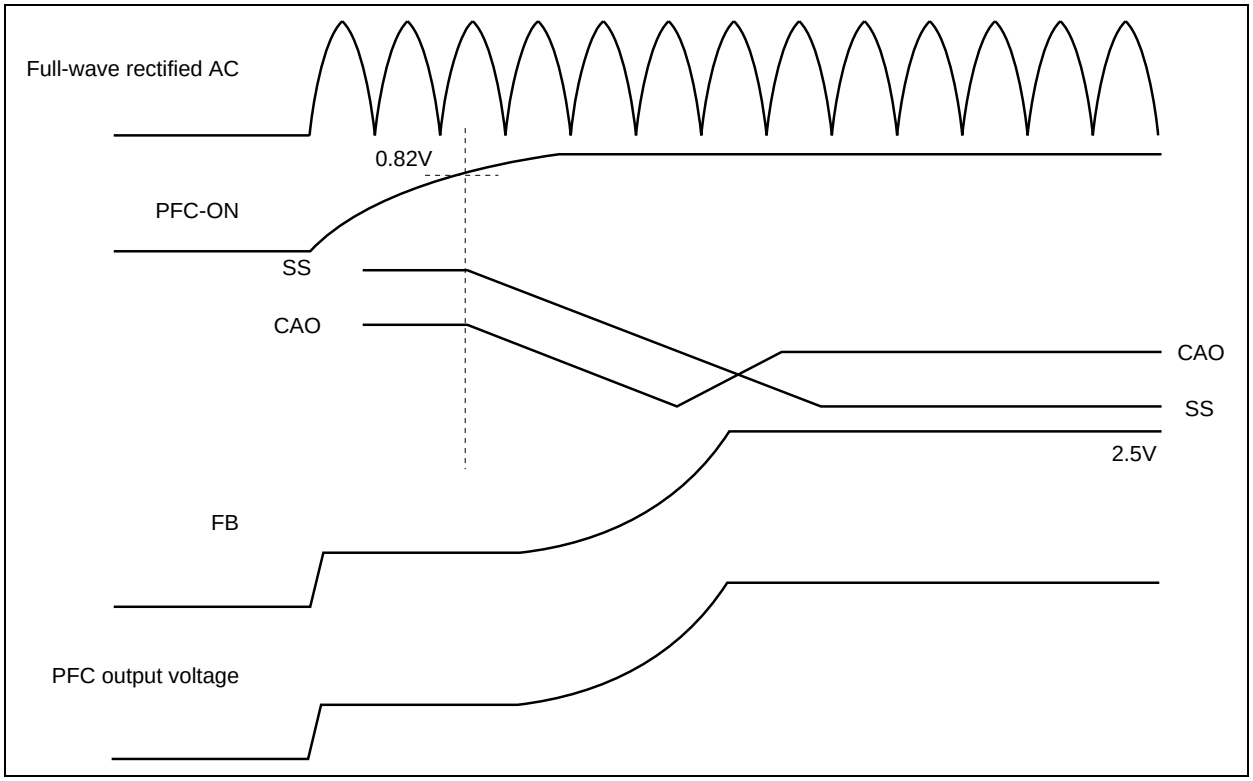


Figure 9 Waveform in Startup Operation

5-2. Operation when the Power-Supply Stops

When the supply of AC voltage stops, both of the PFC output voltage and the voltage on the FB pin fall. When the voltage on the FB pin is lower than 0.52 V, the PFC operation stops and the SS pin is reset.

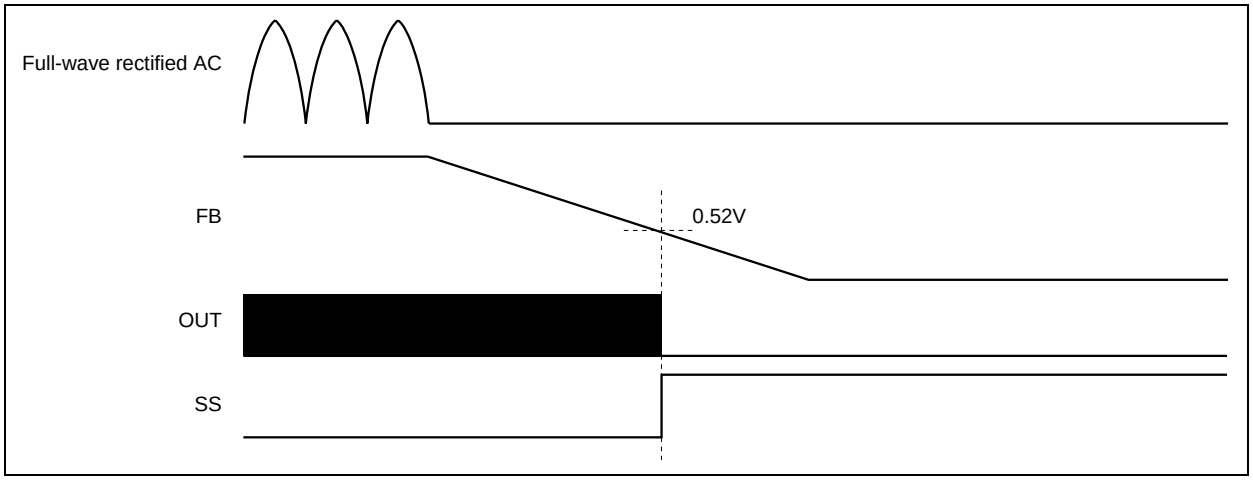


Figure 10 Waveform in Stop Operation

Note: When the PFC output voltage is driving light load, the PFC output voltage falls slowly, and the PFC-hold function may be activated before the voltage on the FB pin falls to 0.52 V. In this case, the PFC hold function operates, stopping output on the OUT pin and resetting the SS pin.

5-3. Overvoltage Operation

When the PFC output voltage is larger than 7.5% of the prescribed voltage due to an abnormality in the system or a sudden change of AC voltage or load, operation of the OUT pin is stopped. When the PFC output voltage returns to within 5.5% of the prescribed voltage, operation of the OUT pin is resumed.

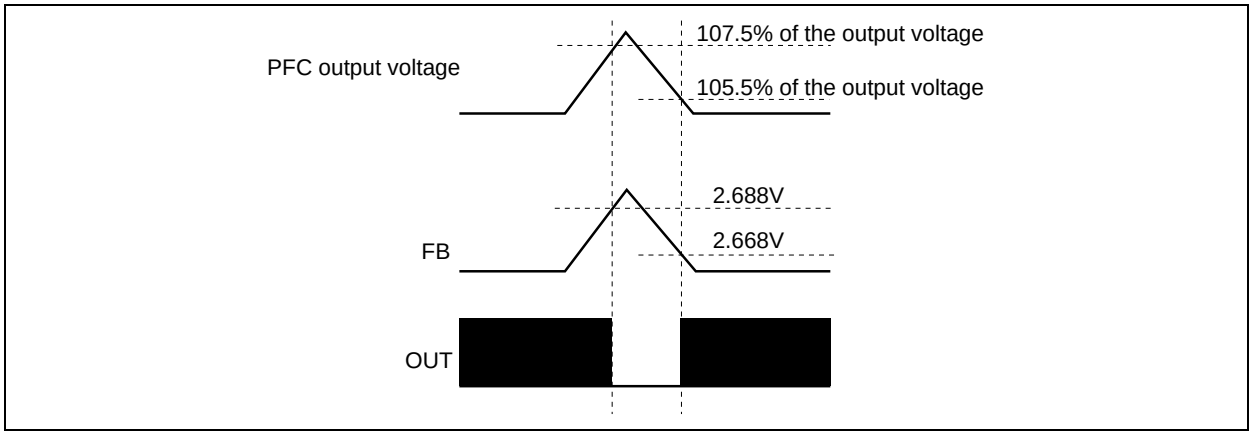


Figure 11 Waveform of Operation after Overvoltage detection by the FB Pin

6. IC Shutdown Function

When the DELAY pin is pulled up to 4 V, the IC shutdown function operates. During shutdown, the IC enters the standby state. To reset the circuit from the shutdown state, the voltage on VCC must be lowered to 4 V or less. After this reset, when the VCC pin voltage reaches 10.5 V, the IC is restarted.

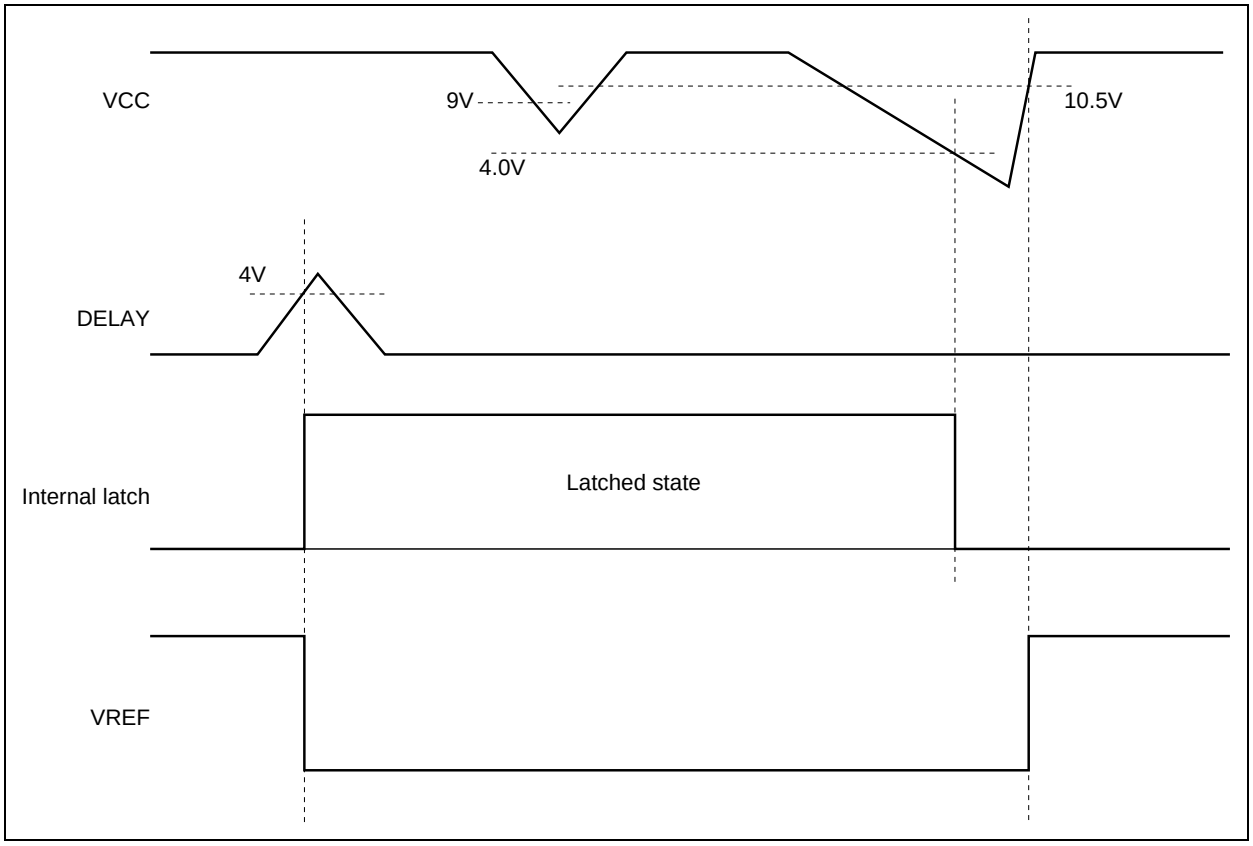
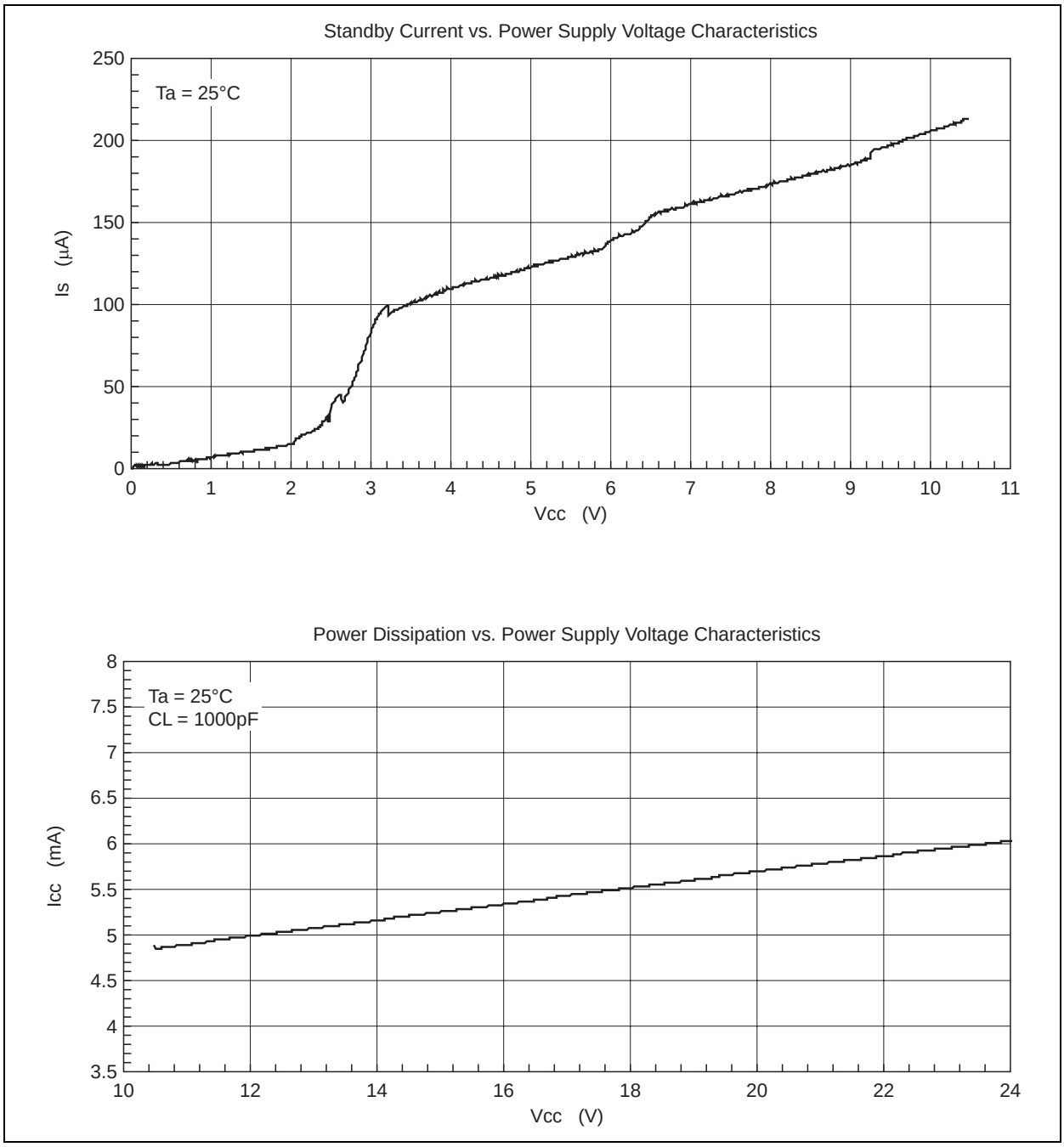
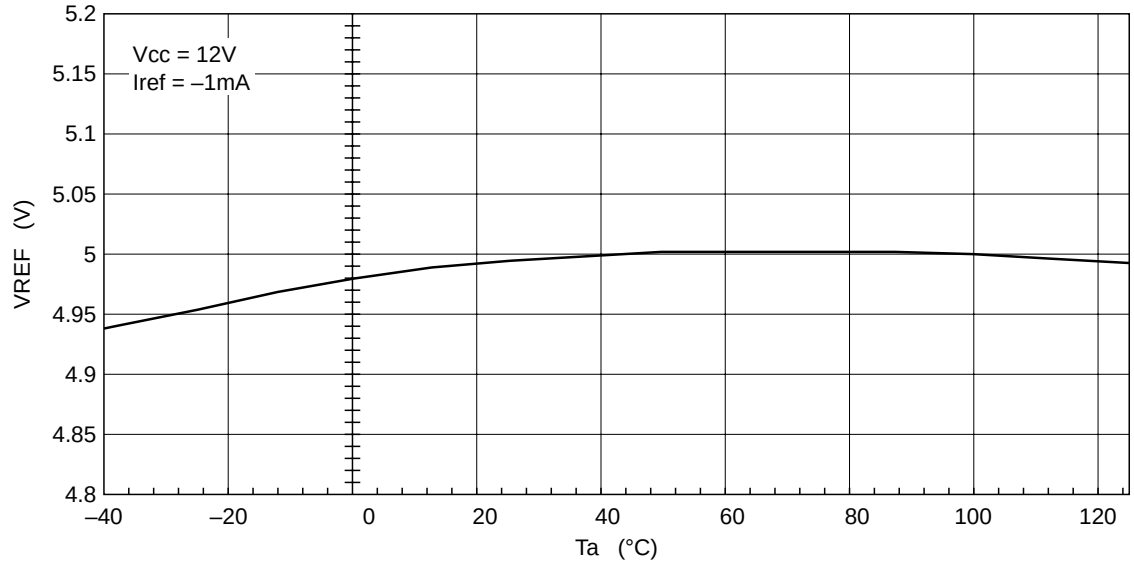


Figure 12 Waveform of Operation in IC Shutdown

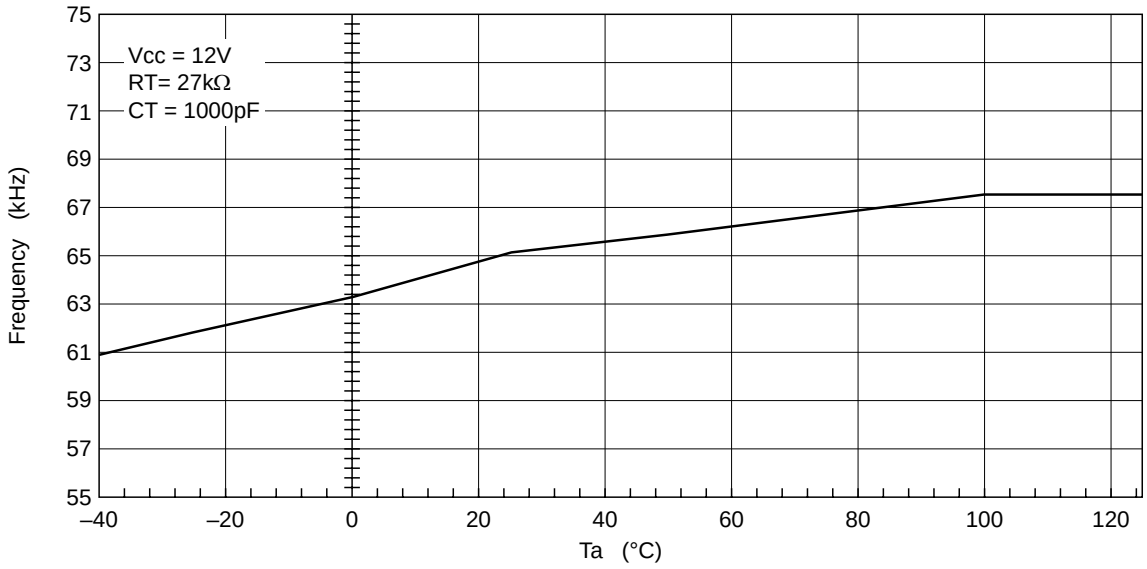
Main Characteristics

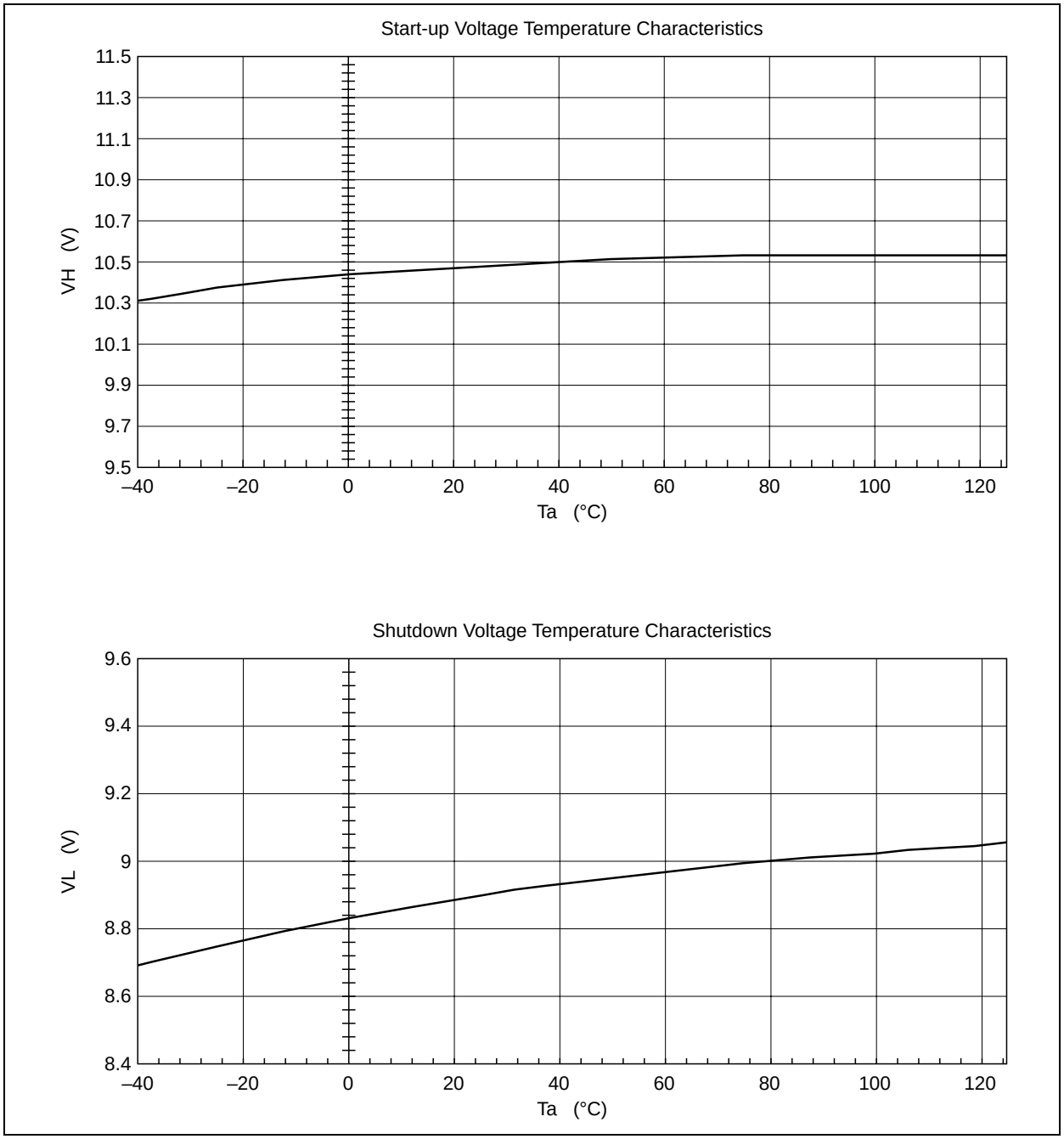


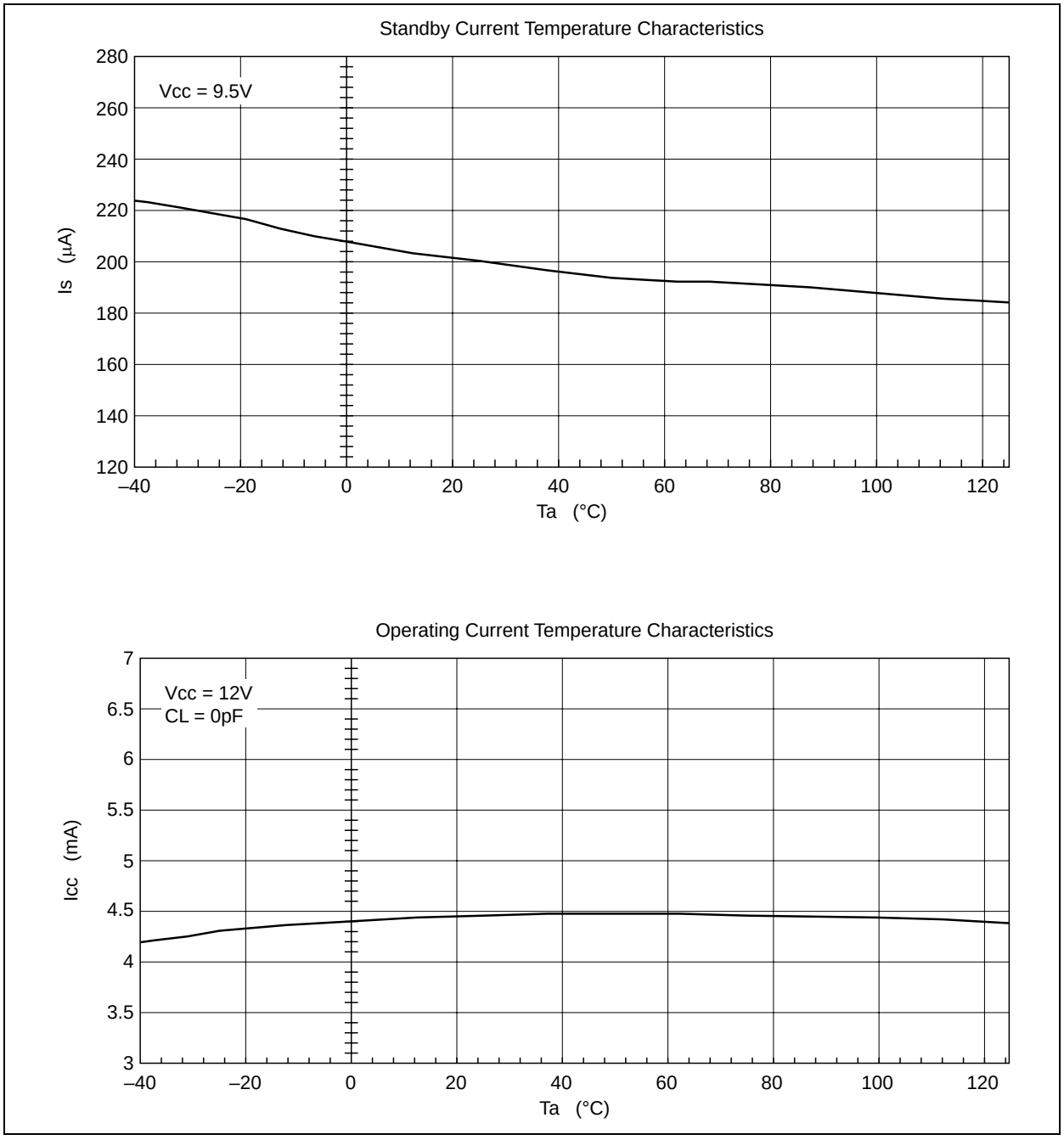
Reference Voltage Temperature Characteristics

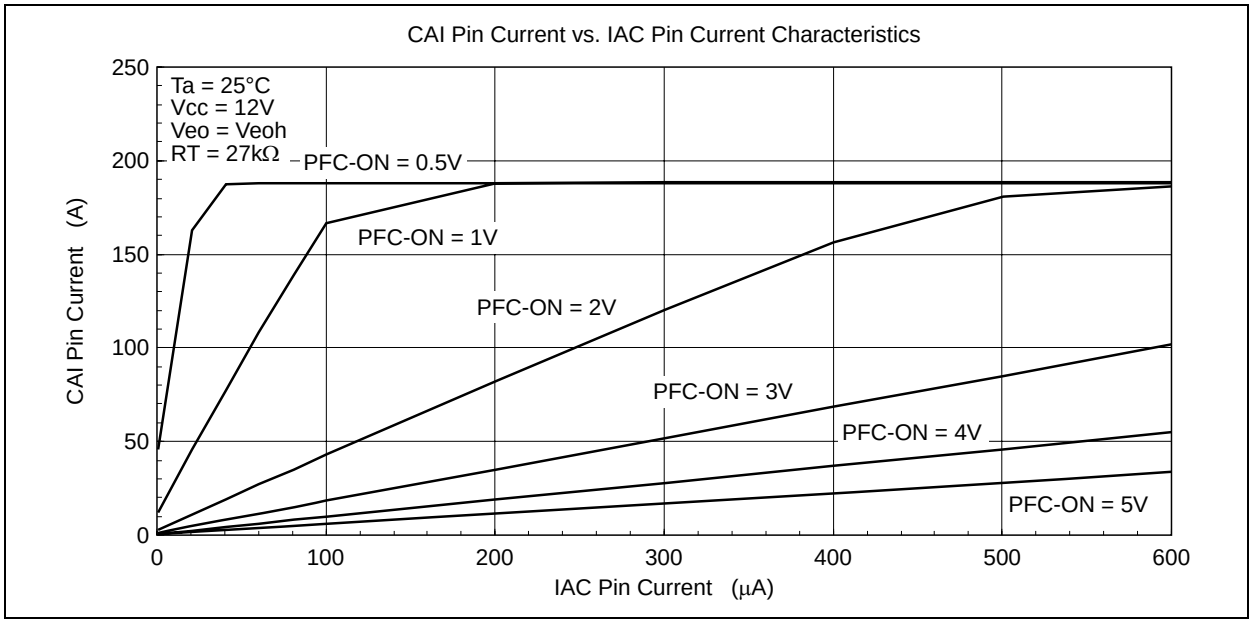


Operating Frequency Temperature Characteristics









Precautions on Usage

Figure 13 shows symbols which are used in this chapter.

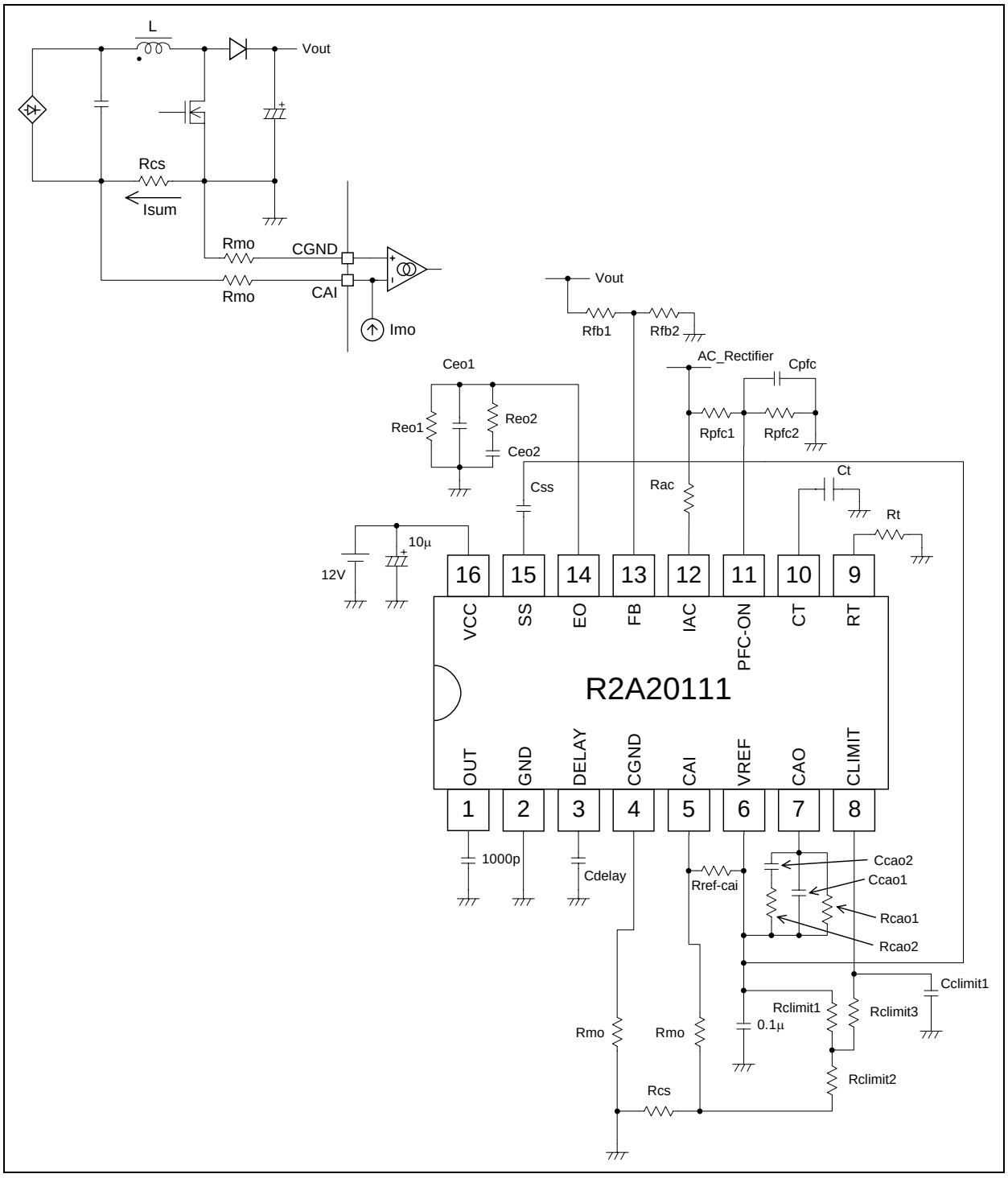


Figure 13 Template Illustrating Symbols of External Circuit Elements

1. Power Limit Function

1-1. Limited Power Value

When the load exceeds the rated load, the power is limited by the set power value and the IC enters the constant power control state. This indicates that the power is limited by nearly-constant power independent of the input AC voltage, compared to the conventional overcurrent detection circuit. The limited power value is determined by the values of external resistors and is expressed by the following equation:

$$P_{limit} = 1.74 \bullet \frac{R_{mo} \bullet (R_{pfc1} + R_{pfc2})^2}{R_{cs} \bullet R_{ac} \bullet R_{pfc2}^2}$$

This is the equation for reference only. Be sure to sufficiently confirm the operation by using the actual circuit board. The actual value may differ from the equation by conditions, but the trend indicated by the equation remains the same (For instance, as the amount of Rmo becomes large, the limited power value increases). Therefore, use the equation above for reference to fine-tune the resistance values.

1-2. Trend of Limited Power Value for Input AC Voltage

Although the limited power value is nearly constant with respect to the input AC voltage, it may be deviated to a certain degree from linearity by conditions. When it has a negative slant with respect to the input AC voltage, add a resistor between the CAI pin and the VREF pin so that the deviation from linearity can be corrected to some degree.

1-3. Limit on Constant Power Function

After the PFC power supply enters the constant power operation state and load increases further, the PFC output voltage reaches about $\sqrt{2} \times$ input AC voltage. At this point the PFC output voltage is unable to fall below the point in principle of the boost converter. If the load increases further at this point, current increases on the peak part of input current, then the power starts increasing again. This current cannot be controlled by the IC.

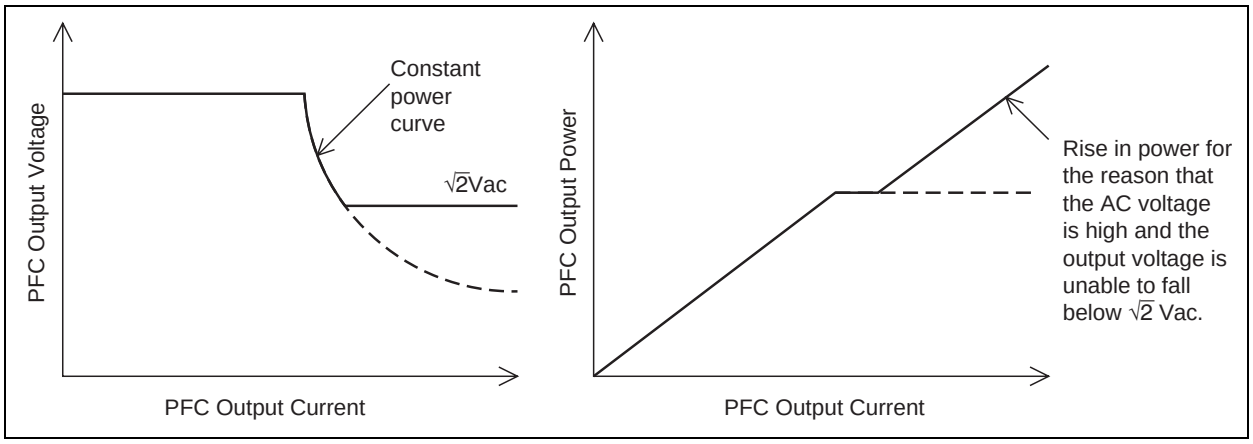


Figure 14 Outline of Constant Power Limit Function

1-4. Effects on Power Limit Characteristics of Resistor Rcao1 of CAO Pin

As the external resistance Rcao1 of the CAO pin is small, the limited power value decreases.

This decrease is caused by rise of the voltage on the EO pin in principle as Rcao1 becomes small. When the load becomes heavy and the voltage on the EO pin is clamped at the upper limit, the IC is operated in the power limit operation mode. Therefore, since the voltage on EO pin increases, the power limit value decreases relatively.

1-5. Relations between RT Resistor and Power Limit

The maximum current on the CAI pin is expressed in inverse proportion to the resistance of the RT pin as 4.7/RT.

Since Imo is proportional to the input AC current, when the value of AC voltage drops, Imo rises. Imo is, however, limited by the above maximum current value. If the value of Imo (max.) is set higher than the required current value with the minimum input AC voltage, the power limit function is operated in all range of input AC voltage without any difficulty. If the value of Imo (max.) is smaller than the required current, the rated power can not load (see figure 15).

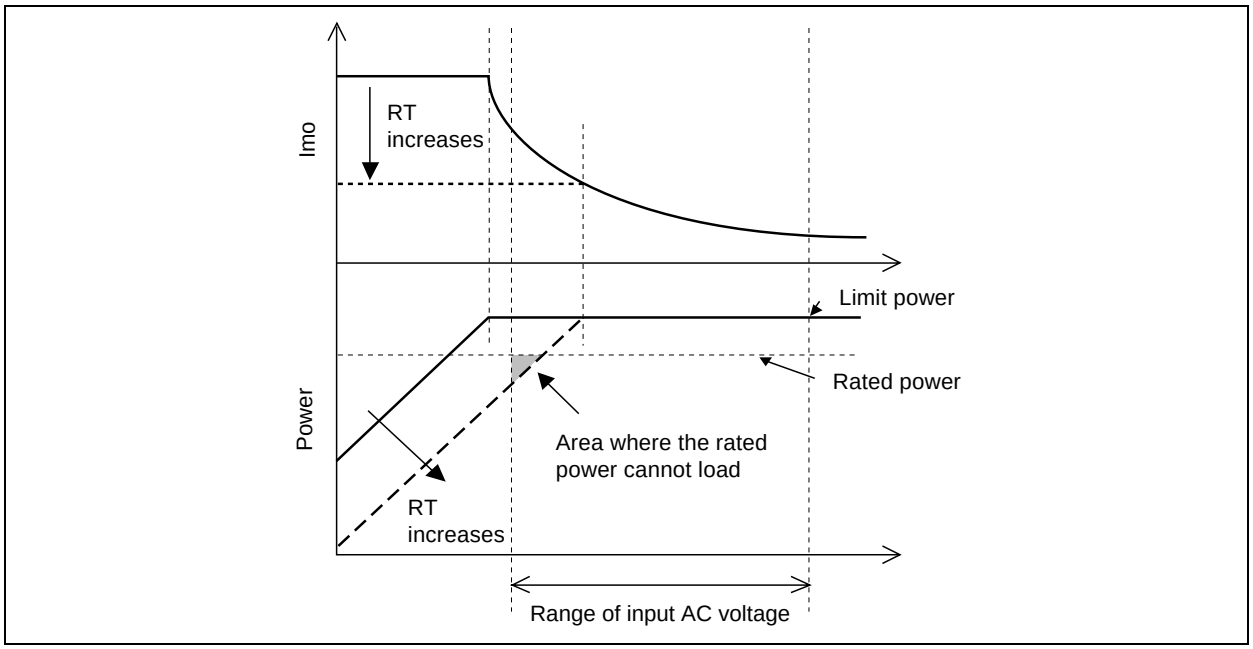


Figure 15 RT and Power Limit

In case of sudden turn from low AC voltage to high AC voltage as in return from a momentary outage or sag, the voltage on the PFC-ON pin changes after the AC voltage for its smoothing capacitance. Therefore, the voltage on the PFC-ON pin remains low while the AC voltage is high. In such a state, the current is controlled to increase transiently (see figure 16). The overcurrent detection circuit is operated due to this increase in current, and noise of an inductor may be generated. In this case, set the limitation on current by adjusting the RT pin resistance to prevent the operation of overcurrent detection circuit.

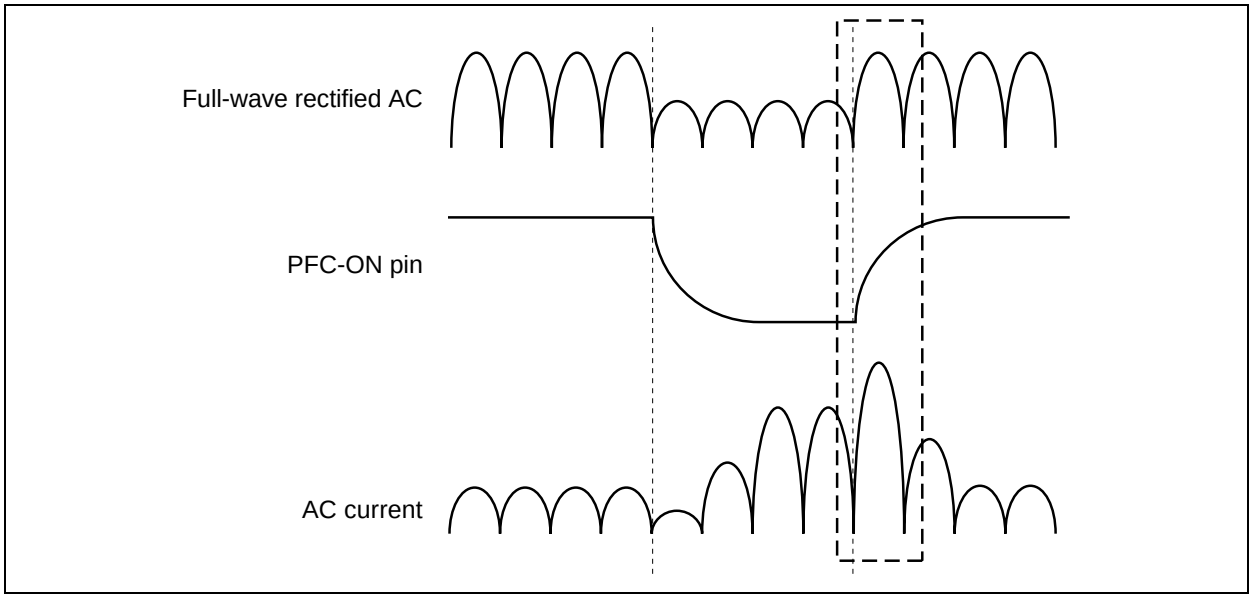


Figure 16 Increase in Current due to AC Voltage Sag

1-6. Tolerance of Limited Power Values

The tolerance of the limited power values depend on the tolerance of the CAI pin current. Since overcurrent detection value is constant, set the RT resistance as illustrated in figure 17, so that the resistance does not exceed the overcurrent detection level. Seen in figure 17, the key to select a switching device is not the tolerance in the limited power value but in the current value limited by RT. The tolerance of this current ranges from – 10% to + 10%.

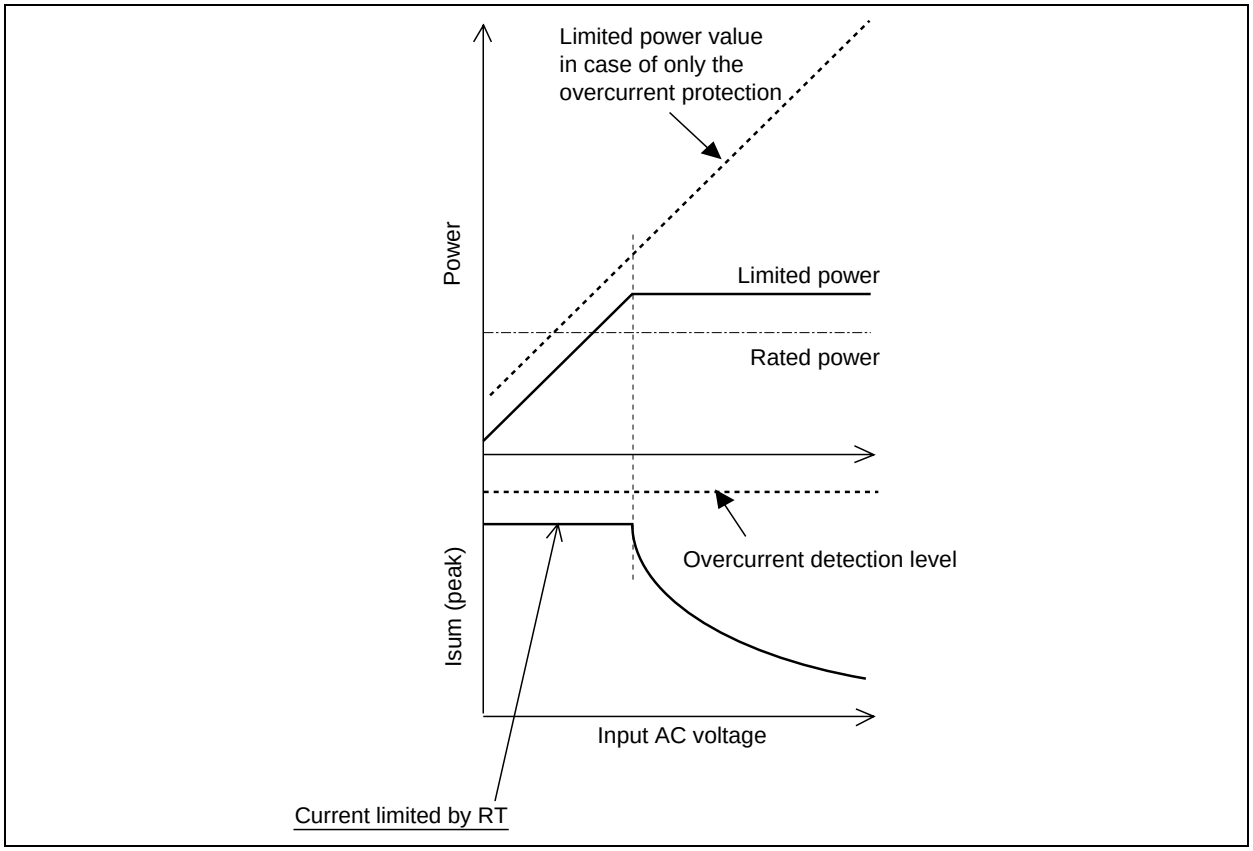


Figure 17 Overcurrent Detection Level and Power Limitation

2. Operation of PFC On/Off Function

PFC function of the R2A20111 can be turned on and off externally using the following methods.

(1) Pull down the voltage on the PFC-ON pin to the GND level.
(2) Pull up the voltage on the SS pin to the VREF voltage level.
(3) Pull down the voltage on the CLIMIT pin to 1.3 V or lower.
(4) Pull up the voltage on the DELAY pin to 4 V or more.

Since the voltage on the OUT pin is fixed to the GND level in each case, the boost operation is halted. The sections from 2-1 to 2-4 describe phenomena which may occur for functional reasons of the IC. Make sure to sufficiently confirm each operation using the actual the power-supply board. When the current flows transiently and noise of an inductor is generated, refer to section 1-5 “Relations between RT Resistor and Power Limit”.

2-1. On/Off Operation by Using the PFC-ON Pin

When the voltage on the PFC-ON pin drops, the IC controls to increase the AC current. Therefore, the AC current is controlled to increase while the voltage on the PFC-ON pin is pulled down. Furthermore, the PFC-ON pin has the PFC hold function. Since the PFC operation is not halted during the hold periods, the control current increases during this period (see figure 18). Also, when the PFC function is turned off in the light load, the output voltage may rise due to this increase current.

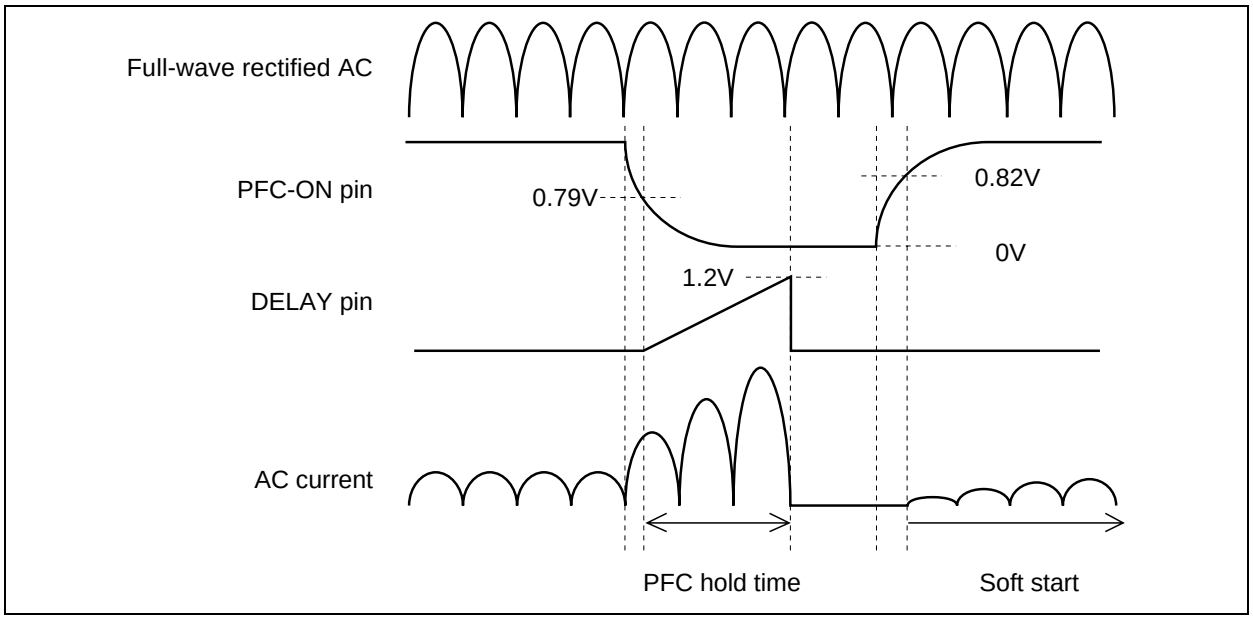


Figure 18 On/Off Operation by PFC-ON pin

2-2. On/Off Operation by Using the SS Pin

When the voltage on the SS pin is pulled up to the VREF voltage level, the voltage level of the CAO pin is also pulled up together with the SS pin. Then, the OUT pin is stopped.

After the voltage level of the SS pin is pulled up, a few pulses on the OUT pin may be generated by capacitance of the phase-compensation circuit of the CAO pin (see figure 19).

The circuit to directly pulls up the CAO pin is not recommended since the circuit may affect the phase-compensation circuit of the current amplifier.

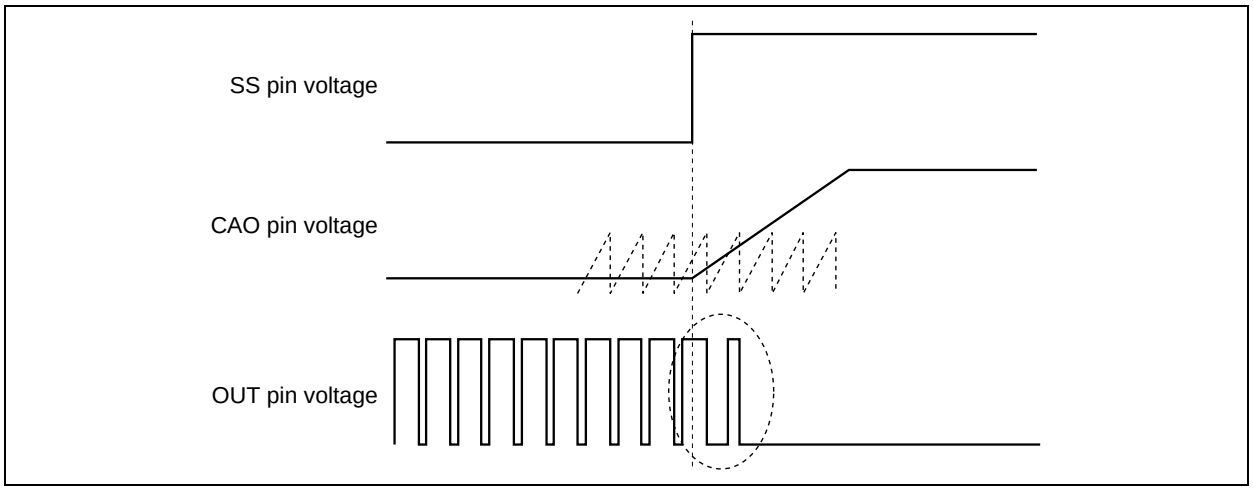


Figure 19 On/Off Operation by Pulling up SS Pin

2-3. On/Off Operation by using the CLIMIT Pin

When the voltage on the CLIMIT pin falls to 1.3 V or lower, the pulses on the OUT pin stop by the overcurrent detection circuit. When the voltage of the CLIMIT pin is released, the pulses on the OUT pin is resumed without soft start.

2-4. On/Off Operation by Using the DELAY Pin

When the voltage on the DELAY pin is pulled up to 4 V or more, the IC enters the shutdown state and the pulses on the OUT pin is stopped. Since the shutdown function is operated in latch mode, the IC is not resumed even when the voltage level of the DELAY pin is pulled down. The IC resumes only when lower the voltage on the VCC pin to 4 V or lower once and raise the voltage on the VCC pin higher than the UVL voltage.

Figure 20 illustrates an example of detection circuit.

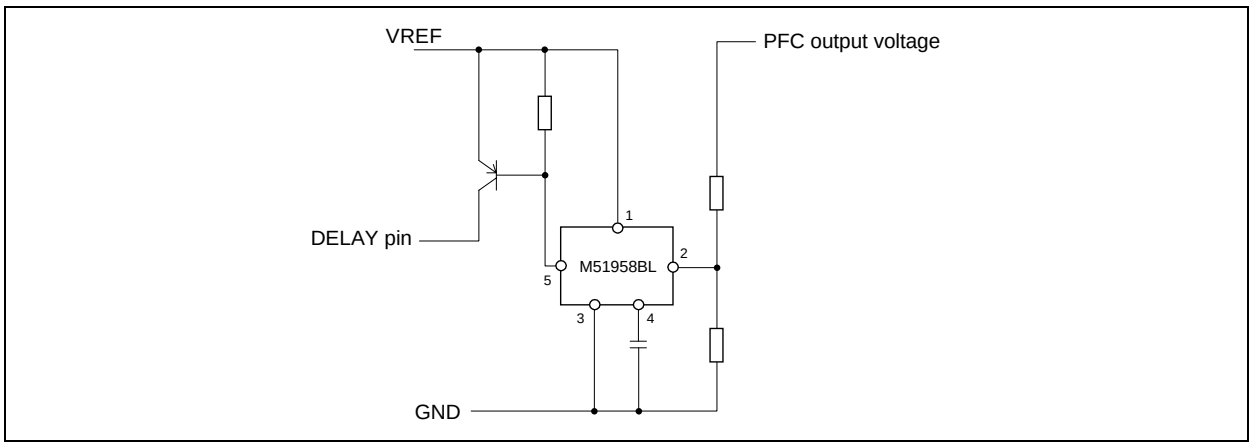


Figure 20 Example of Shutdown Circuit

3. Overcurrent Detection Circuit

When the RC filter is added the CLIMIT pin to prevent noise errors (see figure 21), the cut-off frequency shifts on the lower frequency side than the added RC filter because of the Rclimit 1 and Rclimit 2. This causes possibility that exactly current can not detect.

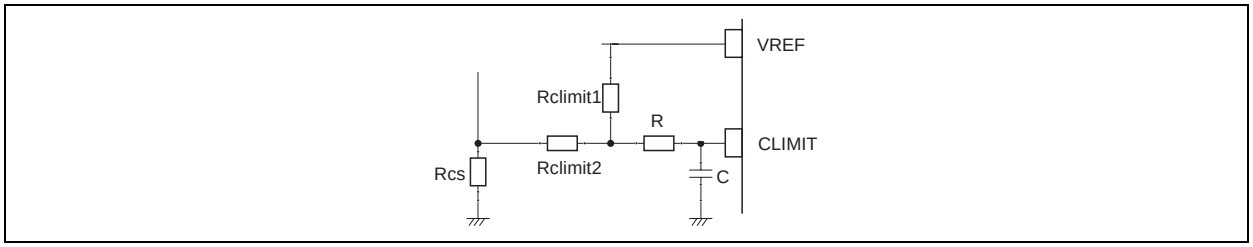


Figure 21 Example of CLIMIT Pin Filter

Since the overcurrent is detected by coil current, the detected current value is not the same as the peak value of the AC input current (see figure 22). Because of this difference, the overcurrent detection circuit is operated before the power reaches the constant power limit, and noise of an inductor may occur. In such a case, raise the overcurrent detection level.

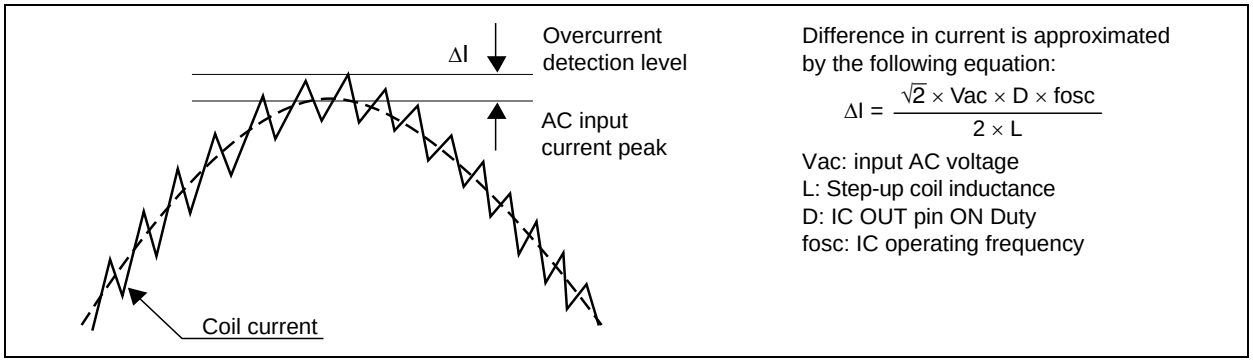


Figure 22 AC Input Current and Coil Current

4. PFC Hold Function

The PFC hold time can be adjusted by changing the value of the capacitor connected to the DELAY pin. The capacitance is charged with the source current from the IC and the PFC hold function is operated until the voltage on the DELAY pin reaches 1.2 V. Although the PFC-ON pin detects an occurrence of the momentary outage, the detection delay time occurs because a smoothing capacitor is connected to the PFC-ON pin. This delay time depends on the value of a resistor and the value of a smoothing capacitor which are connected to the PFC-ON pin. Therefore, the hold time is dependent on the following:

(a) Value of the capacitor connected to the DELAY pin
(b) Current value of the DELAY pin
(c) Values of the resistor and the capacitor connected to the PFC-ON pin

Actual PFC hold time thold is expressed in the following equation (see figure 23):

$$thold = t1 + t2 - t3$$

$$t1 = -R_{pfc2} \bullet C_{pfc} \bullet \ln\left(\frac{0.79^{V}}{V_{PFC\text{-}ON}}\right)$$

$$t2 + t3 = C_{DELAY} \bullet \frac{1.2^{V}}{I_{src\text{-}delay}}$$

$$t3 = -C_{pfc} \bullet \frac{R_{pfc1} \bullet R_{pfc2}}{R_{pfc1} + R_{pfc2}} \bullet \ln\left(\frac{0.82^{V} - \frac{2 \bullet \sqrt{2} \bullet V_{AC}}{\pi}}{0.4^{V} - \frac{2 \bullet \sqrt{2} \bullet V_{AC}}{\pi}}\right)$$

$$I_{src\text{-}delay} = \frac{4.7^{V}}{R_T}$$

$$V_{PFC\text{-}ON} = \frac{2 \bullet \sqrt{2} \bullet V_{AC}}{\pi} \bullet \frac{R_{pfc2}}{R_{pfc1} + R_{pfc2}}$$

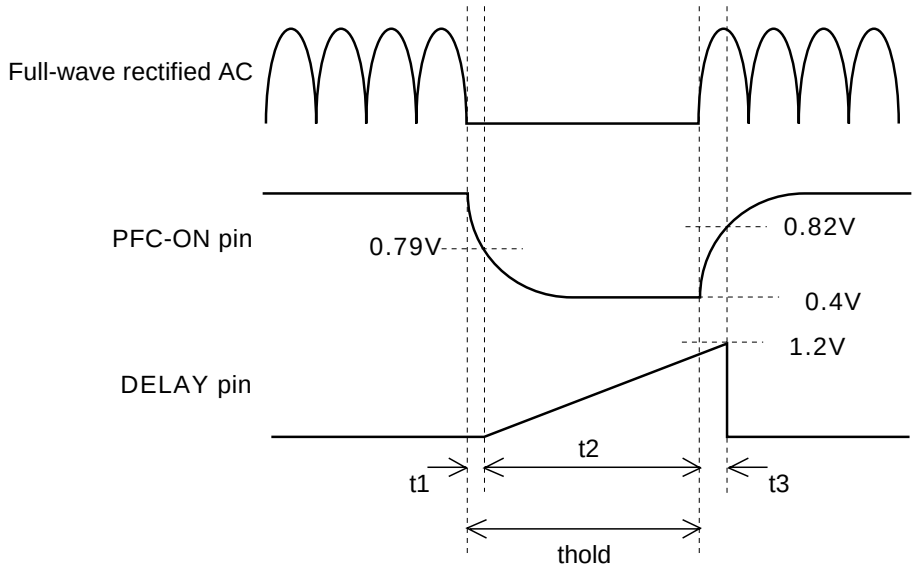


Figure 23 PFC Hold Time

5. Precautions on Pins

5-1. OUT Pin

Undershoot may occur on the PWM pulse of the OUT pin because of a parasitic inductance of wiring, etc. This undershoot (negative electric potential) may cause errors of the IC. In such a case, use a Schottky barrier diode, etc. to suppress the undershoot.

5-2. DELAY Pin

When the voltage on the DELAY pin reaches 4 V or more, the shutdown function is operated and the IC enters the shutdown state. Since the shutdown state is in latch mode, the IC is not resumed unless the voltage on the VCC pin is, once, lowered to 4 V or below.

When the PFC hold function is not used, lower the DELAY pin capacitance as possible. However, connect a capacitor with a few thousands pF or more capacitance to the DELAY pin so that the shutdown function will not be operated due to noise, etc. and note wiring pattern not to catch the noise.

5-3. CAI Pin and CLIMIT Pin

These pins are connected to a current detection resistor via a resistor. Provide a rush-current protection circuit, not to exceed the maximum rating because of the rush current at the startup of power supply.

5-4. VREF Pin

The voltage on the VREF pin is a reference voltage in the IC. For stabilizing the voltage on the VREF pin, be sure to connect a capacitor between the VREF pin and GND. However, in capacitance of a capacitor to be connected, overshoot may occur at the rising of the VREF pin (see figure 24). Pay special attention to this point when the voltage on the VREF pin is used as the power supply for an external circuit and a reference voltage.

Furthermore, note that the source current of the VREF pin will not exceed the maximum rating.

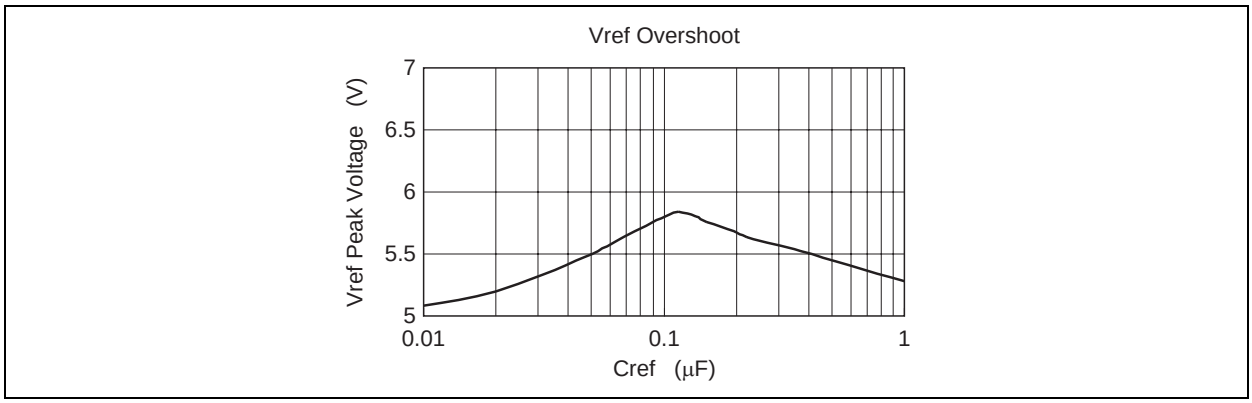
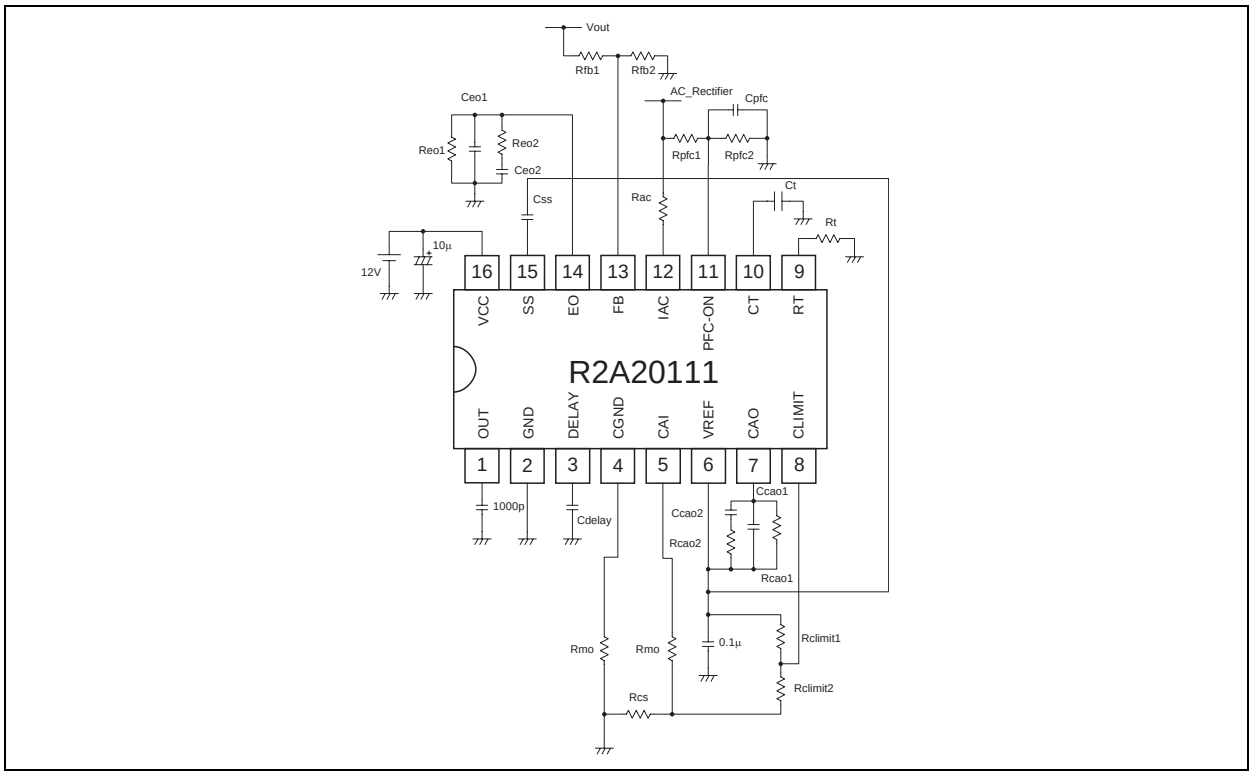


Figure 24 Overshoot Amount on VREF Pin (Reference Data)

6. Pattern Layout

In designing the pattern layout, pay as much attention as is possible to the following points.

(1) Place the IC pins (particularly, CGND, CAI, PFC-ON, IAC, FB) and their wiring as far from high-voltage switching lines (particularly the drain voltage for the power MOSFET) as possible and in general design the wiring to minimize switching noise.
(2) Wiring between CGND and Rcs via Rmo and wiring between CAI and RCS via Rmo connect nearly and separately to Rcs.
(3) It is probable that stability operation is achieved by inputting signals via low pass filter to CLIMIT, PFC-ON, IAC, FB terminal.
(4) Place a resistors and capacitors connect VREF , RT, CAO, CT, VCC as close to the IC as possible, and keep the wiring short.
(5) Pattern layout priority (for reference)
   1. Place the IC as far from high voltage switching lines as possible.
   2. The pattern of the GND should be as wide as possible.
   3. Place the stabilizing capacitor for VREF as close to the IC as possible.
   4. Place the stabilizing capacitor for VCC as close to the IC s possible.
   5. Place the resistors and capacitors (Rcao1, Rcao2, Ccao1, Ccao2) for CAO as close to the IC as possible.
   6. Wiring between CGND and Rcs via Rmo and Wiring between CAI and Rcs via Rmo connect nearly and separately to Rcs.
   7. Place the timing resistor for RT as close to the IC as possible.
   8. Place the timing capacitor for CT as close to the IC as possible.
   9. Place the resistors and capacitors (Reo1, Reo2, Ceo1, Ceo2) for EO as close to the IC as possible.
   10. Place the resistors and capacitors (Rpfc1, Rpfc2, Cpfc) for PFC-ON as close to the IC as possible.
   11. Place the resistors (Rfb1, Rfb2) for FB as close to the IC as possible.
   12. Place the resistors (Rac) for IAC as close to the IC as possible.
   13. Place the resistors (Rclimit1, Rclimit2) for CLIMIT as close to the IC as possible.
   14. Place the capacitor (Cdelay) for DELAY as close to the IC as possible.
   15. Place the capacitor (Css) for SS as close to the IC as possible.



(6) There is a potential that placing the heat sink between ICs and power MOSFET will be a some kind of shield and reduce the radiation noise (figure 25).

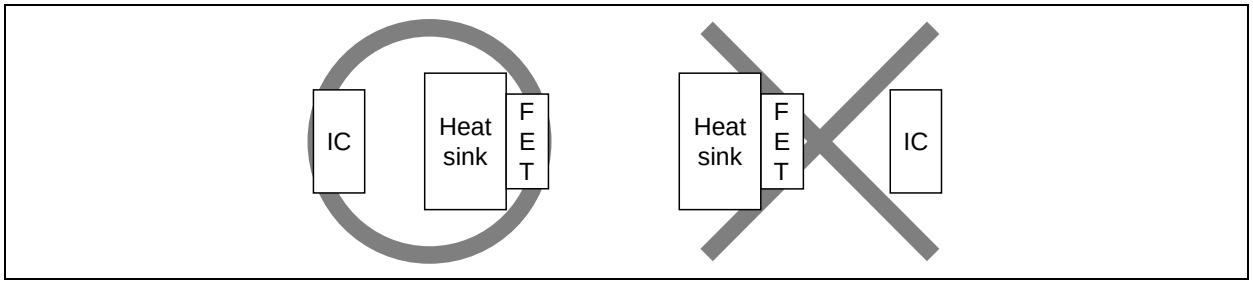
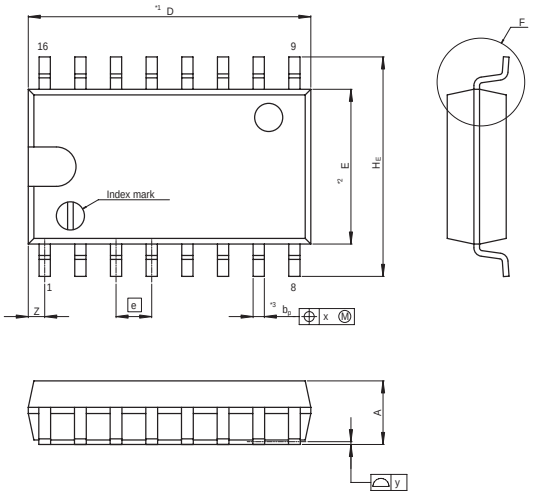
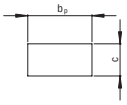


Figure 25 Example of Layout of Parts

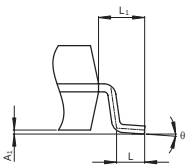
Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP16-5.5x10.06-1.27	PRSP0016DH-B	FP-16DAV	0.24g





Terminal cross section
(Ni/Pd/Au plating)

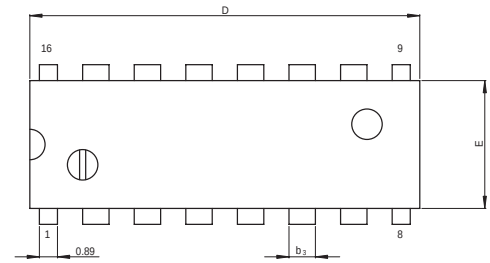


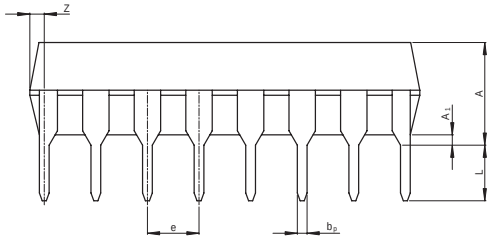
Detail F

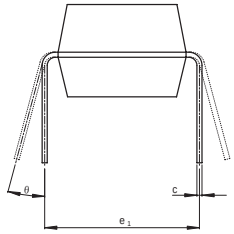
NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	10.06	10.5
E	—	5.50	—
A_2	—	—	—
A_1	0.00	0.10	0.20
A	—	—	2.20
b_p	0.34	0.40	0.46
b_1	—	—	—
c	0.15	0.20	0.25
c_1	—	—	—
θ	0°	—	8°
H_E	7.50	7.80	8.00
e	—	1.27	—
x	—	—	0.12
y	—	—	0.15
Z	—	—	0.80
L	0.50	0.70	0.90
L_1	—	1.15	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP16-6.3x19.2-2.54	PRDP0016AE-B	DP-16FV	1.05g







(Ni/Pd/Au plating)

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e_1	—	7.62	—
D	—	19.2	20.32
E	—	6.3	7.4
A	—	—	5.06
A_1	0.51	—	—
b_p	0.40	0.48	0.56
b_3	—	1.30	—
c	0.19	0.25	0.31
θ	0°	—	15°
e	2.29	2.54	2.79
Z	—	—	1.12
L	2.54	—	—

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

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Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.
Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510

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