HD404719/HD404439/ HD4074719

Description

The HD404719, HD404439, and HD4074719 are 4-bit single-chip microcomputers each incorporating five timers, two serial interfaces, an A/D converter, an input capture timer, and an output compare timer. Each also includes a 32.768-kHz oscillator and low-power dissipation modes. The HD404719 and HD404439 are mask ROM versions. The HD4074719 is a PROM version (ZTAT™ microcomputer), which can be programmed by a PROM programmer. The HD404719 has high-voltage pins, and the HD404439 has only standard pins.

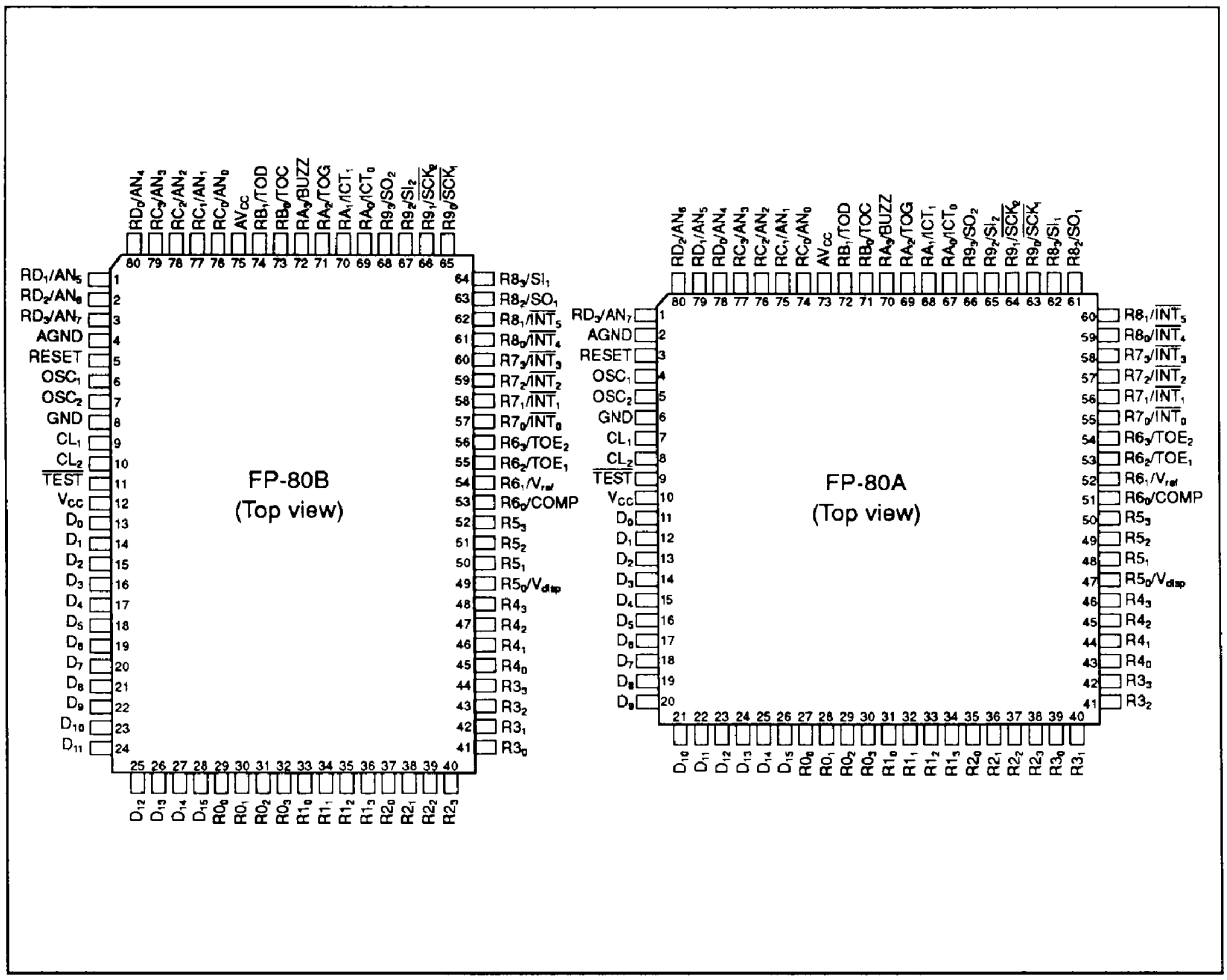
Features

- 16,384-word × 10-bit ROM (HD404719, HD404439)
  16,384-word × 10-bit PROM (HD4074719)
  ZTAT™ version is 27256-compatible
- 960-digit × 4-bit RAM
- 70 I/O pins including 36 high-voltage (40 V max.), high-current (15 mA max.) pins (except for HD404439 which has only standard pins)
- Five timer/counters
- Two 8-bit clock-synchronous serial interfaces
- 8-bit × 8-channel A/D converter
- Voltage comparator (with one input channel)
- Input capture timer/free-running counter
- 16-bit output compare timer
- Eight-level output buzzer line
- 14 interrupt sources
  — Six external sources, including three edge programmable type sources
  — Eight internal sources
- Subroutine stack up to 16 levels, including interrupts
- Four low-power dissipation modes
  — Subactive mode
  — Standby mode
  — Watch mode
  — Stop mode
- Built-in oscillator
  — Crystal or ceramic filter (external clock also enabled) main clock
  — 32.768-kHz crystal subclock
- Instruction cycle time: 0.89 µs (V_{CC} = 3.5 to 6 V), 1.78 µs (V_{CC} = 3.0 to 6 V)

Ordering Information

Type	Product Name	ROM (Words)	Package
Mask ROM	HD404719FS HD404439FS	16,384	FP-80B
	HD404719H HD404439H	16,384	FP-80A
ZTAT™	HD4074719FS	16,384	FP-80B
	HD4074719H	16,384	FP-80A

Pin Arrangement



Pin Description

Pin Number			Input/	Pin Number			Input/
FP-80B	FP-80A	Pin Name	Output	FP-80B	FP-80A	Pin Name	Output
1	79	RD_1/AN_5	I	34	32	$R1_1$	I/O
2	80	RD_2/AN_6	I	35	33	$R1_2$	I/O
3	1	RD_3/AN_7	I	36	34	$R1_3$	I/O
4	2	AGND		37	35	$R2_0$	I/O
5	3	RESET	I	38	36	$R2_1$	I/O
6	4	OSC_1	I	39	37	$R2_2$	I/O
7	5	OSC_2	O	40	38	$R2_3$	I/O
8	6	GND		41	39	$R3_0$	I/O
9	7	CL_1	I	42	40	$R3_1$	I/O
10	8	CL_2	O	43	41	$R3_2$	I/O
11	9	TEST	I	44	42	$R3_3$	I/O
12	10	V_{CC}		45	43	$R4_0$	I/O
13	11	D_0	I/O	46	44	$R4_1$	I/O
14	12	D_1	I/O	47	45	$R4_2$	I/O
15	13	D_2	I/O	48	46	$R4_3$	I/O
16	14	D_3	I/O	49	47	$R5_0/V_{disp}$	I
17	15	D_4	I/O	50	48	$R5_1$	I
18	16	D_5	I/O	51	49	$R5_2$	I
19	17	D_6	I/O	52	50	$R5_3$	I
20	18	D_7	I/O	53	51	$R6_0$/COMP	I/O
21	19	D_8	I/O	54	52	$R6_1/V_{ref}$	I/O
22	20	D_9	I/O	55	53	$R6_2/TOE_1$	I/O
23	21	D_{10}	I/O	56	54	$R6_3/TOE_2$	I/O
24	22	D_{11}	I/O	57	55	$R7_0/\overline{INT_0}$	I/O
25	23	D_{12}	I/O	58	56	$R7_1/\overline{INT_1}$	I/O
26	24	D_{13}	I/O	59	57	$R7_2/\overline{INT_2}$	I/O
27	25	D_{14}	I/O	60	58	$R7_3/\overline{INT_3}$	I/O
28	26	D_{15}	I/O	61	59	$R8_0/\overline{INT_4}$	I/O
29	27	$R0_0$	I/O	62	60	$R8_1/\overline{INT_5}$	I/O
30	28	$R0_1$	I/O	63	61	$R8_2/SO_1$	I/O
31	29	$R0_2$	I/O	64	62	$R8_3/SI_1$	I/O
32	30	$R0_3$	I/O	65	63	$R9_0/\overline{SCK_1}$	I/O
33	31	$R1_0$	I/O	66	64	$R9_1/\overline{SCK_2}$	I/O

Pin Description (cont)

Pin Number			Input/	Pin Number			Input/
FP-80B	FP-80A	Pin Name	Output	FP-80B	FP-80A	Pin Name	Output
67	65	$R9_2/SI_2$	I/O	74	72	RB_1/TOD	I/O
68	66	$R9_3/SO_2$	I/O	75	73	AV_{CC}	
69	67	RA_0/ICT_0	I/O	76	74	RC_0/AN_0	I
70	68	RA_1/ICT_1	I/O	77	75	RC_1/AN_1	I
71	69	RA_2/TOG	I/O	78	76	RC_2/AN_2	I
72	70	RA_3/BUZZ	I/O	79	77	RC_3/AN_3	I
73	71	RB_0/TOC	I/O	80	78	RD_0/AN_4	I

Pin Functions

Power Supply

V_{CC}: Apply power voltage to this pin.

GND: Connect to ground.

$\overline{TEST}$: Used for test purposes only. Connect it to V_{CC}.

RESET: Resets the MCU.

Oscillators

OSC_1, OSC_2: Used as pins for the internal oscillator circuit. They can be connected to a crystal resonator or a ceramic filter resonator, or OSC_1 can be connected to an external oscillator circuit.

CL_1, CL_2: Used for a 32.768-kHz crystal oscillator that acts as a clock.

Ports

D_0–D_{15} (D Port): Input/output port addressable by individual bits. Each port output consists of an open-drain PMOS which enables high-voltage, high-current drive ability for its pin.

R0–RD (R Ports): Input/output ports addressable in 4-bit units. R5, RC, and RD are input-only ports. The R5 to RD port pins are standard pins, but the R0 to R4 pins are high-voltage pins. Each of the R0 to R4 output pins consists of an open-drain PMOS which enables high-voltage drive ability for its pin. The R6 to RD pins are multiplexed with peripheral pins.

Interrupts

$\overline{INT}_0$–$\overline{INT}_5$: Input external interrupts to the MCU. $\overline{INT}_0$ to $\overline{INT}_5$ are multiplexed with $R7_0$ to $R7_3$ and $R8_0$ to $R8_1$, respectively.

Serial Communications Interface

$\overline{SCK}_1$, $\overline{SCK}_2$: Input/output SCI clock pins that are multiplexed with pins $R9_0$ and $R9_1$, respectively.

SI_1, SI_2: SCI receiving data input pins that are multiplexed with pins $R8_3$ and $R9_2$, respectively.

SO_1, SO_2: SCI transmission data output pins that are multiplexed with pins $R8_2$ and $R9_3$, respectively.

Timers

TOC, TOD: Output variable-duty square waves. They are multiplexed with pins RB_0 and RB_1, respectively.

TOE_1, TOE_2: Output square waves from the PWM. They are multiplexed with pins $R6_2$ and $R6_3$, respectively.

TOG: Outputs a square wave specified by the output compare function. It is multiplexed with pin RA_2.

Buzzer

Buzz: Outputs a variable-duty square wave. It is multiplexed with RA_3.

A/D Converter

AV_{CC}: V_{CC} power supply for the A/D converter.

AGND: GND power supply for the A/D converter.

AN_0–AN_7: Analog data input pins for A/D conversion that are multiplexed with pins RC_0 to RC_3 and RD_0 to RD_3, respectively.

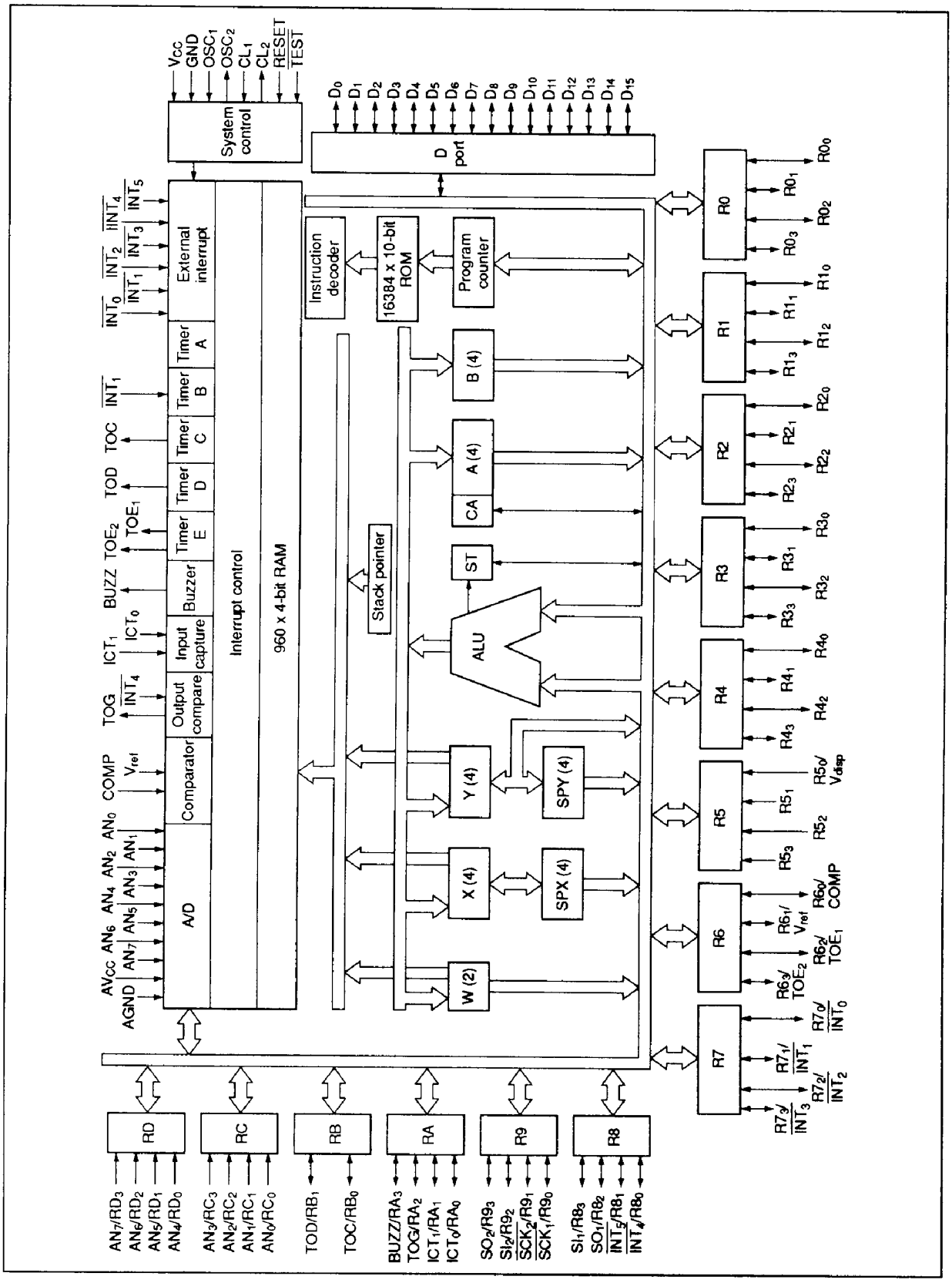
Comparator

COMP: Input pin for the comparator. It is multiplexed with pin $R6_0$.

V_{ref}: Inputs reference voltage for the analog comparator. It is multiplexed with pin $R6_1$.

Note: The HD404439 has only standard pins.

Block Diagram



Memory Map

ROM Memory Map

The ROM memory map is shown in figure 1, and the ROM is described in detail below.

Vector Address Area ($0000–$001F): Reserved for JMPL instructions that branch to the start addresses of the reset and interrupt routines. After an MCU reset or interrupt execution, the program starts from the vector address.

Zero-Page Subroutine Area ($0000–$003F): Reserved for subroutines. The program branches to the subroutine in this area in response to the CAL instruction.

Pattern Area ($0000–$0FFF): Reserved for ROM data that is referenced as a pattern by the P instruction.

Program Area ($0000–$3FFF): Used for program code.

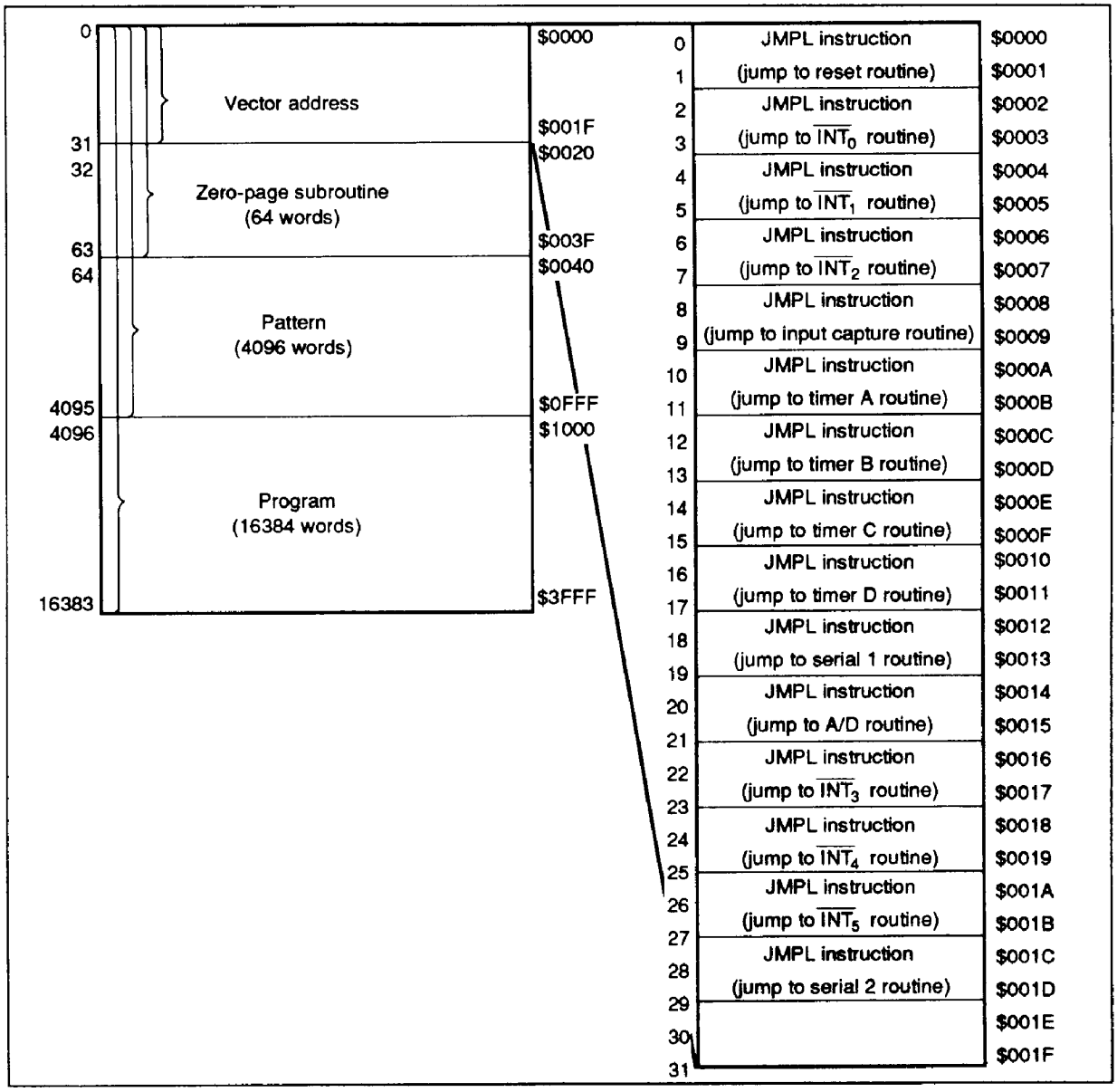


Figure 1 ROM Memory Map

RAM Memory Map

The MCU contains a 960-digit × 4-bit RAM area for data and stack areas. In addition, interrupt control bits and special function registers are mapped onto the same RAM memory space outside this area. The RAM memory map is shown in figure 2 and the RAM area is described in detail below.

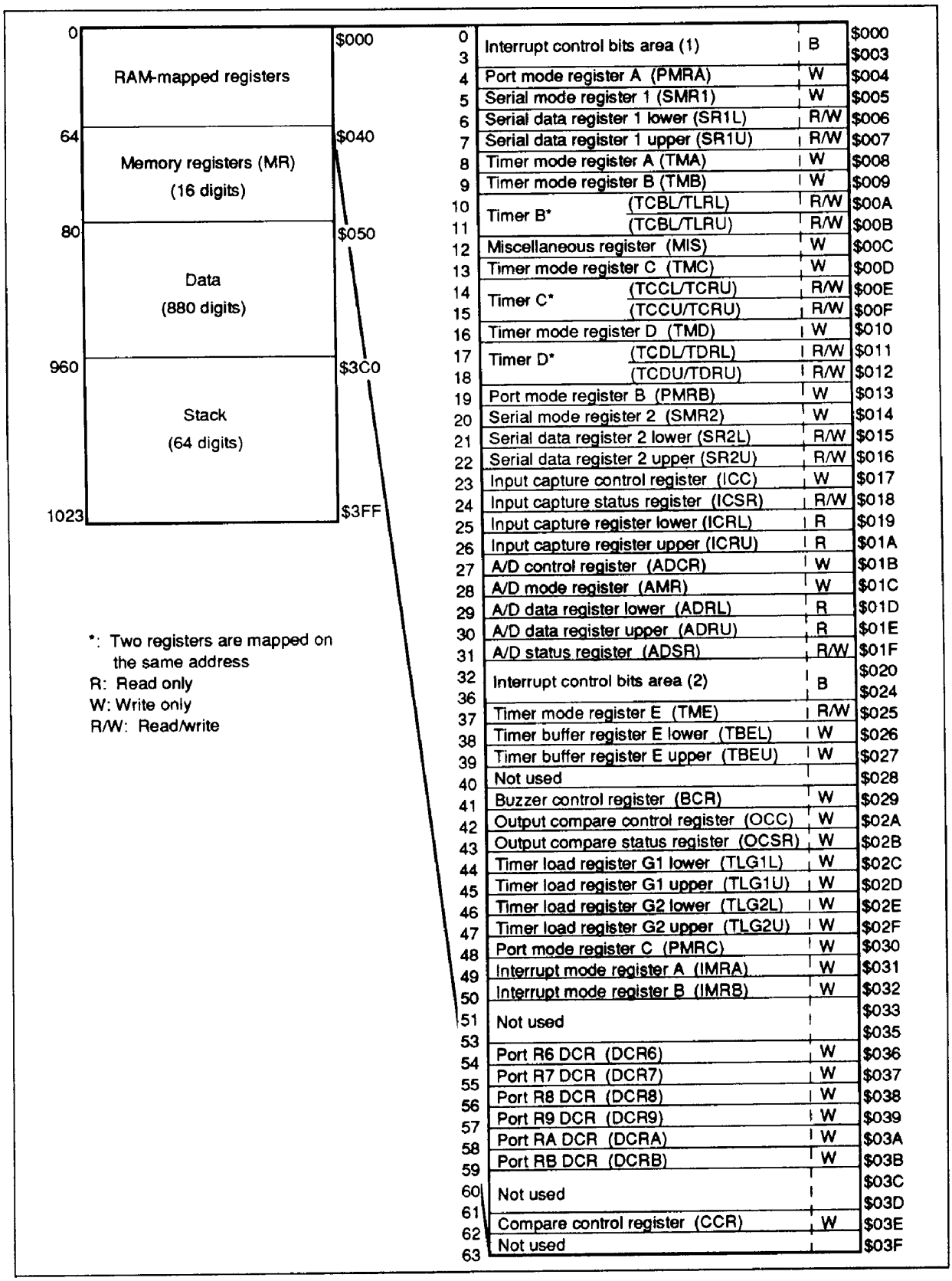
Interrupt Control Bits Area ($000–$003, $020–$024) : Used for interrupt control (figure 3). It can be accessed only by RAM bit manipulation instructions. However, note that the interrupt request flag cannot be set by software, the RSP bit is used only to reset the stack pointer, the DTON, LSON, and WDON flags are accessed only by RAM bit manipulation instructions, and the WDON flag can only be set to 1 by the SEM and SEMD instructions.

Special Function Registers Area ($004–$01F, $025–$03F): Used as mode registers for external interrupts, the serial interface, the timer/counters, and as data control registers and data registers for I/O ports. As shown in figure 2, there are three types of registers: read-only, write-only, and read/write. These registers cannot be accessed by RAM bit manipulation instructions.

Data Area ($040–$04F, $050–$3BF): The memory registers (MR), which consist of 16 digits ($040–$04F), can also be accessed by the LAMR and XMRA instructions (figure 4).

Stack Area ($3C0–$3FF): Used for saving the contents of the program counter (PC), status flag (ST), and carry flag (CA) at subroutine call (CAL or CALL instruction) and interrupt processing. This area can be used as a 16-level nesting subroutine stack in which one level requires four digits. The stack area and data to be saved in it are shown in figure 4.

The program counter is popped from the stack by the RTN and RTNI instructions. The status and carry flags can only be popped from the stack by the RTNI instruction. Any unused area is available for data storage.



0	Interrupt control bits area (1)		B	$000
3				$003
4	Port mode register A (PMRA)		W	$004
5	Serial mode register 1 (SMR1)		W	$005
6	Serial data register 1 lower (SR1L)		R/W	$006
7	Serial data register 1 upper (SR1U)		R/W	$007
8	Timer mode register A (TMA)		W	$008
9	Timer mode register B (TMB)		W	$009
10	Timer B*	(TCBL/TLRL)	R/W	$00A
11		(TCBL/TLRU)	R/W	$00B
12	Miscellaneous register (MIS)		W	$00C
13	Timer mode register C (TMC)		W	$00D
14	Timer C*	(TCCL/TCRU)	R/W	$00E
15		(TCCU/TCRU)	R/W	$00F
16	Timer mode register D (TMD)		W	$010
17	Timer D*	(TCDL/TDRL)	R/W	$011
18		(TCDU/TDRU)	R/W	$012
19	Port mode register B (PMRB)		W	$013
20	Serial mode register 2 (SMR2)		W	$014
21	Serial data register 2 lower (SR2L)		R/W	$015
22	Serial data register 2 upper (SR2U)		R/W	$016
23	Input capture control register (ICC)		W	$017
24	Input capture status register (ICSR)		R/W	$018
25	Input capture register lower (ICRL)		R	$019
26	Input capture register upper (ICRU)		R	$01A
27	A/D control register (ADCR)		W	$01B
28	A/D mode register (AMR)		W	$01C
29	A/D data register lower (ADRL)		R	$01D
30	A/D data register upper (ADRU)		R	$01E
31	A/D status register (ADSR)		R/W	$01F
32	Interrupt control bits area (2)		B	$020
36				$024
37	Timer mode register E (TME)		R/W	$025
38	Timer buffer register E lower (TBEL)		W	$026
39	Timer buffer register E upper (TBEU)		W	$027
40	Not used			$028
41	Buzzer control register (BCR)		W	$029
42	Output compare control register (OCC)		W	$02A
43	Output compare status register (OCSR)		W	$02B
44	Timer load register G1 lower (TLG1L)		W	$02C
45	Timer load register G1 upper (TLG1U)		W	$02D
46	Timer load register G2 lower (TLG2L)		W	$02E
47	Timer load register G2 upper (TLG2U)		W	$02F
48	Port mode register C (PMRC)		W	$030
49	Interrupt mode register A (IMRA)		W	$031
50	Interrupt mode register B (IMRB)		W	$032
51	Not used			$033
53				$035
54	Port R6 DCR (DCR6)		W	$036
55	Port R7 DCR (DCR7)		W	$037
56	Port R8 DCR (DCR8)		W	$038
57	Port R9 DCR (DCR9)		W	$039
58	Port RA DCR (DCRA)		W	$03A
59	Port RB DCR (DCRB)		W	$03B
60	Not used			$03C
61				$03D
62	Compare control register (CCR)		W	$03E
63	Not used			$03F

Figure 2 RAM Memory Map

	Bit 3	Bit 2	Bit 1	Bit 0	
0	IM0 (IM of $\overline{INT_0}$)	IF0 (IF of $\overline{INT_0}$)	RSP (Reset SP bit)	IE (Interrupt enable flag)	$000
1	IM2 (IM of $\overline{INT_2}$)	IF2 (IF of $\overline{INT_2}$)	IM1 (IM of $\overline{INT_1}$)	IF1 (IF of $\overline{INT_1}$)	$001
2	IMTA (IM of timer A)	IFTA (IF of timer A)	IMIC (IM of input capture)	IFIC (IF of input capture)	$002
3	IMTC (IM of timer C)	IFTC (IF of timer C)	IMTB (IM of timer B)	IFTB (IF of timer B)	$003
32	DTON (Direct transfer on flag)		WDON (Watchdog on flag)	LSON (Low speed on flag)	$020
33	IMS1 (IM of serial 1)	IFS1 (IF of serial 1)	IMTD (IM of timer D)	IFTD (IF of timer D)	$021
34	IM3 (IM of $\overline{INT_3}$)	IF3 (IF of $\overline{INT_3}$)	IMAD (IM of A/D)	IFAD (IF of A/D)	$022
35	IM5 (IM of $\overline{INT_5}$)	IF5 (IF of $\overline{INT_5}$)	IM4 (IM of $\overline{INT_4}$)	IF4 (IF of $\overline{INT_4}$)	$023
36			IMS2 (IM of serial 2)	IFS2 (IF of serial 2)	$024

IF: Interrupt request flag
IM: Interrupt mask
IE: Interrupt enable flag
SP: Stack pointer

Note: Bits in the interrupt control bits area and register flag area are set by the SEM or SEMD instruction, reset by the REM or REMD instruction, and tested by the TM or TMD instruction. Other instructions have no effect.
However, note that the IF cannot be set by the SEM or SEMD instruction. If the RSP bit or a non-existent bit is tested by the TM or TMD instruction, its status is undefined.
The WDON flag can only be used by the SEM or SEMD instruction (it is reset only by MCU reset).

Figure 3 Configuration of Interrupt Control Bits and Register Flag Areas

Memory registers			Stack area		
64	MR (0)	$040	960 Level 16		$3C0
65	MR (1)	$041	Level 15		
66	MR (2)	$042	Level 14		
67	MR (3)	$043	Level 13		
68	MR (4)	$044	Level 12		
69	MR (5)	$045	Level 11		
70	MR (6)	$046	Level 10		
71	MR (7)	$047	Level 9		
72	MR (8)	$048	Level 8		
73	MR (9)	$049	Level 7		
74	MR (10)	$04A	Level 6		
75	MR (11)	$04B	Level 5		
76	MR (12)	$04C	Level 4		
77	MR (13)	$04D	Level 3		
78	MR (14)	$04E	Level 2		
79	MR (15)	$04F	1023 Level 1		$3FF

	Bit 3	Bit 2	Bit 1	Bit 0	
1020	ST	$\overline{PC_{13}}$	$\overline{PC_{12}}$	$\overline{PC_{11}}$	$3FC
1021	$\overline{PC_{10}}$	$\overline{PC_9}$	$\overline{PC_8}$	$\overline{PC_7}$	$3FD
1022	CA	$\overline{PC_6}$	$\overline{PC_5}$	$\overline{PC_4}$	$3FE
1023	$\overline{PC_3}$	$\overline{PC_2}$	$\overline{PC_1}$	$\overline{PC_0}$	$3FF

PC_{13}–PC_0: Program counter
ST: Status flag
CA: Carry flag

Figure 4 Configuration of Memory Registers and Stack Area, and Stack Position

Functional Description

Registers and Flags

The MCU has nine registers and two flags for CPU operations. They are shown in figure 5 and described below.

Accumulator (A), B Register (B): Four-bit registers used to hold results from the arithmetic logic unit (ALU) and to transfer data between memory, I/O, and other registers.

W Register (W), X Register (X), Y Register (Y): Two-bit (W) and four-bit (X and Y) registers used for indirect RAM addressing. The Y register is also used for D-port addressing.

SPX Register (SPX), SPY Register (SPY): Four-bit registers used to supplement the X and Y registers.

Carry Flag (CA): One-bit flag that stores any ALU overflow generated by an arithmetic operation. CA is also affected by the SEC, REC, ROTL, and ROTR instructions. A carry is pushed onto the stack during an interrupt, and popped from the stack by the RTNI instruction—but not by the RTN instruction.

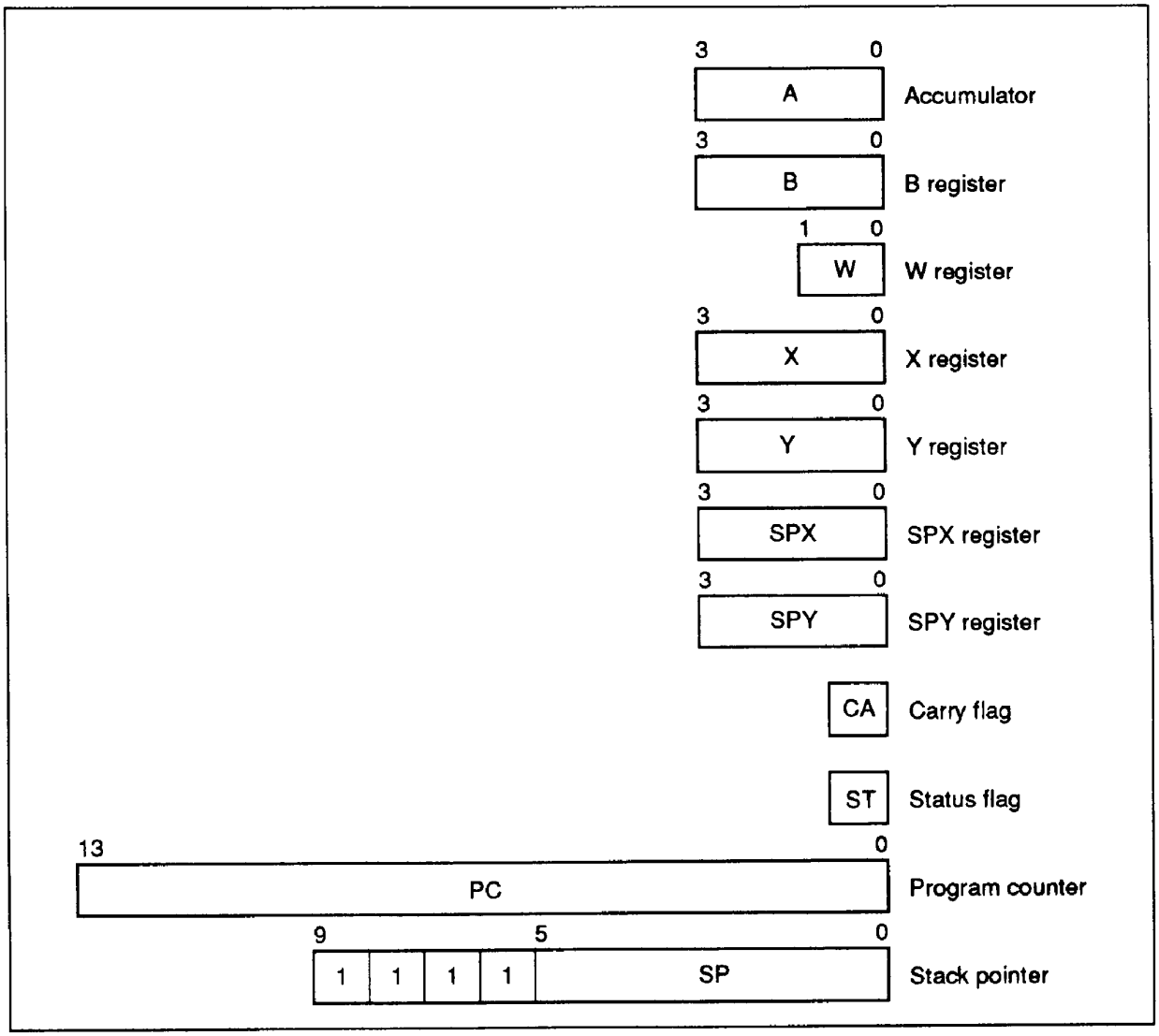


Figure 5 Registers and Flags

Status Flag (ST): One-bit flag that indicates an ALU overflow or ALU non-zero generated during an arithmetic or compare instruction, or the result of a bit test instruction. ST is used as a branch condition of the BR, BRL, CAL, and CALL instructions. The contents of ST remain unchanged until the next arithmetic, compare, or bit test instruction is executed, but become 1 after the BR, BRL, CAL, or CALL instruction is fetched, regardless of whether the instruction is executed or skipped. The contents of ST are pushed onto the stack during an interrupt, and popped from the stack by the RTNI instruction—but not by the RTN instruction.

Program Counter (PC): A 14-bit counter that points to the ROM address of the instruction being executed.

Stack Pointer (SP): Ten-bit pointer that contains the address of the stack area to be used next. The SP is initialized to $3FF by MCU reset. It is decremented by 4 when data is pushed onto the stack, and is incremented by 4 when data is popped from the stack. Since the top 4 bits of the SP are fixed to 1111, a stack of up to 16 levels can be used.

The SP is initialized to $3FF in two ways: by MCU reset or by resetting the RSP bit with the REM or REMD instruction.

Reset

The MCU is reset by setting the RESET pin high. At power-on or when stop mode is cancelled, RESET must be high for at least one t_{RC} to enable the oscillator to stabilize. In other cases, a RESET input for two instruction cycles resets the MCU.

Initial values of the registers and counters after MCU reset are listed in table 1.

Table 1 Initial Values after MCU Reset

Item		Abbr.	Initial Value	Contents
Program counter		(PC)	$0000	Indicates program execution point from start address of ROM area
Status flag		(ST)	1	Enables conditional branching
Stack pointer		(SP)	$3FF	Stack level 0
Interrupt flags/ mask	Interrupt enable flag	(IE)	0	Inhibits all interrupts
	Interrupt request flag	(IF)	0	Indicates there is no interrupt request
	Interrupt mask	(IM)	1	Prevents (masks) interrupt requests
I/O	Open-drain PMOS port data register	(PDR)	All bits 0	Enables output at level 0
	Standard port data register	(PDR)	All bits 1	Enables output at level 1
	Data control register	(DCR)	All bits 0	Turns output buffer off (to high impedance)
	Port mode register A	(PMRA)	0000	Refer to description of port mode register A
	Port mode register B	(PMRB)	0000	Refer to description of port mode register B
	Port mode register C	(PMRC)	0000	Refer to description of port mode register C
	Interrupt mode registers A, B	(IMRA, IMRB)	0000	Refer to description of interrupt mode registers A and B

Table 1 Initial Values after MCU Reset (cont)

Item		Abbr.	Initial Value	Contents
Timer/ counters, serial interface	Timer mode register A	(TMA)	0000	Refer to description of timer mode register A
	Timer mode register B	(TMB)	0000	Refer to description of timer mode register B
	Timer mode register C	(TMC)	0000	Refer to description of timer mode register C
	Timer mode register D	(TMD)	0000	Refer to description of timer mode register D
	Timer mode register E	(TME)	0000	Refer to description of timer mode register E
	Serial mode register 1	(SMR1)	0000	Refer to description of serial mode register 1
	Serial mode register 2	(SMR2)	0000	Refer to description of serial mode register 2
	Prescaler S		$000	—
	Prescaler W		$00	—
	Timer counter A	(TCA)	$00	—
	Timer counter B	(TCB)	$00	—
	Timer counter C	(TCC)	$00	—
	Timer counter D	(TCD)	$00	—
	Timer buffer register E	(TBE)	$00	Refer to description of timer buffer register E
	Timer load register B	(TLR)	$00	Refer to description of timer load register B
	Timer load register C	(TCR)	$00	Refer to description of timer load register C
	Timer load register D	(TDR)	$00	Refer to description of timer load register D
	Octal counter (× 2)		000	—
	Timer load register G	(TLG)	$0000	Refer to description of timer load register G
	A/D control register	(ADCR)	0000	Refer to description of A/D control register
	Input capture control register	(ICC)	0000	Refer to description of input capture control register
	Input capture data register	(ICSR)	0000	Refer to description of input capture data register
	Buzzer control register	(BCR)	0000	Refer to description of buzzer control register

Table 1 Initial Values after MCU Reset (cont)

Item		Abbr.	Initial Value	Contents
Timer/ counters, serial interface (cont)	Output compare control register	(OCC)	0000	Refer to description of output compare control register
	Output compare status register	(OCSR)	0000	Refer to description of output compare status register
	A/D status register	(ADSR)	0000	Refer to description of A/D status register
	A/D data register	(ADR)	$80	Refer to description of A/D data register
	16-bit counter (timer counter G)	(TCG)	$0000	—
	8-bit counter (timer counter F)	(TCF)	$00	—
	Compare control register	(CCR)	0000	Refer to description of output compare control register
Bit register	Low speed on flag	(LSON)	0	Refer to description of operating modes
	Watchdog timer on flag	(WDON)	0	Refer to description of timer C
	Direct transfer on flag	(DTON)	0	Refer to description of operating modes
Miscellaneous register		(MIS)	0000	Refer to description of miscellaneous register

Note: The status of other registers and flags after MCU reset are shown below.

Item	Abbr.	Status after Cancellation of Stop Mode by MCU Reset	In Other Cases at MCU Reset
Carry flag	(CA)	Pre-MCU-reset values are not retained: values must be initialized by software	Pre-MCU-reset values are not retained: values must be initialized by software
Accumulator	(A)		
B register	(B)		
W register	(W)		
X/SPX register	(X/SPX)		
Y/SPY register	(Y/SPY)		
Serial 1 data register	(S1R)		
Serial 2 data register	(S2R)		
RAM		Pre-MCU-reset (pre-STOP-instruction) values are retained	

Interrupts

The MCU has 14 interrupt sources: six external signals ($\overline{INT_0}$–$\overline{INT_5}$), four timer/counters (timer A, timer B, timer C, and timer D), two serial interfaces (serial 1 and serial 2), an A/D converter, and an input capture. An interrupt request flag (IF), interrupt mask (IM), and vector address are provided for each interrupt source, and an interrupt enable flag (IE) controls the entire interrupt process.

Interrupt Control Bits and Interrupt Processing: Locations \$000 through \$003 and \$020 through \$024 in RAM are reserved for the interrupt control bits which can only be accessed by RAM bit manipulation instructions. The interrupt request flags (IFs) can only be set by signals from interrupt sources. MCU reset initializes the interrupt enable flag (IE) and interrupt request flags (IFs) to 0 and the interrupt masks (IMs) to 1.

A block diagram of the interrupt control circuit is shown in figure 6, interrupt priorities and vector addresses are listed in table 2, and the interrupt processing conditions for the 14 interrupt sources are listed in table 3. An interrupt request occurs when the IF is set to 1 and the IM is set to 0. If the IE is 1 at that point, interrupt processing begins. A priority programmable logic array generates the vector address assigned to that interrupt source.

The interrupt processing sequence is shown in figure 7, and an interrupt processing flowchart is shown in figure 8. After an interrupt is acknowledged, the previous instruction is completed in the first cycle. The IE is reset in the second cycle, the carry flag, status flag, and program counter values are pushed onto the stack during the second and third cycles, and the program jumps to the vector address to execute the instruction in the third cycle.

Program the JMPL instruction at each vector address, to branch the program to the start address of the interrupt routine, and reset the IF by a software instruction within the interrupt routine.

Table 2 Vector Addresses and Interrupt Priorities

Reset/Interrupt	Priority	Vector Address
RESET	—	\$0000
$\overline{INT_0}$	1	\$0002
$\overline{INT_1}$	2	\$0004
$\overline{INT_2}$	3	\$0006
Input capture	4	\$0008
Timer A	5	\$000A
Timer B	6	\$000C
Timer C	7	\$000E
Timer D	8	\$0010
Serial 1	9	\$0012
A/D	10	\$0014
$\overline{INT_3}$	11	\$0016
$\overline{INT_4}$	12	\$0018
$\overline{INT_5}$	13	\$001A
Serial 2	14	\$001C

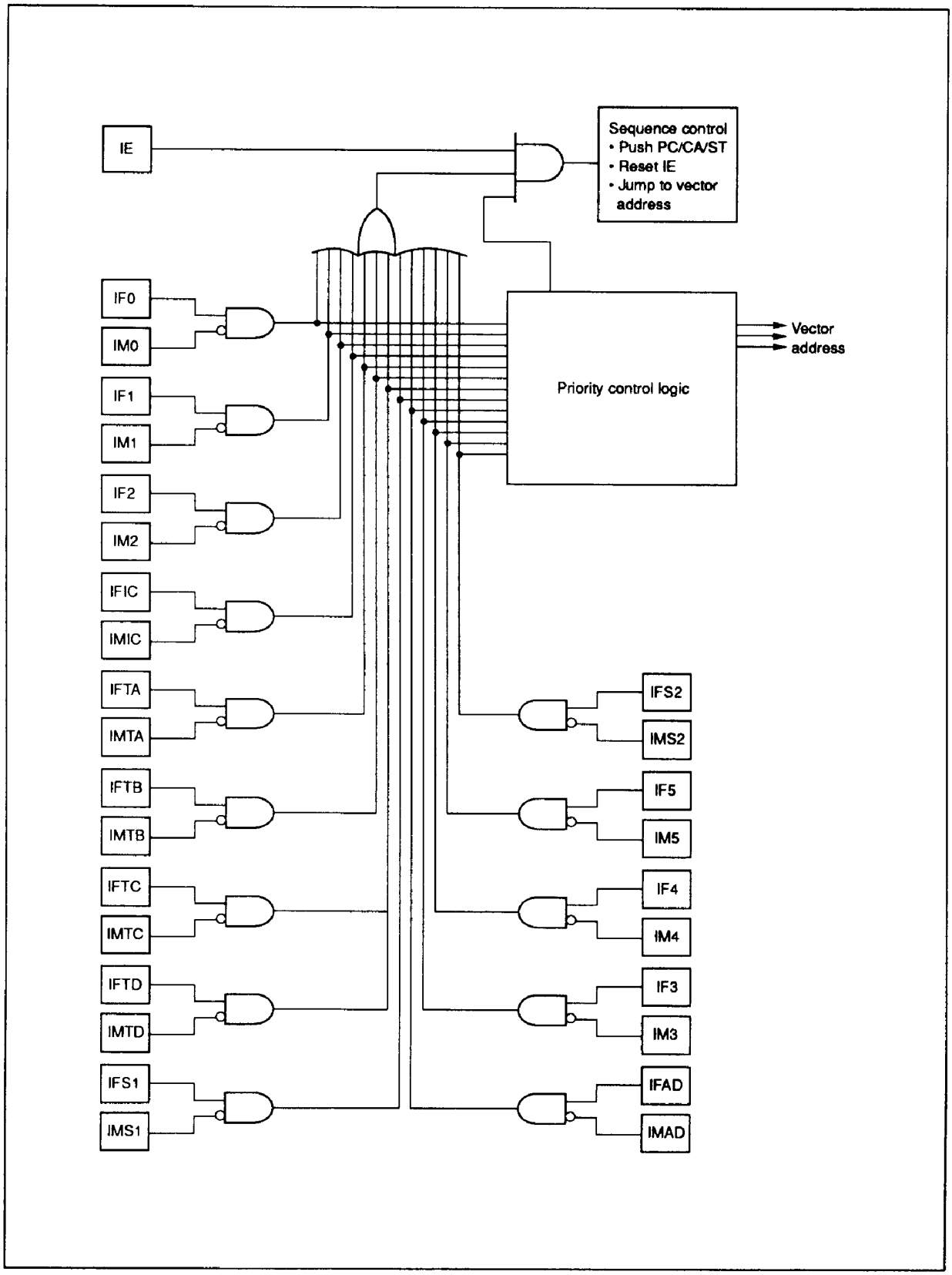


Figure 6 Block Diagram of Interrupt Control Circuit

Table 3 Interrupt Conditions

	Interrupt Source						
Interrupt Control Bit	$\overline{INT_0}$	$\overline{INT_1}$	$\overline{INT_2}$	Input Capture	Timer A	Timer B	Timer C
IE	1	1	1	1	1	1	1
IF0 • $\overline{IM0}$	1	0	0	0	0	0	0
IF1 • $\overline{IM1}$	*	1	0	0	0	0	0
IF2 • $\overline{IM2}$	*	*	1	0	0	0	0
IFIC • $\overline{IMIC}$	*	*	*	1	0	0	0
IFTA • $\overline{IMTA}$	*	*	*	*	1	0	0
IFTB • $\overline{IMTB}$	*	*	*	*	*	1	0
IFTC • $\overline{IMTC}$	*	*	*	*	*	*	1
IFTD • $\overline{IMTD}$	*	*	*	*	*	*	*
IFS1 • $\overline{IMS1}$	*	*	*	*	*	*	*
IFAD • $\overline{IMAD}$	*	*	*	*	*	*	*
IF3 • $\overline{IM3}$	*	*	*	*	*	*	*
IF4 • $\overline{IM4}$	*	*	*	*	*	*	*
IF5 • $\overline{IM5}$	*	*	*	*	*	*	*
IFS2 • $\overline{IMS2}$	*	*	*	*	*	*	*

*: Bits marked by * can be either 0 or 1. Their values have no effect on operation.

Table 3 Interrupt Conditions (cont)

	Interrupt Source						
Interrupt Control Bit	**Timer D**	**Serial 1**	**A/D**	**$\overline{INT_3}$**	**$\overline{INT_4}$**	**$\overline{INT_5}$**	**Serial 2**
IE	1	1	1	1	1	1	1
IF0 • $\overline{IM0}$	0	0	0	0	0	0	0
IF1 • $\overline{IM1}$	0	0	0	0	0	0	0
IF2 • $\overline{IM2}$	0	0	0	0	0	0	0
IFIC • $\overline{IMIC}$	0	0	0	0	0	0	0
IFTA • $\overline{IMTA}$	0	0	0	0	0	0	0
IFTB • $\overline{IMTB}$	0	0	0	0	0	0	0
IFTC • $\overline{IMTC}$	0	0	0	0	0	0	0
IFTD • $\overline{IMTD}$	1	0	0	0	0	0	0
IFS1 • $\overline{IMS1}$	*	1	0	0	0	0	0
IFAD • $\overline{IMAD}$	*	*	1	0	0	0	0
IF3 • $\overline{IM3}$	*	*	*	1	0	0	0
IF4 • $\overline{IM4}$	*	*	*	*	1	0	0
IF5 • $\overline{IM5}$	*	*	*	*	*	1	0
IFS2 • $\overline{IMS2}$	*	*	*	*	*	*	1

*: Bits marked by * can be either 0 or 1. Their values have no effect on operation.

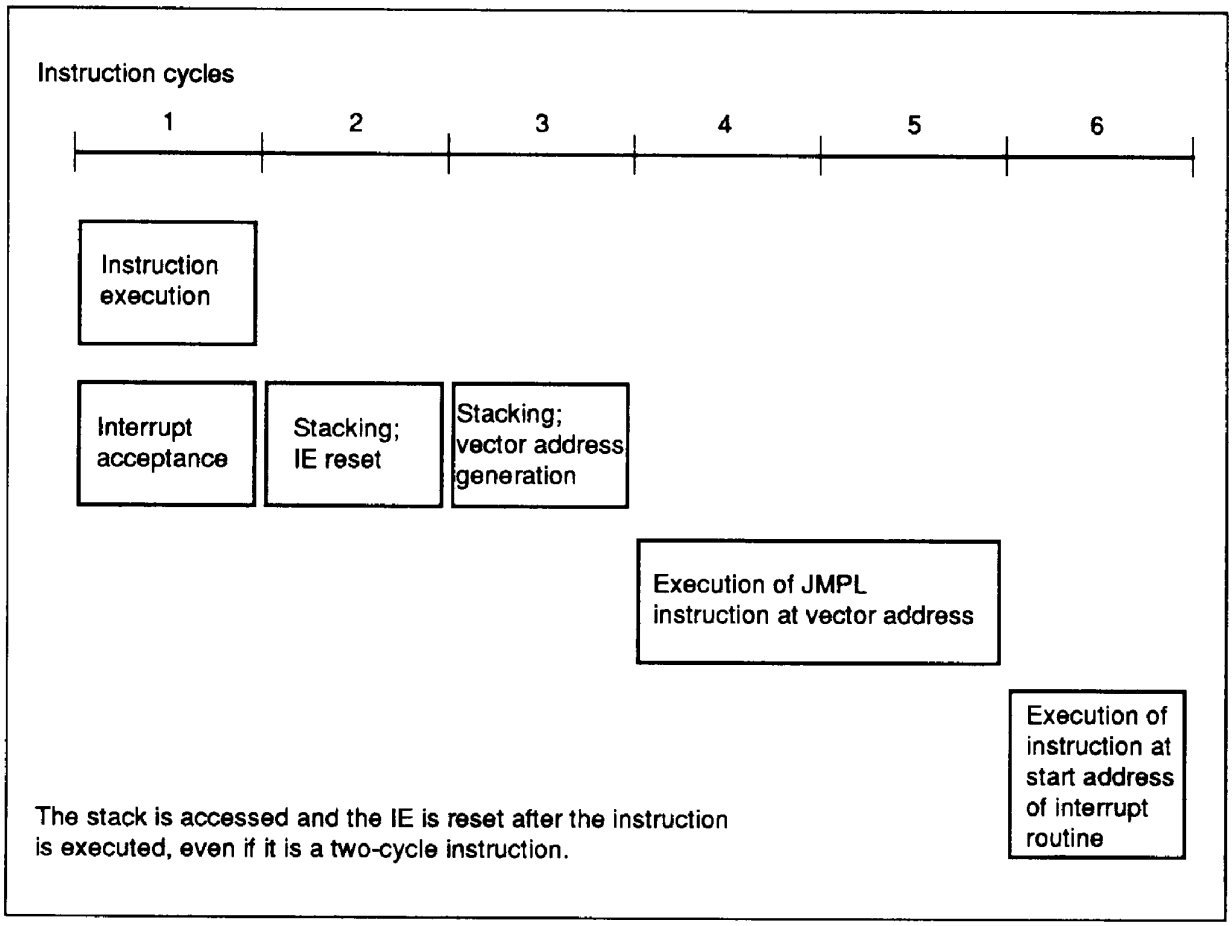


Figure 7 Interrupt Processing Sequence

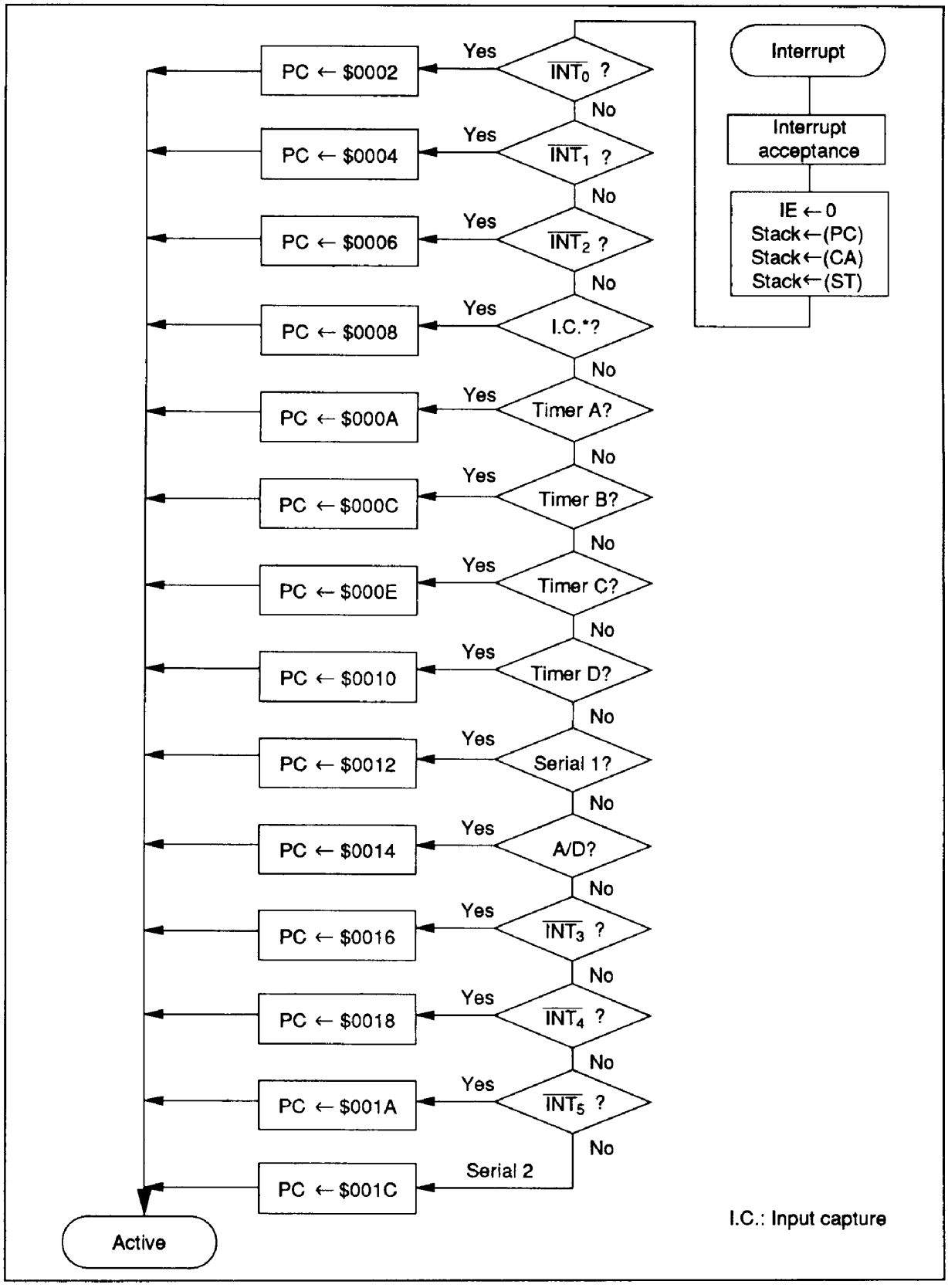


Figure 8 Interrupt Processing Flowchart

Interrupt Enable Flag (IE: $000, Bit 0): Controls all interrupts (table 4). IE is reset to 0 by the interrupt processing and set to 1 by the RTNI instruction.

External Interrupts ($\overline{INT_0}$–$\overline{INT_5}$): The MCU has six external interrupt pins.

The $\overline{INT_1}$ input can be used as a clock input for timer B in which case timer B increments at each edge selected by the interrupt mode register (IMRA). In this case, the external interrupt request flag (IM1) must be set to inhibit the $\overline{INT_1}$ interrupt request. The $\overline{INT_4}$ input can be used as an external trigger for the output compare timer.

External Interrupt Request Flags (IF0: $000, Bit 2; IF1: $001, Bit 0; IF2: $001, Bit 2; IF3: $022, Bit 2; IF4: $023, Bit 0; IF5: $023, Bit 2): Set at the rising or falling edges of the corresponding $\overline{INT_0}$ to $\overline{INT_5}$ inputs (table 5).

IF0, IF4, and IF5 are set at the falling edges of $\overline{INT_0}$, $\overline{INT_4}$, and $\overline{INT_5}$, respectively, and IF1, IF2, and IF3 are set at either the rising or falling edges of $\overline{INT_1}$, $\overline{INT_2}$, and $\overline{INT_3}$, respectively. The active edge is selected by the interrupt mode register (IMRA, IMRB).

External Interrupt Masks (IM0: $000, Bit 3; IM1: $001, Bit 1; IM2: $001, Bit 3; IM3: $022, Bit 3; IM4: $023, Bit 1; IM5: $023, Bit 3): Mask interrupt requests caused by the corresponding external interrupt request flags (table 6).

Input Capture Interrupt Request Flag (IFIC: $002, Bit 0): Set by an overflow from the input capture timer and an input capture input (table 7).

Input Capture Interrupt Mask (IMIC: $002, Bit 1): Masks an interrupt request caused by the input capture interrupt request flag (table 8).

Table 4 Interrupt Enable Flag

IE	Interrupt Enabled/Disabled
0	Disabled
1	Enabled

Table 5 External Interrupt Request Flags

IF0–IF5	Interrupt Request
0	Disabled
1	Enabled

Table 6 External Interrupt Masks

IM0–IM5	Interrupt Request
0	Enabled
1	Disabled (Masked)

Table 7 Input Capture Interrupt Request Flag

IFIC	Interrupt Request
0	Disabled
1	Enabled

Table 8 Input Capture Interrupt Mask

IMIC	Interrupt Request
0	Enabled
1	Disabled (Masked)

Timer A Interrupt Request Flag (IFTA: $002, Bit 2): Set by an overflow from timer A (table 9).

Timer A Interrupt Mask (IMTA: $002, Bit 3): Masks an interrupt request caused by the timer A interrupt request flag (table 10).

Timer B Interrupt Request Flag (IFTB: $003, Bit 0): Set by an overflow from timer B (table 11).

Timer B Interrupt Mask (IMTB: $003, Bit 1): Masks an interrupt request caused by the timer B interrupt request flag (table 12).

Timer C Interrupt Request Flag (IFTC: $003, Bit 2): Set by an overflow from timer C (table 13).

Timer C Interrupt Mask (IMTC: $003, Bit 3): Masks an interrupt request caused by the timer C interrupt request flag (table 14).

Timer D Interrupt Request Flag (IFTD: $021, Bit 0): Set by an overflow from timer D (table 15).

Timer D Interrupt Mask (IMTD: $021, Bit 1): Masks an interrupt request caused by the timer D interrupt request flag (table 16).

Table 9 Timer A Interrupt Request Flag

IFTA	Interrupt Request
0	Disabled
1	Enabled

Table 10 Timer A Interrupt Mask

IMTA	Interrupt Request
0	Enabled
1	Disabled (Masked)

Table 11 Timer B Interrupt Request Flag

IFTB	Interrupt Request
0	Disabled
1	Enabled

Table 12 Timer B Interrupt Mask

IMTB	Interrupt Request
0	Enabled
1	Disabled (Masked)

Table 13 Timer C Interrupt Request Flag

IFTC	Interrupt Request
0	Disabled
1	Enabled

Table 14 Timer C Interrupt Mask

IMTC	Interrupt Request
0	Enabled
1	Disabled (Masked)

Table 15 Timer D Interrupt Request Flag

IFTD	Interrupt Request
0	Disabled
1	Enabled

Table 16 Timer D Interrupt Mask

IMTD	Interrupt Request
0	Enabled
1	Disabled (Masked)

Serial Interrupt Request Flags (IFS1: $021, Bit 2; IFS2: $024, Bit 0): Set when the octal counter counts the eighth clock signal or when data transmission stops, resetting the octal counter (table 17).

Serial Interrupt Masks (IMS1: $021, Bit 3; IMS2: $024, Bit 1): Mask an interrupt request caused by the serial 1 and serial 2 interrupt request flags (table 18).

A/D Interrupt Request Flag (IFAD: $022, Bit 0): Set by the completion of an A/D conversion (table 19).

A/D Interrupt Mask (IMAD: $022, Bit 1): Masks an interrupt request caused by the A/D interrupt request flag (table 20).

Table 17 Serial Interrupt Request Flags

IFS1, IFS2	Interrupt Request
0	Disabled
1	Enabled

Table 18 Serial Interrupt Masks

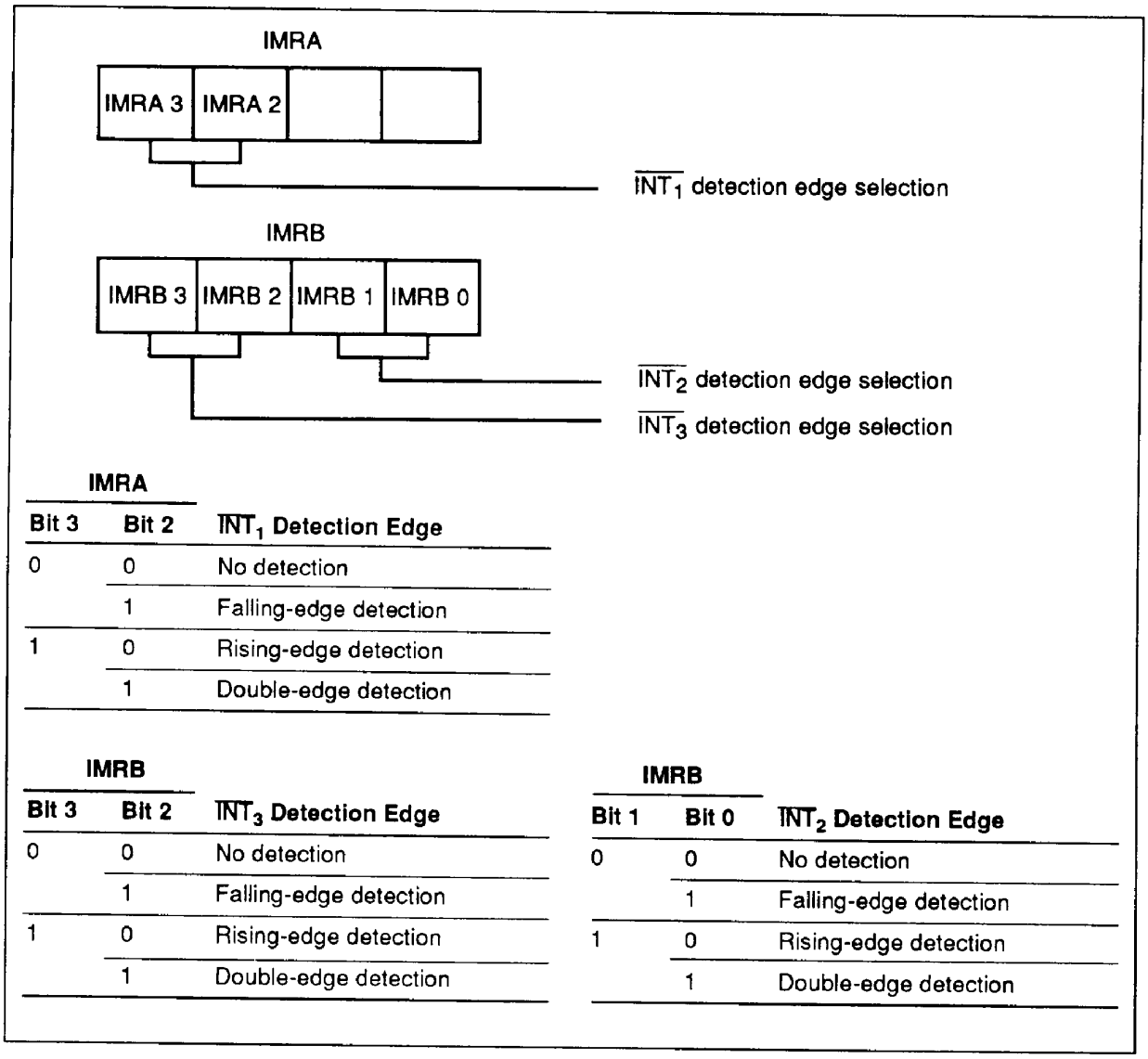
IMS1, IMS2	Interrupt Request
0	Enabled
1	Disabled (Masked)

Table 19 A/D Interrupt Request Flag

IFAD	Interrupt Request
0	Disabled
1	Enabled

Table 20 A/D Interrupt Mask

IMAD	Interrupt Request
0	Enabled
1	Disabled (Masked)



IMRA

Bit 3	Bit 2	$\overline{INT_1}$ Detection Edge
0	0	No detection
	1	Falling-edge detection
1	0	Rising-edge detection
	1	Double-edge detection

IMRB

Bit 3	Bit 2	$\overline{INT_3}$ Detection Edge
0	0	No detection
	1	Falling-edge detection
1	0	Rising-edge detection
	1	Double-edge detection

IMRB

Bit 1	Bit 0	$\overline{INT_2}$ Detection Edge
0	0	No detection
	1	Falling-edge detection
1	0	Rising-edge detection
	1	Double-edge detection

Figure 9 Interrupt Mode Register

Operating Modes

Five operating modes are available, specified by how the clock is used, as shown in table 21. The functions available in each mode are listed in table 22, operations are listed in table 23, and transitions between operating modes are listed in figure 10.

Active Mode: The MCU operates according to the clock generated by the system oscillator.

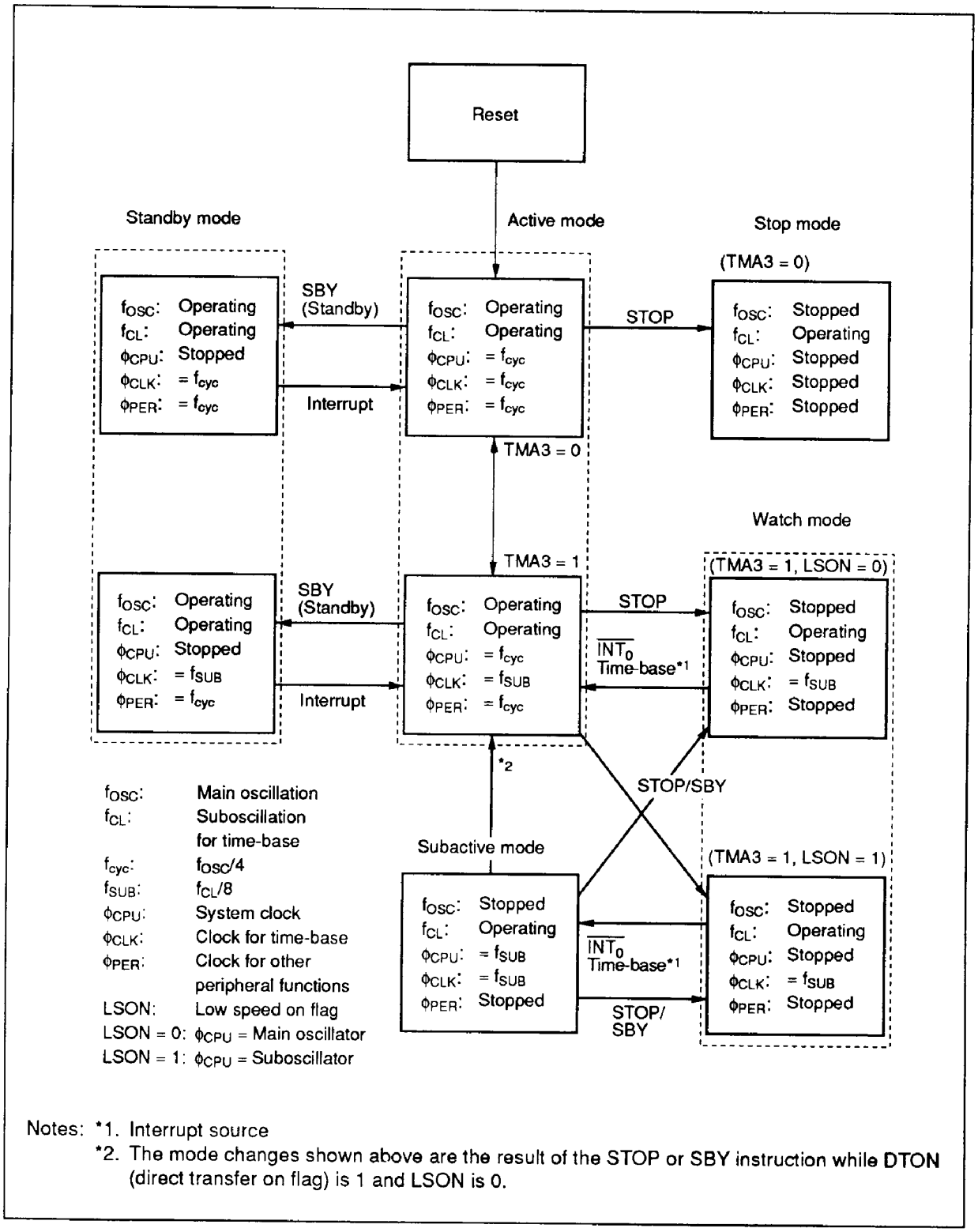
Standby Mode: The MCU enters standby mode if the SBY instruction is executed in active mode.

In this mode, the oscillator remains active and peripheral functions such as interrupts, timer/counters, and the serial interface are enabled, although all instruction-control clocks stop. The stopping of these clocks stops the CPU, retaining all RAM and register contents and maintaining the current I/O pin status.

Standby mode is terminated by a RESET input or an interrupt request. If it is terminated by a RESET input, the MCU is reset as well. After an interrupt request, the MCU enters active mode and executes the instruction following the SBY instruction. If the interrupt enable flag is 1, the interrupt is then processed; if it is 0, the interrupt request is left pending and the program is resumed. A flowchart of operation in standby mode is shown in figure 11.

Table 21 Low-Power Dissipation Modes

		System Clock (ϕ_{CPU})	
		Operating	**Stopped**
Non-time-base peripheral function clock (ϕ_{PER})	Operating	Active mode (LSON = 0)	Standby mode
	Stopped	Subactive mode (optional) (LSON = 1)	Watch mode (TMA3 = 1)
			Stop mode (TMA3 = 0)



Notes: *1. Interrupt source
*2. The mode changes shown above are the result of the STOP or SBY instruction while DTON (direct transfer on flag) is 1 and LSON is 0.

Figure 10 MCU Status Transitions

Table 22 Operations in Low-Power Dissipation Modes

Function		Stop Mode	Watch Mode	Standby Mode	Active Mode	Subactive Mode Note 4
System oscillator		Stopped	Stopped			Stopped
Subsystem oscillator		Note 2				
CPU operation (ϕ_{CPU})	Instruction execution	Stopped	Stopped	Stopped		
	RAM	Retained	Retained	Retained		
	Registers, flags	Reset	Retained	Retained		
	I/O Note 3	Reset	Retained	Retained		
Peripheral functions, interrupts (ϕ_{PER})	$\overline{INT_0}$–$\overline{INT_5}$	Reset	Retained			Retained
	Timer A	Reset	Retained			Retained
	Timer B	Reset	Retained			Retained
	Timer C	Reset	Retained			Retained
	Timer D	Reset	Retained			Retained
	Timer E (PWM)	Reset	Retained			Retained
	Input capture	Reset	Retained			Retained
	Output compare	Reset	Retained			Retained
	Serial 1, Serial 2	Reset	Retained			Retained
	A/D	Reset	Retained			Retained
Time-base functions, interrupts (ϕ_{CLK})	$\overline{INT_0}$	Reset	Note 5	Note 6	Note 6	Note 5
	Time-base	Reset	Note 5	Note 6	Note 6	Note 5

Notes: 1. ▒▒ indicates operating.
2. To reduce I_{CC}, stop oscillation in external circuits.
3. Refer to table 23.
4. Subactive mode is an optional function.
5. Refer to the Interrupt Frame section.
6. If TMA3 is set to 1, timer A and $\overline{INT_0}$ are switched to time-base function and interrupt, respectively.

Table 23 Input/Output in Low-Power Dissipation Modes

	Output		Input
	Standby Mode	Stop/Watch/ Subactive Mode	All Modes (Input state)
D_0–D_{15}	Retained/peripheral function output	High impedance	Input enabled
R0–RA	Retained/peripheral function output	High impedance	Input enabled

Note: Applying a voltage between (V_{CC} – 0.3) and (GND + 0.3 V) to input-state pins increases the current between V_{CC} and GND.

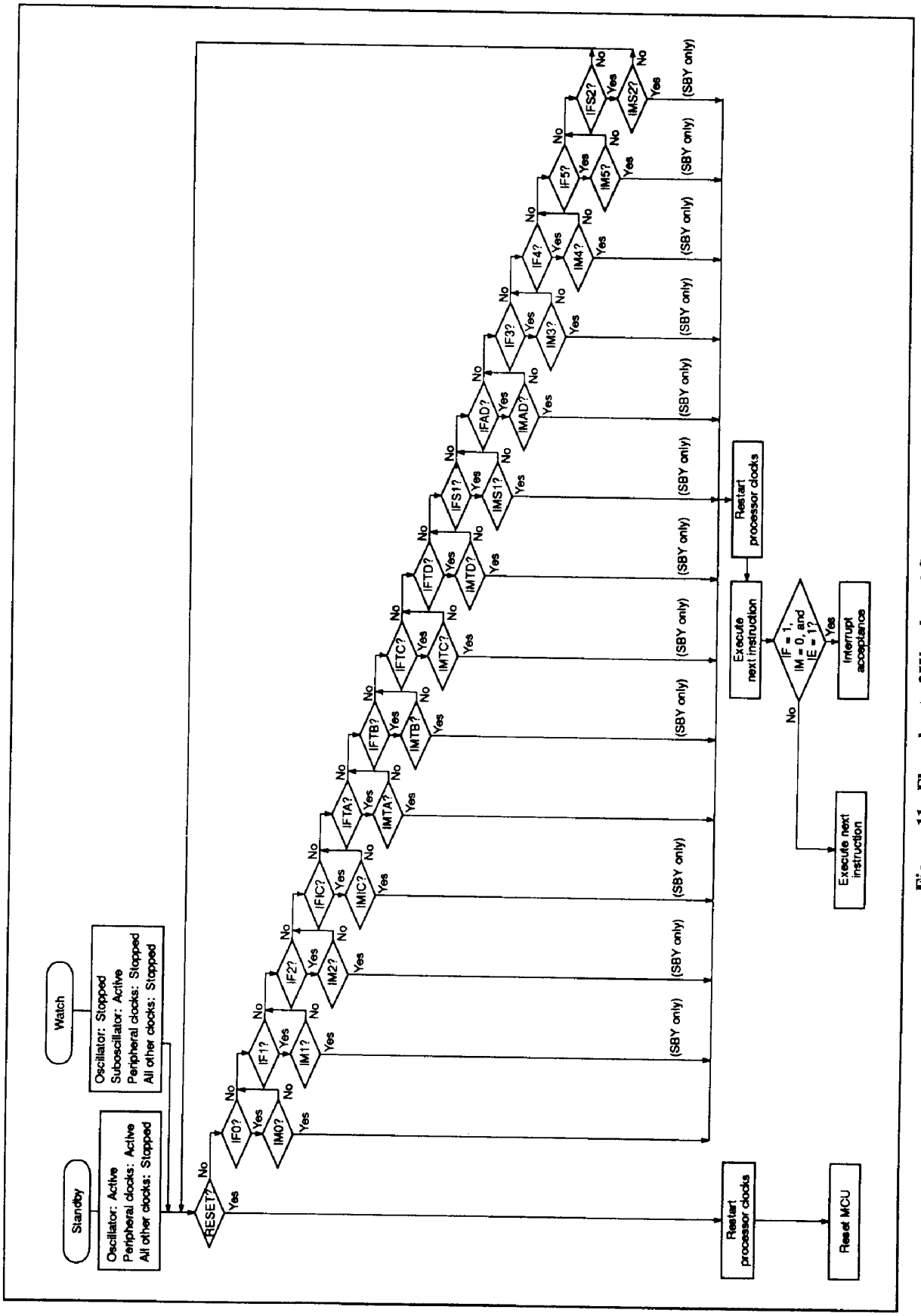


Figure 11 Flowchart of Watch and Standby Modes

Stop Mode: The MCU enters stop mode if the STOP instruction is executed in active mode while TMA3 = 0. In this mode, the system oscillator stops, causing all MCU functions to stop as well.

Stop mode is terminated by a RESET input as shown in figure 12. RESET must be high for at least one t_{RC} to stabilize oscillation (refer to the AC Characteristics section). In stop mode, all RAM contents are retained.

After stop mode is cancelled, the contents of the accumulator, B register, W register, X/SPX register, Y/SPY register, carry flag, and serial data register are not retained.

Watch Mode: The MCU enters watch mode if the STOP instruction is executed in active mode while TMA3 = 1, or if the STOP/SBY instruction is executed in subactive mode.

Watch mode is terminated by a RESET input, a timer A interrupt request, or a $\overline{INT_0}$ interrupt request. For details of RESET input, refer to the Stop Mode section. When terminated by a timer A interrupt request or a $\overline{INT_0}$ interrupt request, the MCU enters active mode if LSON is 0 or subactive mode if LSON is 1. Any interrupt request generated during the transition to active mode is delayed for half the interrupt frame period (t_{RC}) to give the oscillation time to stabilize (figure 14). Operation during mode transition is the same as that at standby mode cancellation (figure 11).

Subactive Mode: The CPU operates with a clock generated by the CL_1 and CL_2 oscillation circuits. Functions which can operate in subactive mode are listed in table 23.

The MCU enters active mode from subactive mode by the following steps. The MCU enters watch mode if the STOP or SBY instruction is executed in subactive mode while the LSON is reset and the DTON is set. At the next interrupt frame, the MCU waits for the oscillation time selected by the MIS to stabilize, and then enters active mode (figure 13). After that, the DTON is automatically reset (the DTON can be set only in subactive mode).

Subactive mode is an optional function that the user must specify on the function option list.

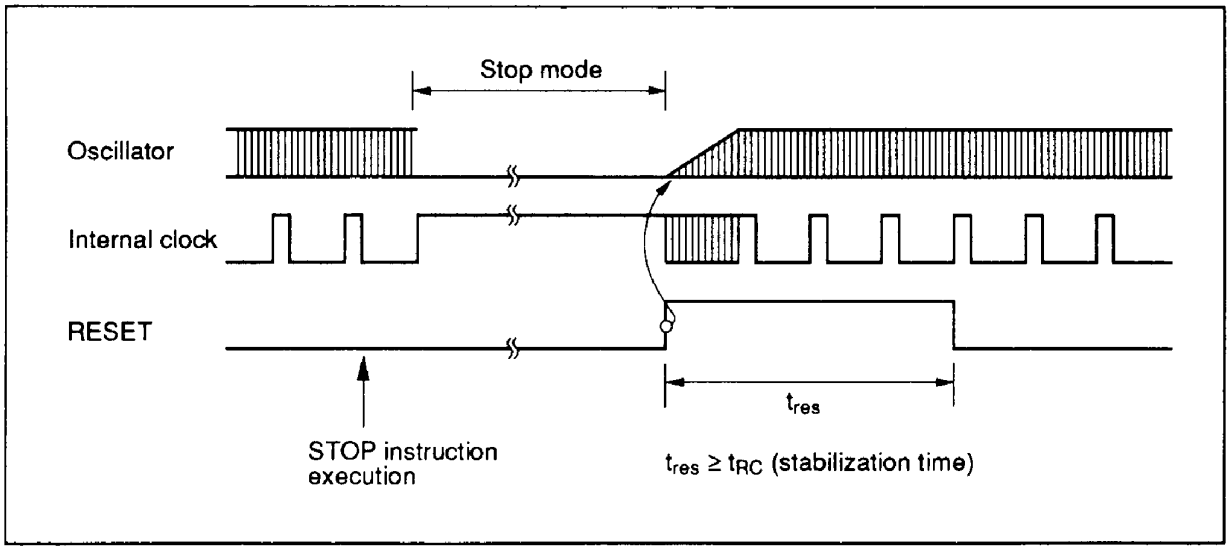


Figure 12 Timing of Stop Mode Cancellation

Interrupt Frame: In watch and subactive modes, timer A and $\overline{INT_0}$ interrupts are generated in synchronism with the interrupt frame. The interrupt frame is repeated at the timing shown in figure 14. Three interrupt frame cycles can be selected by the settings of the miscellaneous register (figure 15).

The period from the interrupt strobe to the interrupt request generation is used as the oscillation time to stabilize during the transition from watch mode to active mode. Operation during the transition from watch mode to active mode is the same as a standby mode cancellation. The overflow timing during the transition to active mode by the timer A interrupt request is the same as the interrupt strobe shown in figure 14.

MCU Operation Sequence: The MCU operates in the sequence shown in figures 16 to 18. It is reset by a RESET input, regardless of its state.

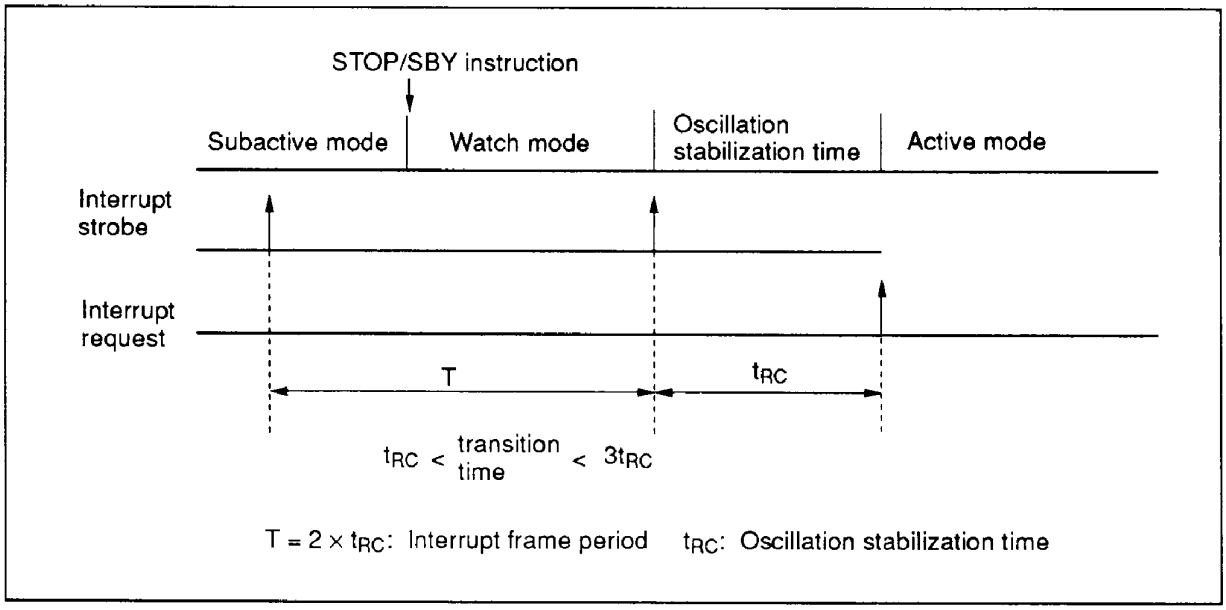


Figure 13 Timing of Subactive Mode Direct Transition

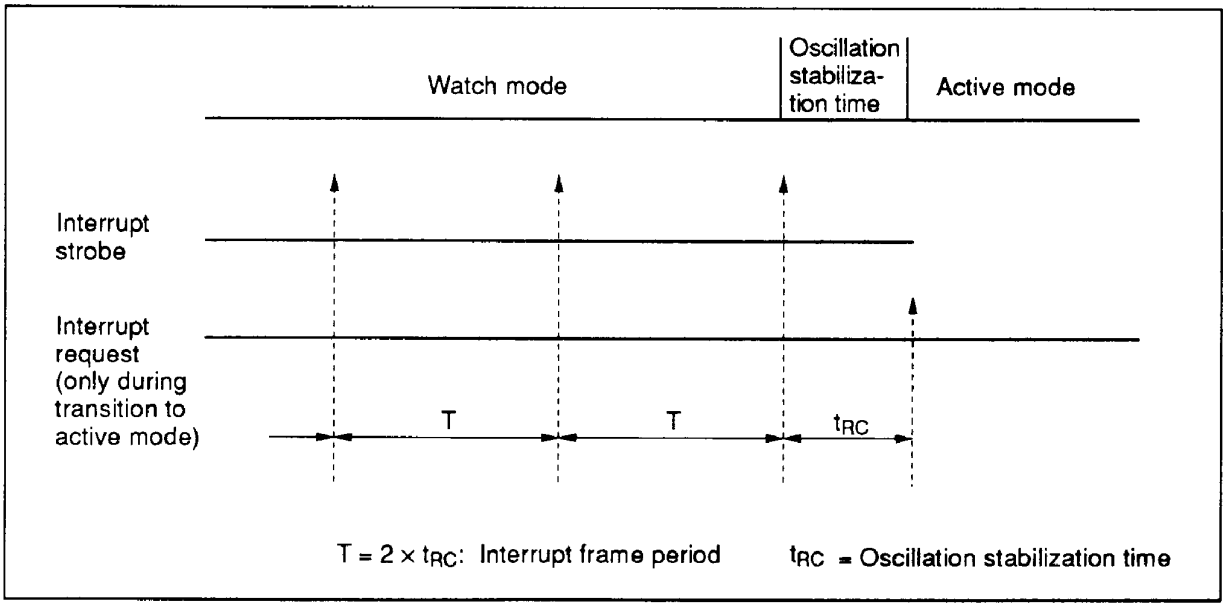
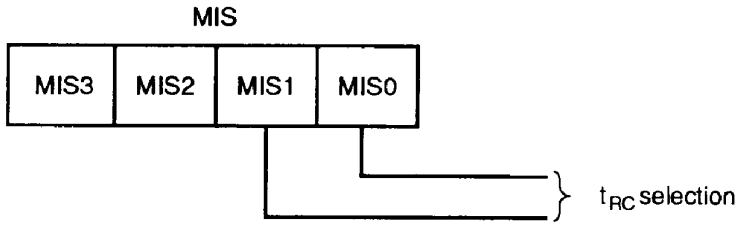


Figure 14 Interrupt Frame



MIS

Bit 1	Bit 0	T/2, t_{RC}
0	0	0.12207 ms
0	1	7.8125 ms
1	0	62.5 ms
1	1	Not used

Note: Only when a 32.768-kHz oscillation is used.
T: Interrupt frame period
t_{RC}: Oscillation stabilization time

Figure 15 Miscellaneous Register

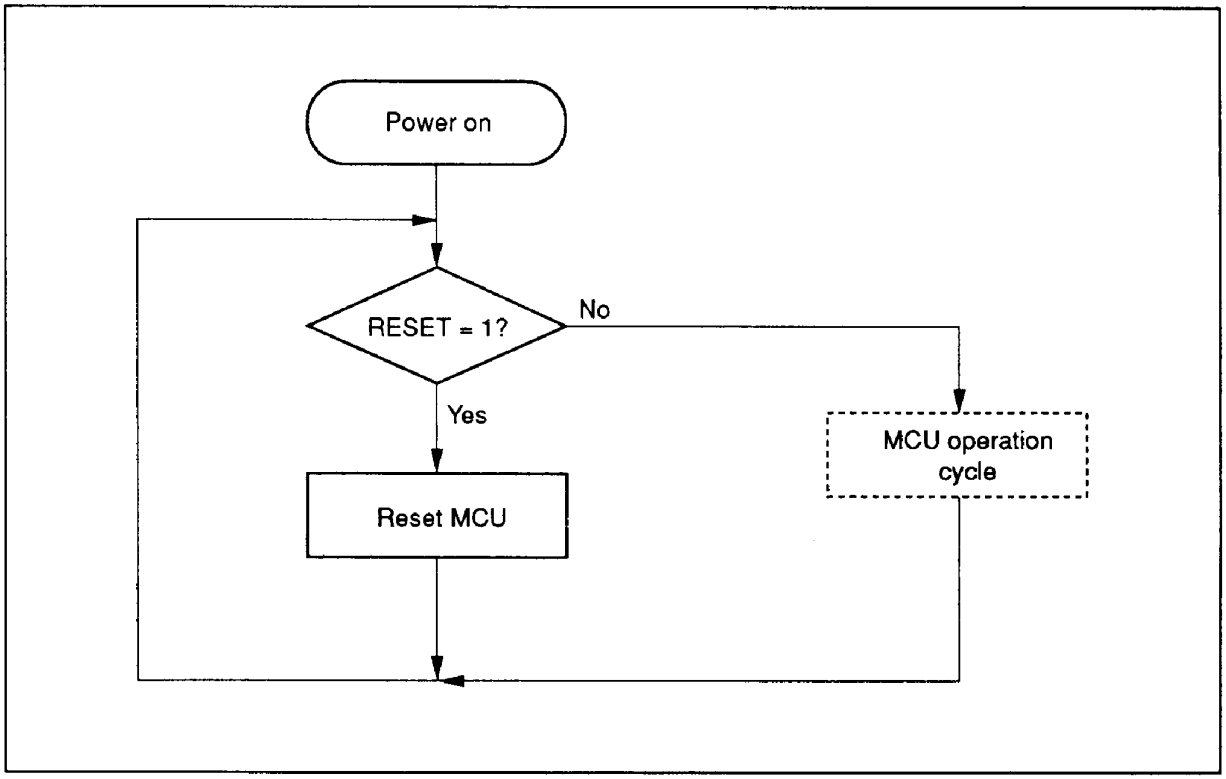


Figure 16 MCU Operation Flowchart (Power On)

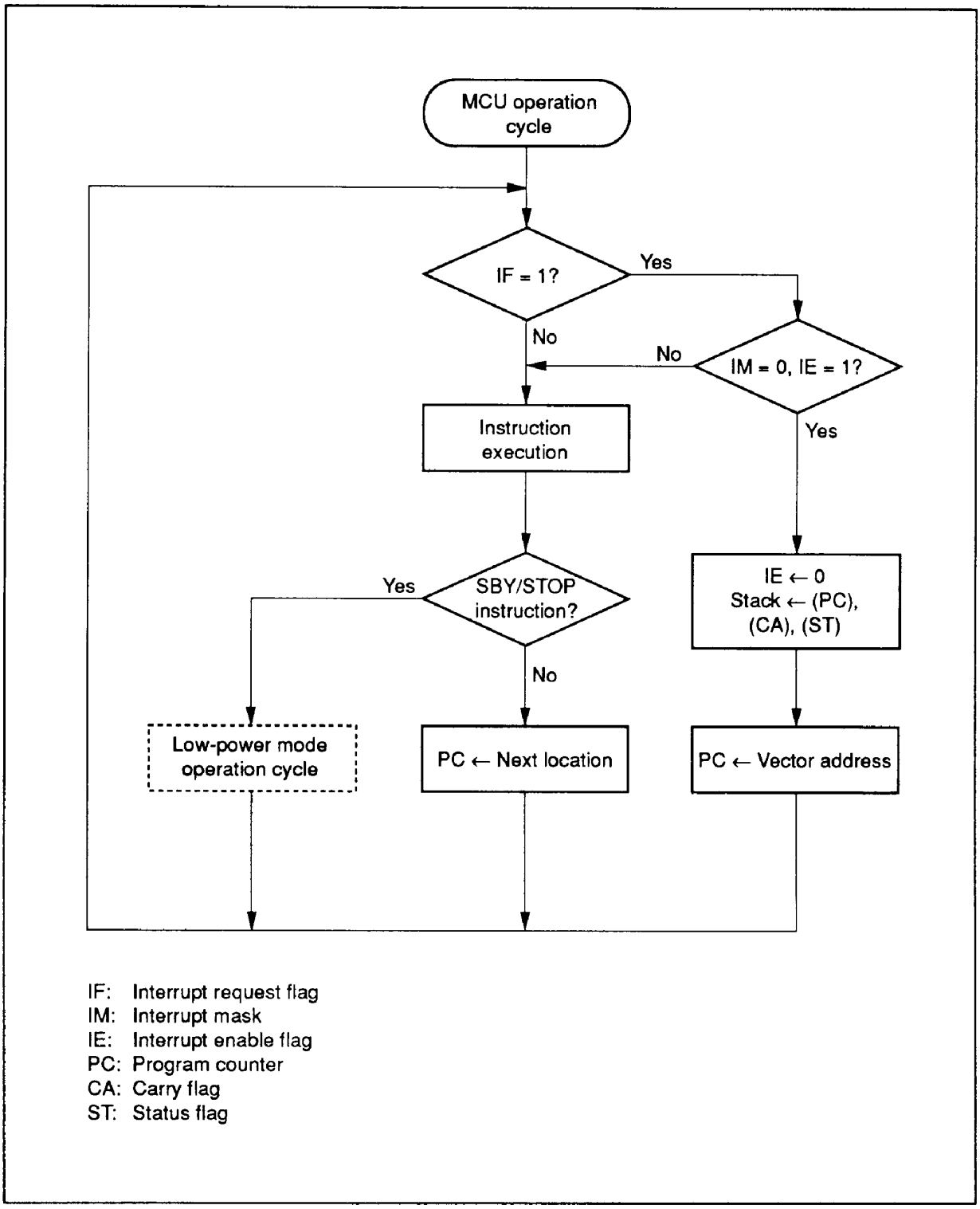


Figure 17 MCU Operation Flowchart (MCU Operation Cycle)

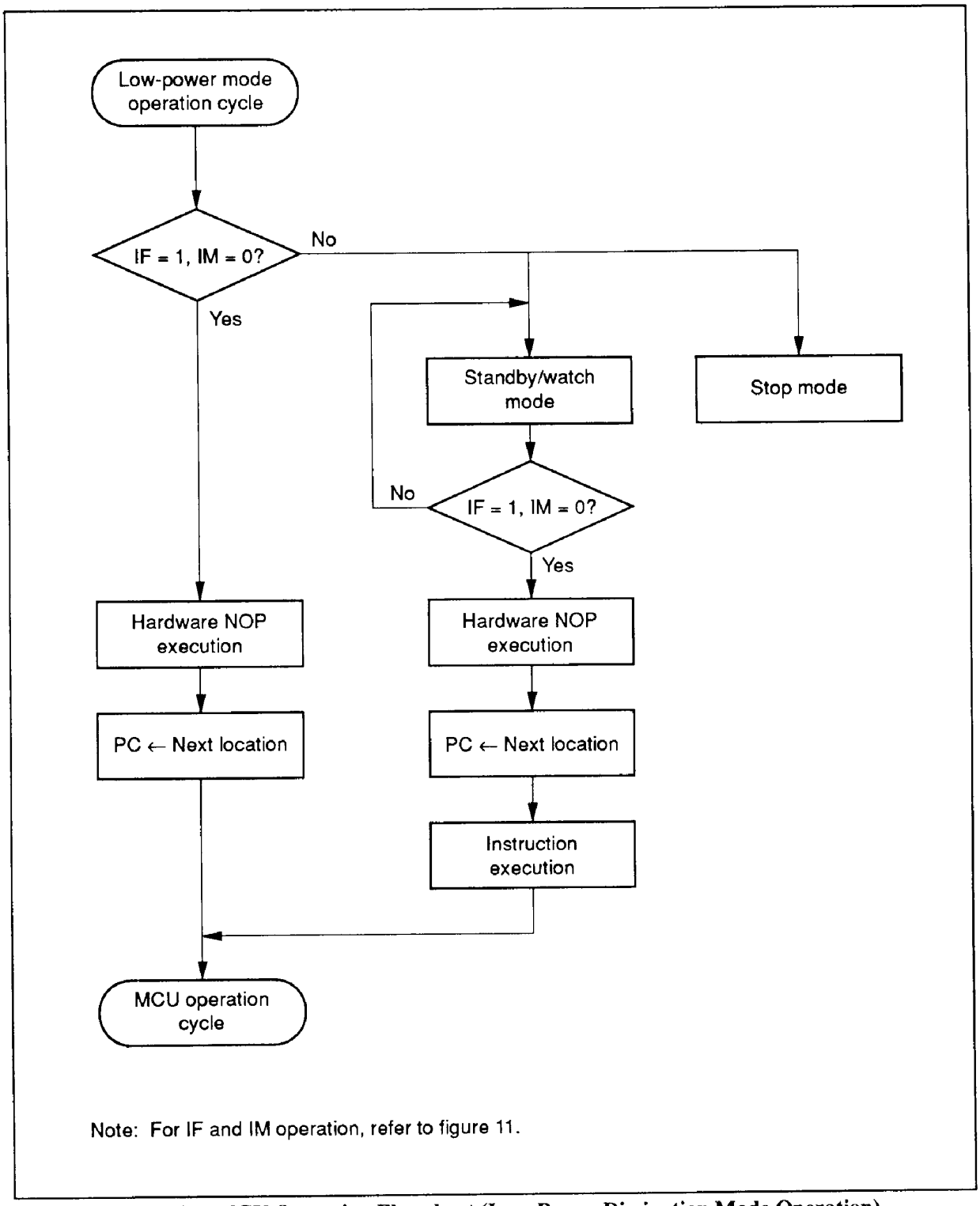


Figure 18 MCU Operation Flowchart (Low-Power Dissipation Mode Operation)

Internal Oscillation Circuit

A block diagram of the internal oscillation circuit is shown in figure 19. As shown in table 24, a crystal or a ceramic oscillator can be connected to OSC_1 and OSC_2, and a crystal oscillator of 32.768-kHz can be connected to CL_1 and CL_2. An external clock operation of the system oscillator is also available. If not using a subsystem oscillator, fix the CL_1 pin to V_{CC} or GND.

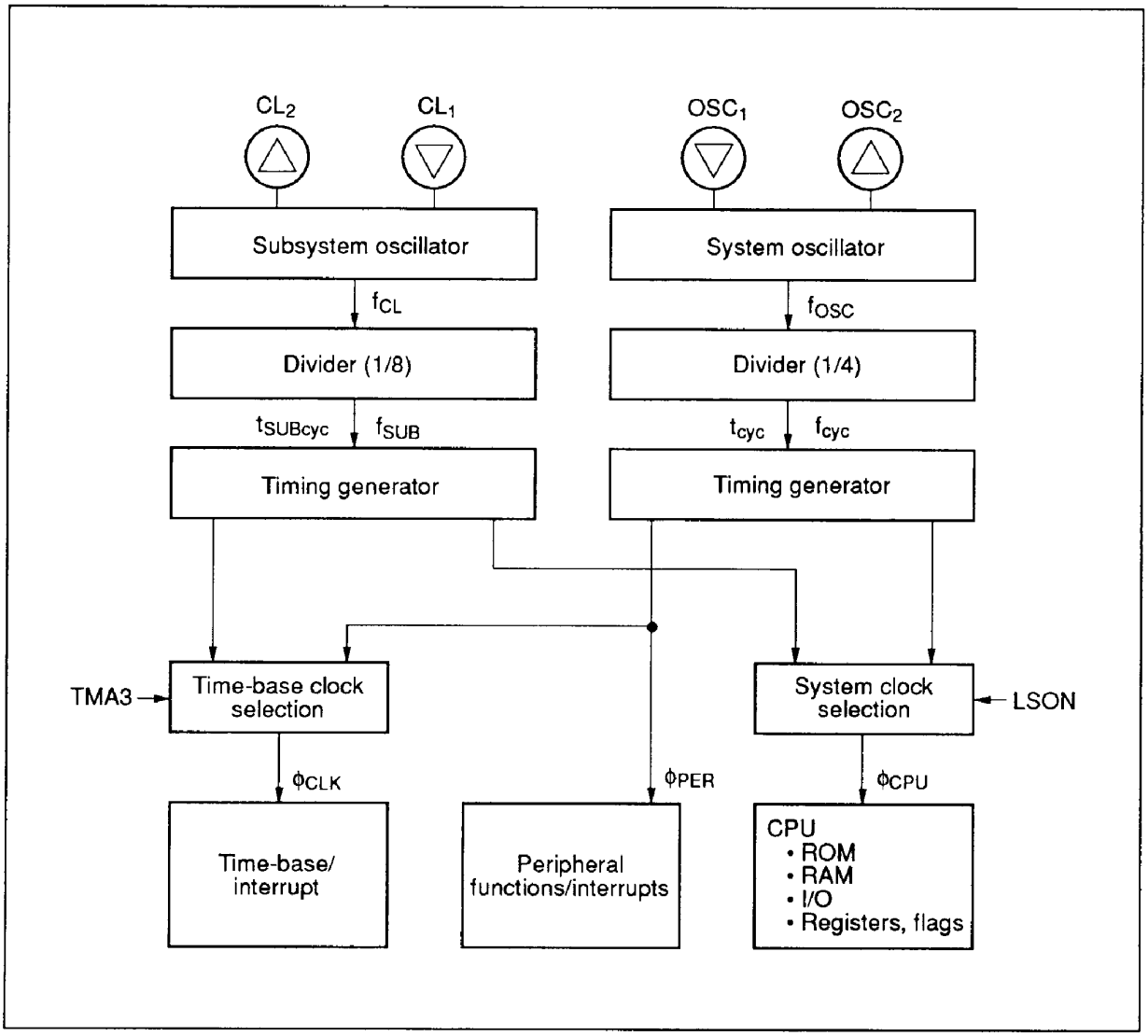


Figure 19 Internal Oscillator Circuit

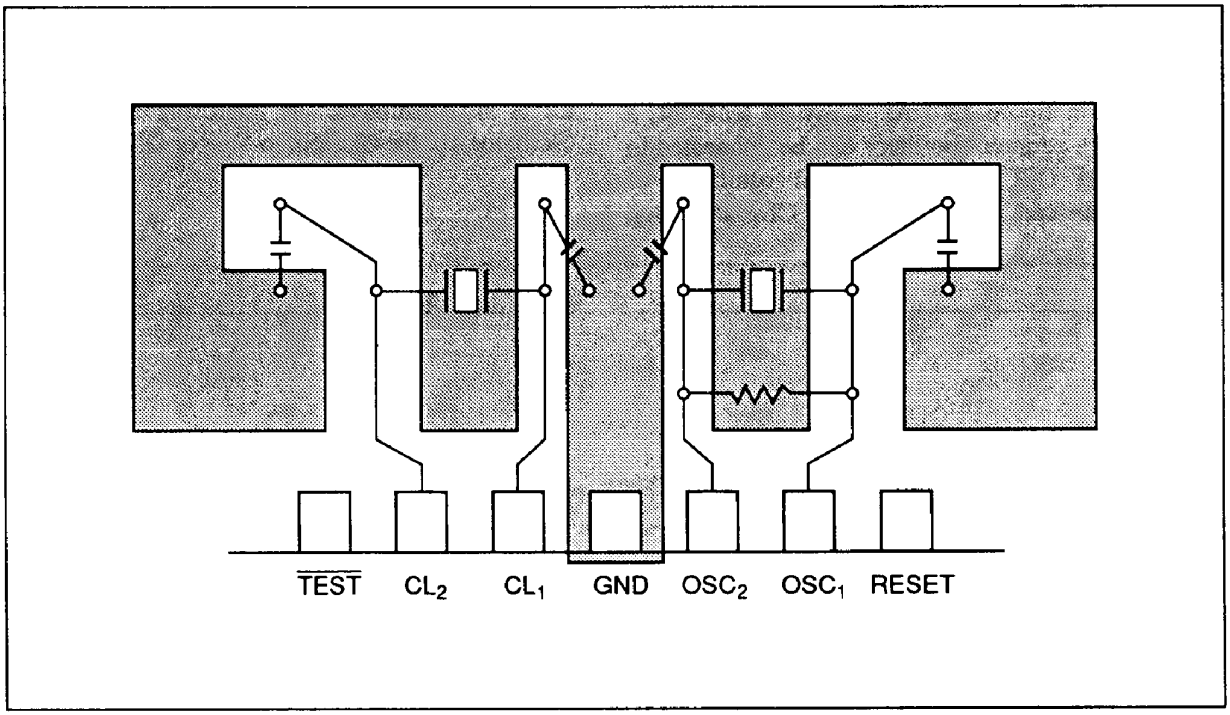
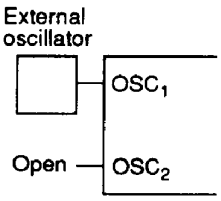
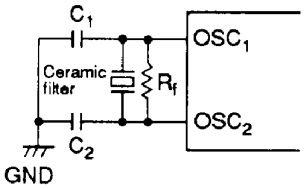
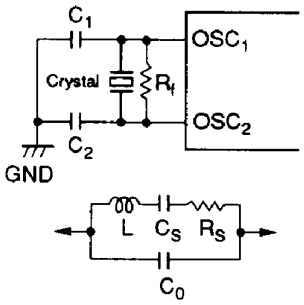
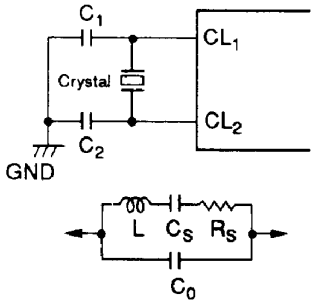


Figure 20 Pattern Layout Example of Oscillation Circuit

Table 24 Oscillator Circuit Examples

Circuit Configuration	Circuit Constants
External clock operation (OSC_1, OSC_2) 	
Ceramic filter oscillator (OSC_1, OSC_2) 	Ceramic filter: CSA4.00MG (Murata) R_f = 1 MΩ ± 20% $C_1 = C_2$ = 33 pF ± 20%
Crystal oscillator (OSC_1, OSC_2) 	R_f = 1 MΩ ± 20% $C_1 = C_2$ = 22 pF ± 20% Crystal: Equivalent to circuit shown at bottom left C_0 = 7 pF, max. R_s = 100 Ω, max. f = 1.6 to 4.5 MHz
Crystal oscillator (CL_1, CL_2) 	$C_1 = C_2$ = 15 pF ± 5% Crystal: MX38T (Nihon Dempa Kogyo) C_0 = 1.5 pF, typ. R_s = 14 kΩ, typ. f = 32.768-kHz

Notes:
1. The circuit constants given above are recommended values provided by the oscillator manufacturer. Since they may be affected by stray capacitances from the oscillator or board, consult the crystal oscillator or ceramic filter manufacturer to determine the actual circuit parameters required.
2. Wiring between the OSC_1/OSC_2 pins and other elements must be as short as possible, and must not cross other wiring. Refer to the recommended layout of the oscillation circuit in figure 20.
3. If not using a 32.768-kHz crystal oscillator, fix the CL_1 pin to GND and leave the CL_2 pin open.

Input/Output

The MCU (mask ROM version) has 70 input/output pins, 33 of the input/output pins being standard pins whose circuits can be selected as with pull-up MOS (B) or without pull-up MOS (C) option.

The HD404719 has 37 other high-voltage pins whose circuits can be selected as with pull-down MOS (E) or without pull-down MOS (D) option. If the former option is selected, the $R5_0/V_{disp}$ pin must be set as V_{disp} by the mask option because the source of the pull-down MOS is connected to V_{disp}.

The HD404439 has no high-voltage pins. The pins corresponding to the HD404719 high-voltage pins are standard open-drain PMOS pins in the HD404439. The circuits must be without pull-down MOS (D). The $R5_0$ pin is only used as an input port.

The HD4074719 has only the pins without pull-up MOS (C) and without pull-down MOS (D).

D Port: The 16 out of 70 I/O pins that are discrete pins (D port), accessed individually. These pins are set by the SED and SEDD instructions, reset by the RED and REDD instructions, and tested by the TD and TDD instructions.

R Ports: Accessed in 4-bit units. Data is input to the ports by the LAR and LBR instructions and output from them by the LRA and LRB instructions. The R6 to RB output buffers are turned on and off by R-port data control registers (DCR6–DCRB).

Mask Options: The circuits of the HD4074719 are either without pull-up MOS (C) or without pull-down MOS (D), as shown in table 25 and figure 21. Options either with pull-up MOS (B) or with pull-down MOS (E) can be selected for the HD404719, and an option with pull-up MOS (B) can be selected for the HD404439. However, note that these MCUs are not compatible with the HD4074719.

How to Deal with Unused I/O Pins: I/O pins that are not needed by the user system must be fixed as follows to prevent LSI malfunctions due to noise. Note the following precautions:

- For high-voltage pins, the without pull-down MOS option must be selected. The pins are connected to the V_{CC} voltage of the user system.
- For standard pins, the without pull-down MOS option must be selected. The pins are connected to the GND voltage of the user system.
- Open-drain PMOS pins are connected to the V_{CC} voltage of the user system.

Table 25 Input/Output Pin Types

Standard Pins

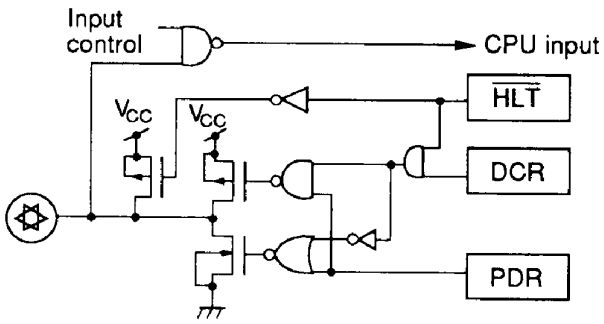
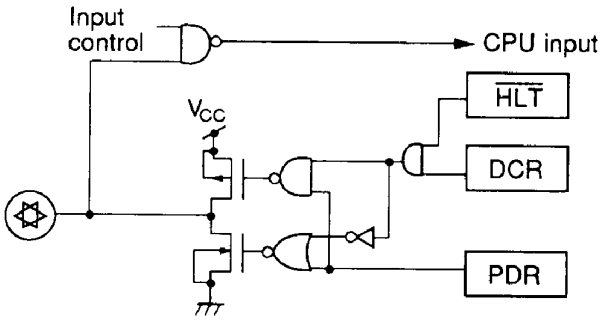
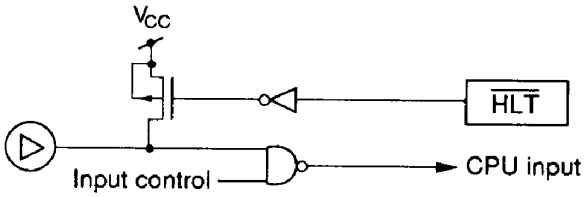
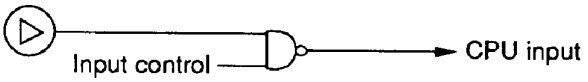
Pin Type	With Pull-Up MOS (B)/Without Pull-Up MOS (C)	Pin Name
I/O pins		$R6_0$–$R6_3$ $R7_0$–$R7_3$ $R8_0$–$R8_3$ $R9_0$–$R9_3$ RA_0–RA_3 RB_0–RB_1
		
Input pins		$R5_1$–$R5_3$ RC_0–RC_3 RD_0–RD_3
		

Table 25 Input/Output Pin Types (cont)

Standard Pins

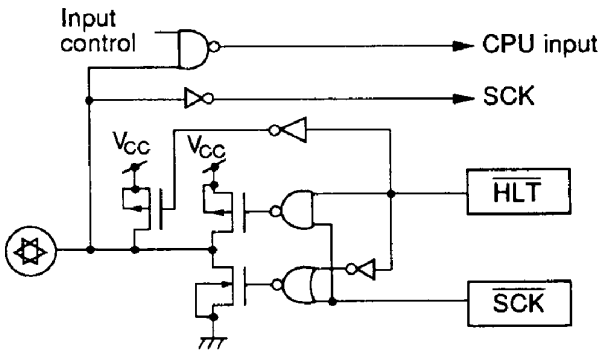
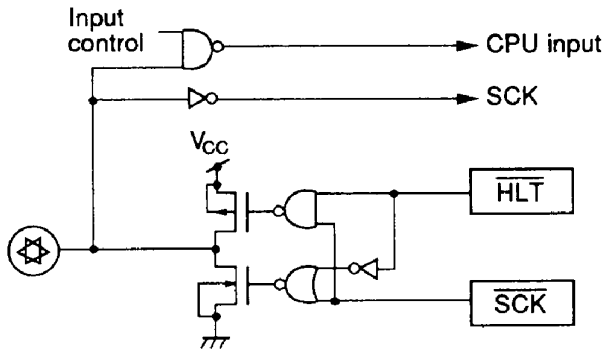
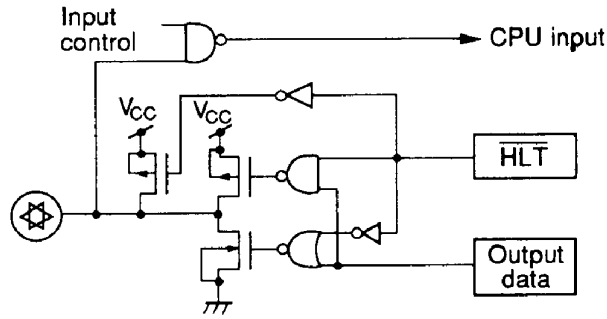
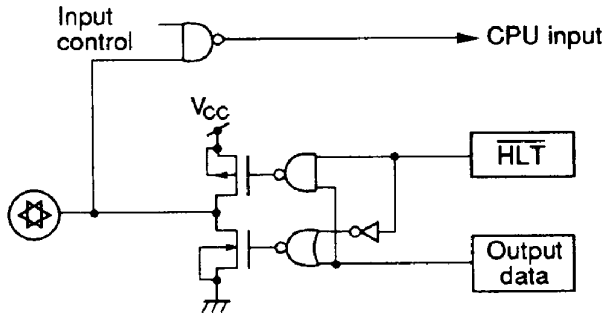
Pin Type	With Pull-Up MOS (B)/Without Pull-Up MOS (C)	Pin Name
Peripheral I/O pins		$\overline{SCK_1}$ $\overline{SCK_2}$ (output)Note 1
		
Peripheral output pins		SO_1, SO_2 TOC TOD TOE_1, TOE_2 TOG BUZZ
		

Table 25 Input/Output Pin Types (cont)

Standard Pins

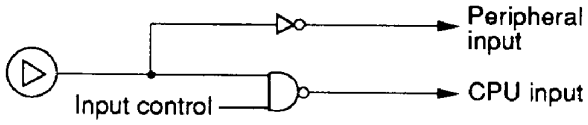
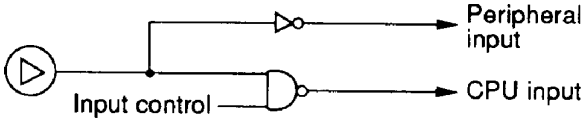
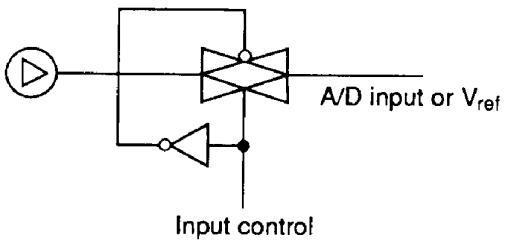
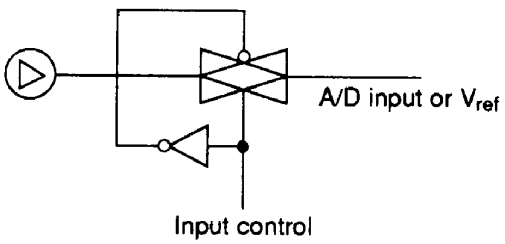
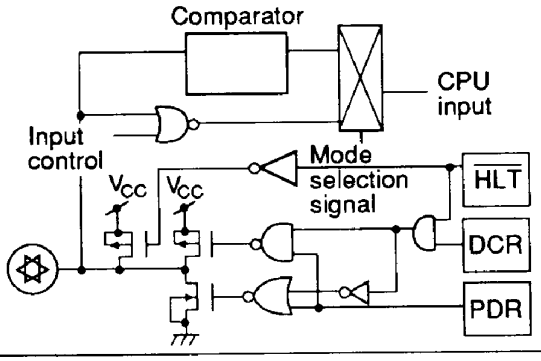
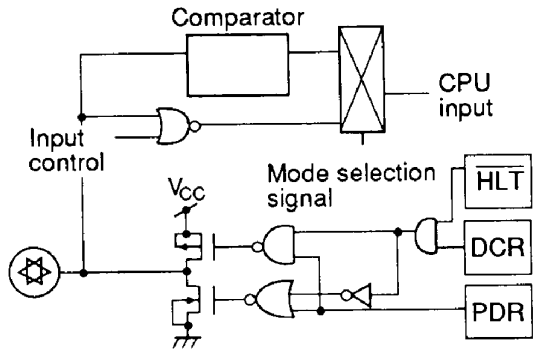
Pin Type	With Pull-Up MOS (B)/Without Pull-Up MOS (C)	Pin Name
Peripheral input pins		$\overline{SCK_1}$, $\overline{SCK_2}$ (input)Note 1 SI_1, SI_2 $\overline{INT_0}$ $\overline{INT_1}$ $\overline{INT_2}$ $\overline{INT_3}$ $\overline{INT_4}$ ICT_0, ICT_1
		
		AN_0–AN_7 V_{ref} ($R6_1$)
		

Table 25 Input/Output Pin Types (cont)

Standard Pins

Pin Type	With Pull-Up MOS (B)/Without Pull-Up MOS (C)	Pin Name
I/O pins		$R6_0$/COMP
		

High-Voltage Pins (Open-Drain PMOS Pins)

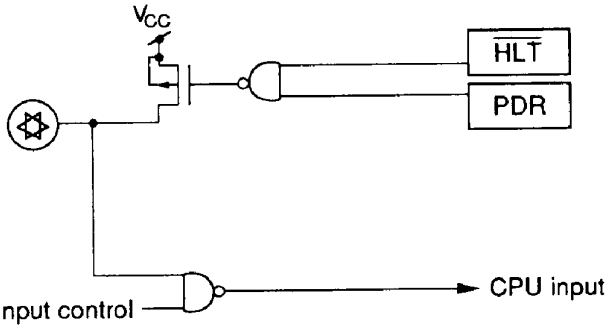
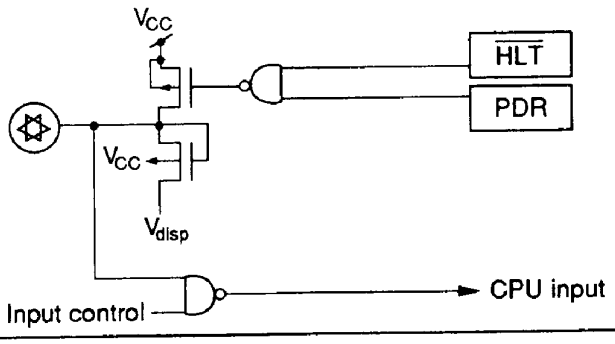
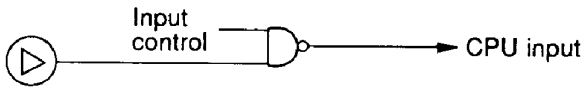
Pin Type	Without Pull-Down MOS (D)/With Pull-Down MOS (E)	Pin Name
I/O pins		D_0–D_{15} $R0_0$–$R0_3$ $R1_0$–$R1_3$ $R2_0$–$R2_3$ $R3_0$–$R3_3$ $R4_0$–$R4_3$
		

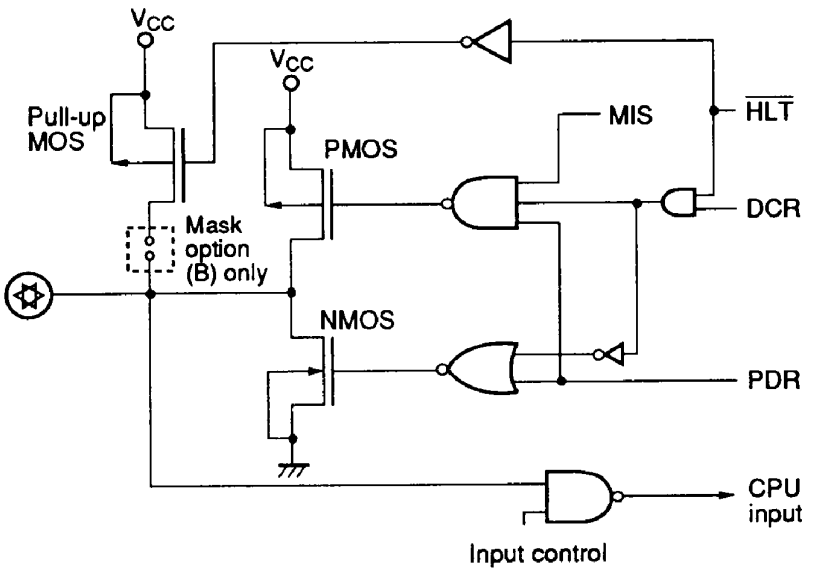
Table 25 Input/Output Pin Types (cont)

High-Voltage Pins

Pin Type	Without Pull-Down MOS (D)	Pin Name
Input pins		$R5_0$

Notes:
1. If external clock mode is selected when the serial interface is used, $\overline{SCK_1}$ and $\overline{SCK_2}$ are used as input pins.
2. In stop mode, the MCU is internally reset and peripheral functions are cancelled. The HLT signal goes high and the output pins are at high impedance.
3. In watch/subactive mode, the HLT signal goes high and the output pins are at high impedance. The input level of I/O pins selected for peripheral functions must be fixed since these pins are in input state.
4. Select the circuit type for a mask ROM MCU as shown below. A mask ROM MCU is compatible with a ZTAT™ MCU only when C- and D-type circuits are selected for the mask ROM MCU.
5. The HD404439 has no high-voltage pins. The pins corresponding to the high-voltage pins are standard open-drain PMOS pins, therefore, the circuits must be used as with pull-down MOS (D). Option E cannot be selected.

	Circuit Type			
Product Type	**B**	**C**	**D**	**E**
Mask ROM (HD404719)	Optional			
Mask ROM (HD404439)	Optional		Fixed	
ZTAT™ (HD4074719)		Fixed		



Mask Option		With Pull-Up MOS (B)				Without Pull-Up MOS (C)			
DCR		0		1		0		1	
PDR		0	1	0	1	0	1	0	1
CMOS buffer	PMOS	—	—	—	On	—	—	—	On
	NMOS	—	—	On	—	—	—	On	—
Pull-up MOS (C)		On	On	On	On	—	—	—	—

Notes: 1. —: Off
2. For the $R8_2/SO_1$ and $R9_3/SO_2$ pins, the PMOSs are off when bits 2 and 3 of the miscellaneous register are set to 1.

MIS Bit 2	$R8_2/SO_1$ PMOS Mode
0	On
1	Off

MIS Bit 3	$R9_3/SO_2$ PMOS Mode
0	On
1	Off

Figure 21 Input/Output Buffer

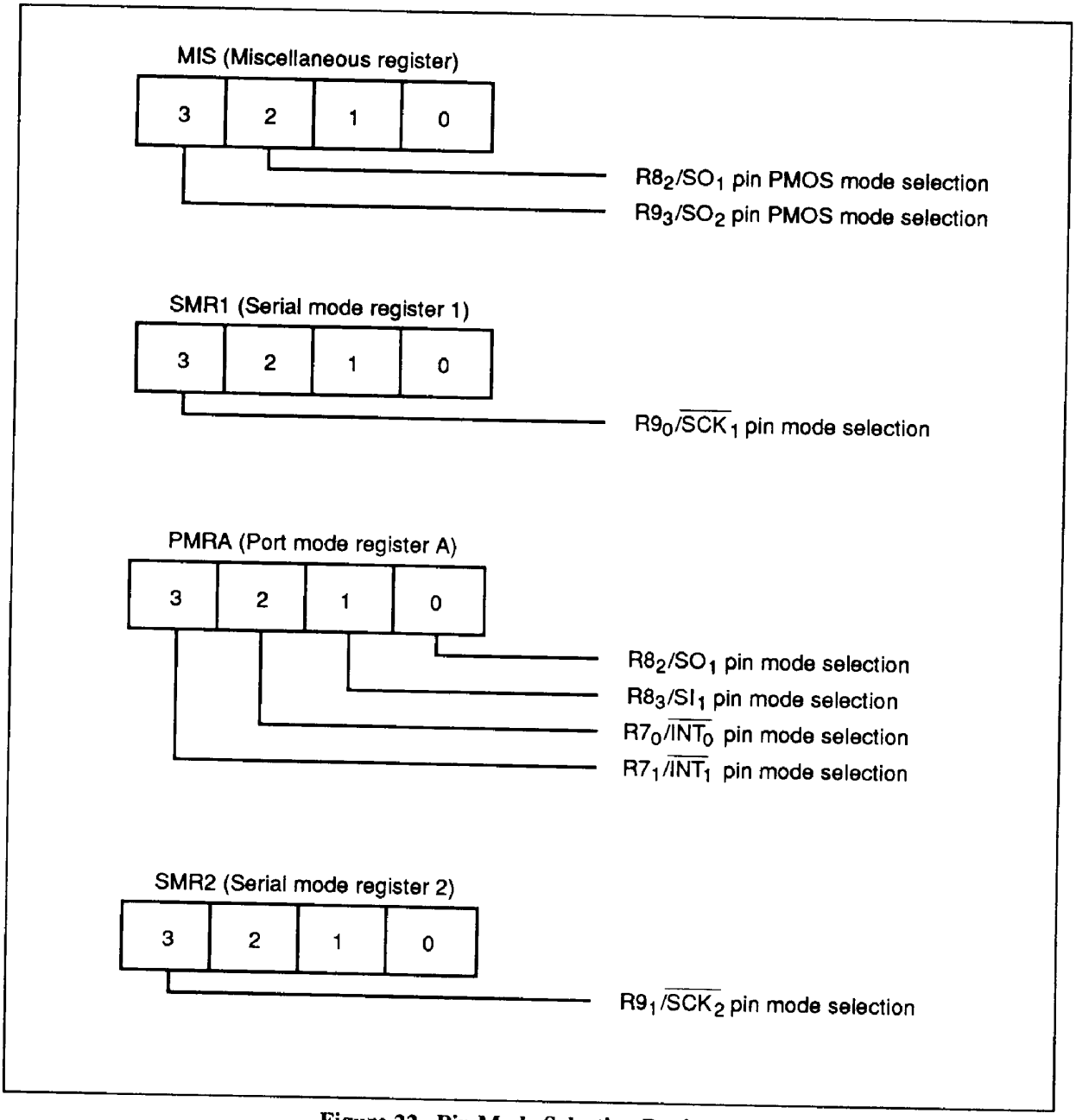


Figure 22 Pin Mode Selection Registers

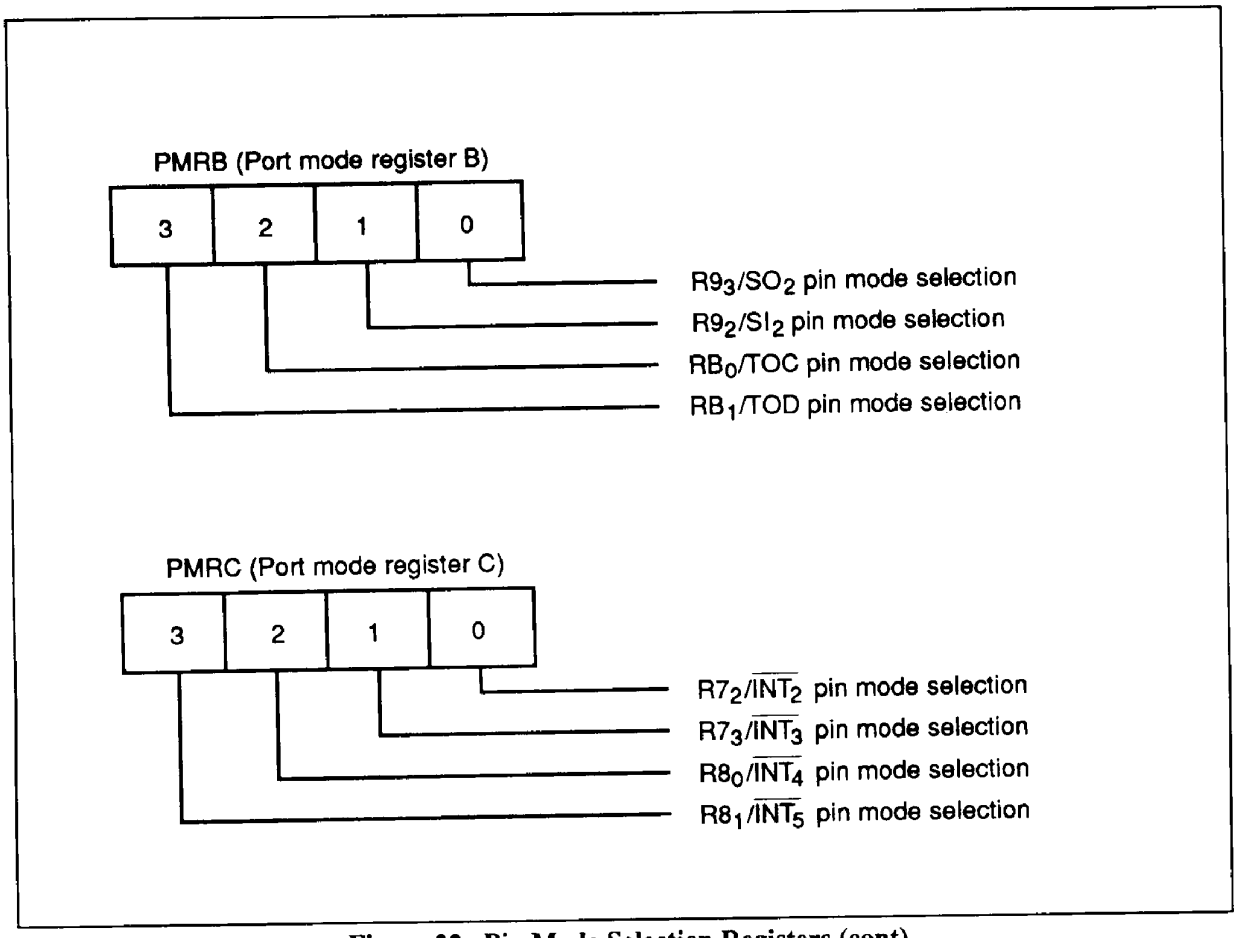


Figure 22 Pin Mode Selection Registers (cont)

Timers

The MCU has two prescalers (S and W) and five timer/counters (A, B, C, D, and E). Block diagrams of the timers are shown in figures 23, 24, 26, and 29.

Prescaler S: Eleven-bit counter that inputs the system clock signal. After being initialized to $000 by MCU reset, prescaler S divides the system clock frequency. Only at MCU reset or during watch and stop modes does prescaler S stop counting.

Prescaler W: Five-bit counter that inputs the CL_1 input clock signal divided by 8. Prescaler W output can be selected as a timer A input clock by timer mode register A.

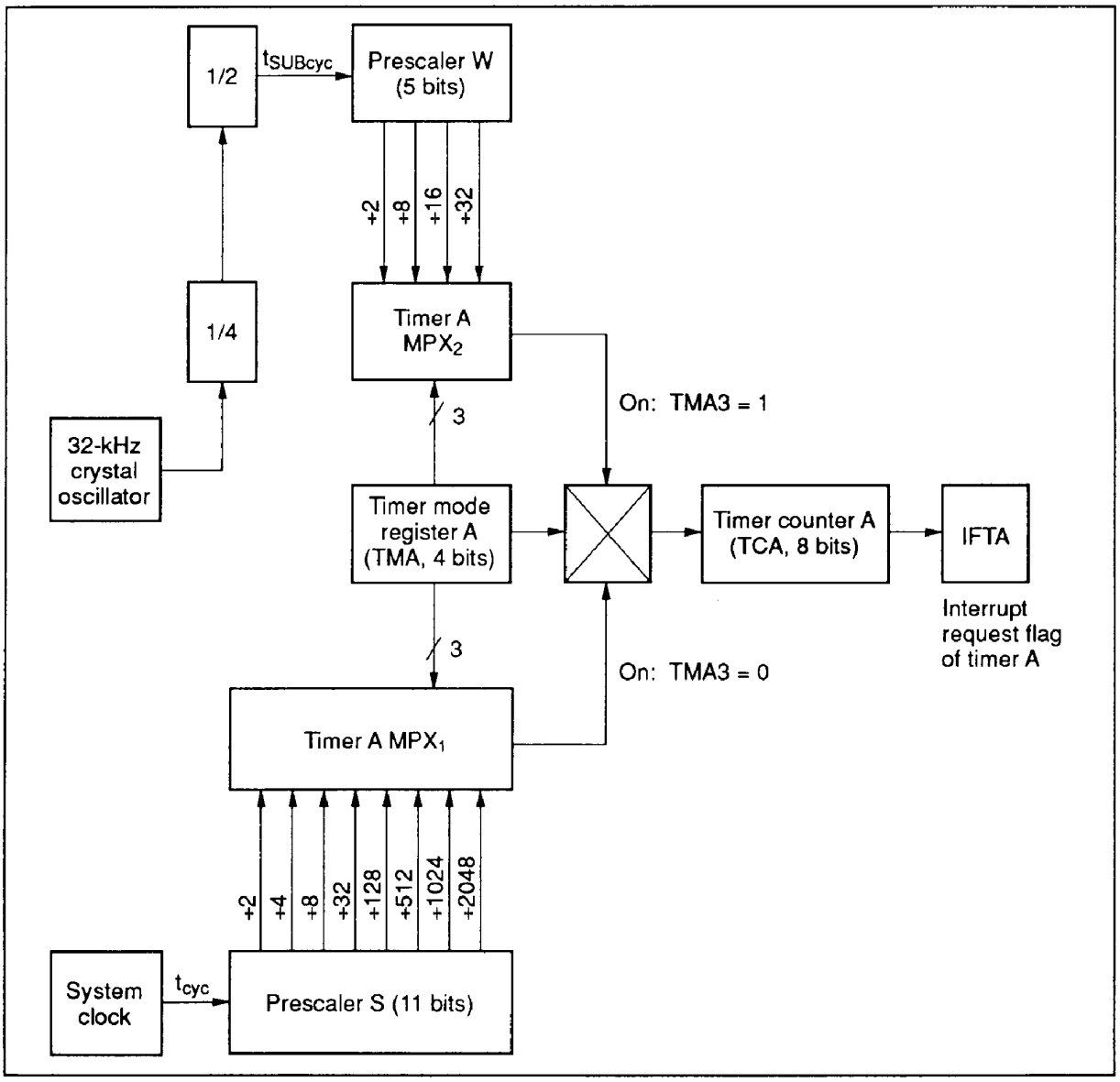


Figure 23 Block Diagram of Timer A

Table 26 Timers A, B, and C Function Selection

Timer A Condition	Function
TMA3 = 0	System clock-base interval timer
TMA3 = 1	Clock time-base

Timer B Condition	Function
TMB2–TMB0 ≠ 111	Automatic reloading timer
TMB2–TMB0 = 111 and PMRA3 = 1	Event counter (Pin $R7_1/\overline{INT_1}$ is specified as $\overline{INT_1}$)

Timer C Condition	Function
WDON = 0 (PMRB2 = 1)	Automatic reloading timer (Pin RB_0/TOC is specified as TOC)
WDON = 1	Watchdog timer

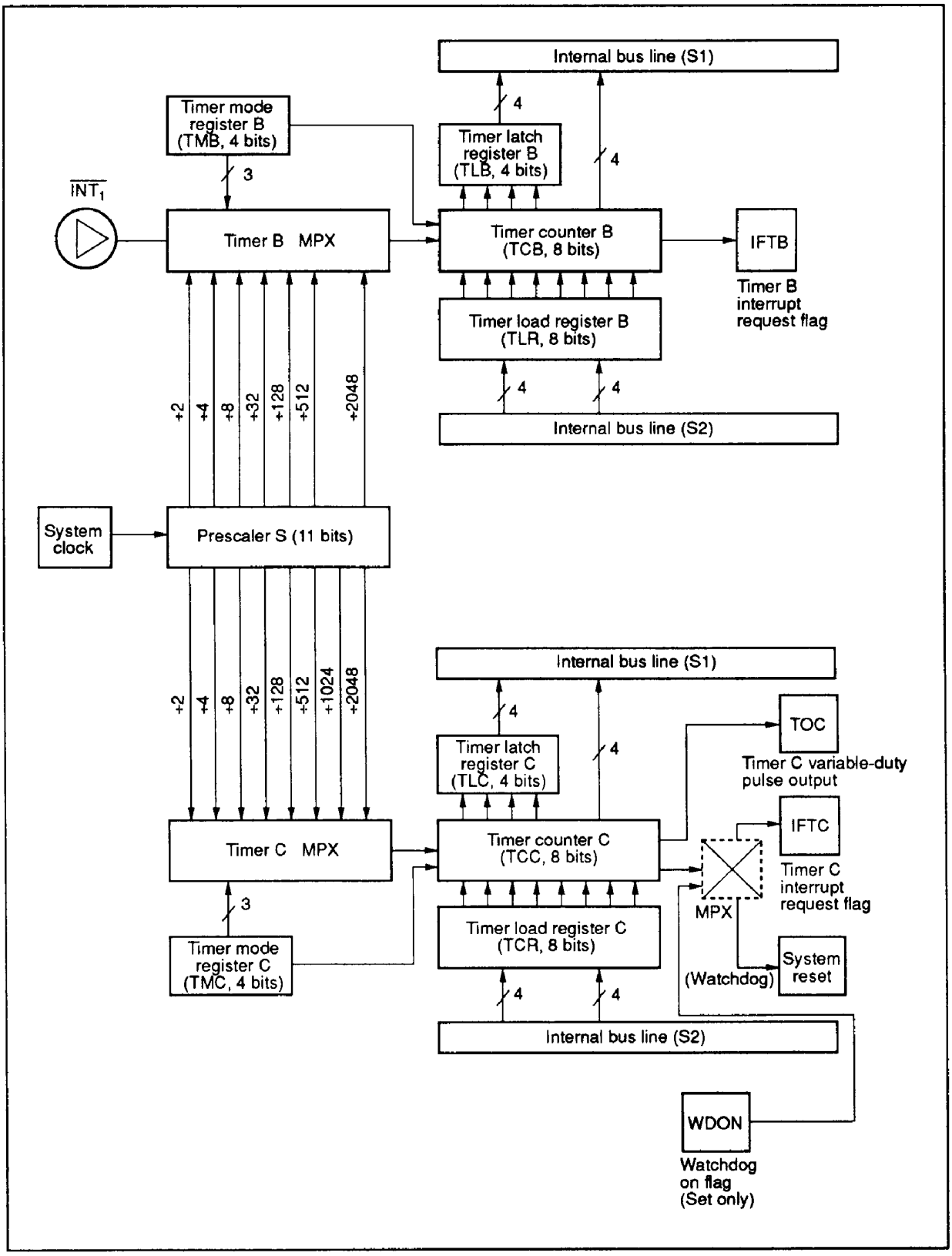


Figure 24 Block Diagram of Timers B and C

Timer A: Eight-bit timer which can be used as a clock time-base. Timer A is initialized to $00 by reset, then incremented by each input clock. If an input clock is applied to timer A after it has reached $FF, an overflow that sets the timer A interrupt request flag (IFTA: $002, bit 2) is generated, and timer A restarts from $00. Timer A is an interval timer which overflows every 256 clock inputs.

Timer A can also be used as a clock time-base when the TMA3 bit of timer mode register A (TMA) is set to 1. The timer is driven by the 32.768-kHz oscillator clock frequency divided by prescaler W. In this case, prescaler W and timer A can be initialized by software. The input clock of timer A is controlled by TMA.

Timer B (TCBL: $00A, TCBU: $00B, TLRL: $00A, TLRU: $00B): Eight-bit write-only timer load register (TLRL and TLRU) and read-only timer counter (TCBL and TCBU) located at the same address. The eight-bit configuration consists of lower and upper digits located at sequential addresses.

Timer counter B is initialized by writing data to timer load register B (TLR). In this case, the lower digit must be written first. Both the upper and lower digits of TLR are loaded into the timer counter at the same time the upper digit is written to TLR. TLR is initialized to $00 by MCU reset.

The count of timer B is obtained by reading timer counter B. In this case, the upper digit must be read first; the count is latched at the same time the upper digit is read.

An automatic reloading function, input clock source, and prescaler division ratio of timer B are selected by timer mode register B (TMB). When an external event input is used as the input clock source of timer B, the $R7_1/\overline{INT_1}$ pin must be specified as the $\overline{INT_1}$ pin by port mode register A (PMRA: $004) and the external interrupt mask (IM1) must be set to inhibit any $\overline{INT_1}$ interrupt request.

Timer B is initialized to the value set in timer load register B (TLR) by software, and is then incremented by one every clock input. If an input clock is applied to timer B after it has reached $FF, an overflow is generated. In this case, if the automatic reloading function is enabled, timer B is initialized to its initial value; if reloading is disabled, the timer is initialized to $00. The overflow sets the timer B interrupt request flag (IFTB: $003, bit 0).

Timer C (TCCL: $00E, TCCU: $00F, TCRL: $00E, TCRU: $00F): Eight-bit write-only timer load register (TCRL and TCRU) and read-only timer counter (TCCL and TCCU) located at the same address. The eight-bit configuration consists of lower and upper digits located at sequential addresses. The operation of timer C is basically the same as that of timer B.

An automatic reloading function and prescaler division ratio of timer C depend on the state of timer mode register C (TMC). Timer C is initialized to the value set in the TMC by software, and is then incremented by one every clock input. If an input clock is applied to timer C after it has reached $FF, an overflow is generated. In this case, if the automatic reloading function is enabled, timer C is initialized to its initial value; if the function is disabled, the timer is initialized to $00. The overflow sets the timer C interrupt request flag (IFTC: $003, bit 2).

Timer C also functions as a watchdog timer. The watchdog timer functions while the watchdog on (WDON) flag is set, and the MCU is reset by an overflow from timer C. If a program routine goes out of control, it can be detected by controlling the timer C reset before the count has reached $FF. Only a 1 can be written to the watchdog on flag. It can be cleared to 0 only by an MCU reset; it cannot be cleared by writing 0.

Timer C has a variable-duty pulse output (TOC) whose output waveform depends on the status of timer mode register C (TMC) and timer load register C (TCR) as shown in figure 25. For pulse output, the RB_0/TOC pins must be specified as TOC by port mode register B (PMRB).

Timer Mode Register A (TMA: $008): Four-bit write-only register which controls timer A as shown in table 27. It is initialized to $0 by MCU reset.

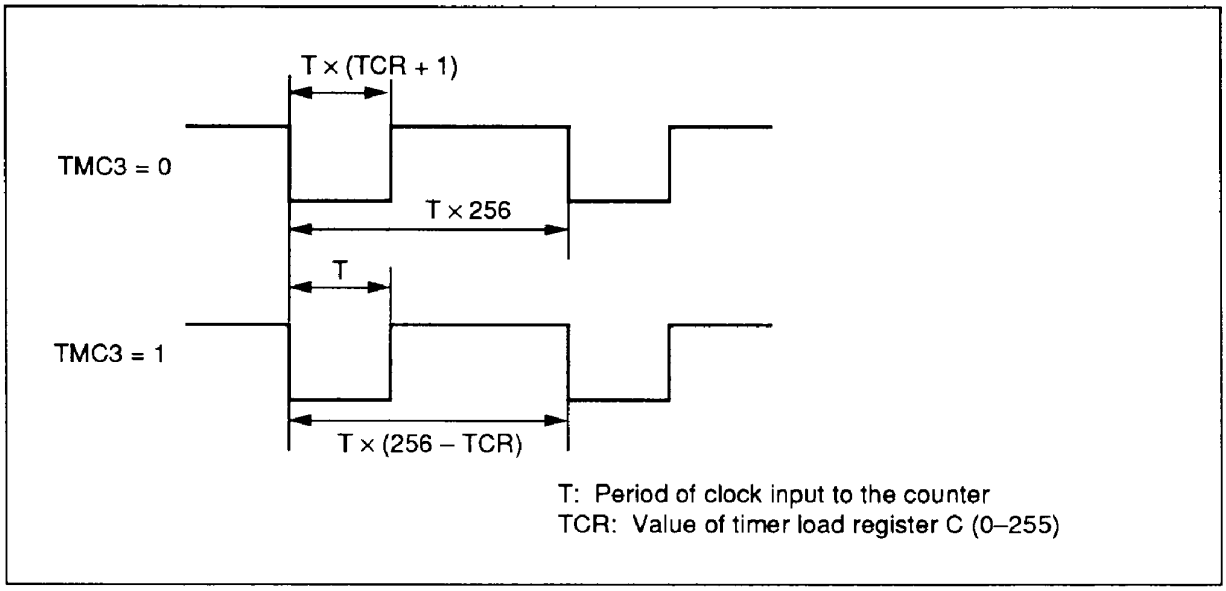


Figure 25 Variable-Duty Pulse Output Waveform

Table 27 Timer Mode Register A

TMA				Source Prescaler, Input Clock Period, Operating Mode	
Bit 3	Bit 2	Bit 1	Bit 0		
0	0	0	0	PSS, 2048 t_{cyc}	Timer A mode
			1	PSS, 1024 t_{cyc}	
		1	0	PSS, 512 t_{cyc}	
			1	PSS, 128 t_{cyc}	
	1	0	0	PSS, 32 t_{cyc}	
			1	PSS, 8 t_{cyc}	
		1	0	PSS, 4 t_{cyc}	
			1	PSS, 2 t_{cyc}	
1	0	0	0	PSW, 32 t_{SUBcyc}	Time-base mode
			1	PSW, 16 t_{SUBcyc}	
		1	0	PSW, 8 t_{SUBcyc}	
			1	PSW, 2 t_{SUBcyc}	
	1	0	0	PSW, TCA reset	
			1		
		1	0		
			1		

Notes: 1. t_{SUBcyc} = 244.14 µs (when a 32.768-kHz crystal oscillator is used)
2. t_{cyc} = 0.9536 µs (when a 4.1943-MHz crystal oscillator is used)
3. Timer counter overflow output period(s) = Input clock period(s) × 256

Timer Mode Register B (TMB: $009): Four-bit write-only register which selects the automatic reloading function, input clock source, and the prescaler division ratio for timer B as shown in table 28. It is initialized to $0 by MCU reset.

Changes made to TMB are valid from the second instruction cycle after the write instruction is executed. Timer B must be programmed so that it is initialized by a write instruction to timer load register B (TLR) after a mode change becomes valid.

Table 28 Timer Mode Register B

TMB	
Bit 3	**Automatic Reloading**
0	Disabled
1	Enabled

TMB			
Bit 2	**Bit 1**	**Bit 0**	**Input Clock Period and Input Clock Source**
0	0	0	2048 t_{cyc}
0	0	1	512 t_{cyc}
0	1	0	128 t_{cyc}
0	1	1	32 t_{cyc}
1	0	0	8 t_{cyc}
1	0	1	4 t_{cyc}
1	1	0	2 t_{cyc}
1	1	1	$\overline{INT_1}$ (external event input)

Note: t_{cyc} = 0.9536 µs (when a 4.1943-MHz crystal oscillator with 1/4 division is used)

Timer Mode Register C (TMC: $00D): Four-bit write-only register which selects the automatic reloading function and the prescaler division ratio for timer C as shown in table 29. It is initialized to $0 by MCU reset.

Changes made to TMC are valid from the second instruction cycle after the write instruction is executed. Timer C must be programmed so that it is initialized by a write instruction to timer load register C (TCR) after a mode change becomes valid.

Table 29 Timer Mode Register C

TMC	
Bit 3	**Automatic Reloading**
0	Disabled
1	Enabled

TMC			
Bit 2	**Bit 1**	**Bit 0**	**Input Clock Period**
0	0	0	2048 t_{cyc}
0	0	1	1024 t_{cyc}
0	1	0	512 t_{cyc}
0	1	1	128 t_{cyc}
1	0	0	32 t_{cyc}
1	0	1	8 t_{cyc}
1	1	0	4 t_{cyc}
1	1	1	2 t_{cyc}

Note: t_{cyc} = 0.9536 µs (when a 4.1943-MHz crystal oscillator with 1/4 division is used)

Timer D (TCDL: $011, TCDU: $012, TDRL: $011, TDRU: $012): Eight-bit write-only timer load register (TDRL and TDRU) and read-only timer counter (TCDL and TCDU) located at the same address. The eight-bit configuration consists of lower and upper digits located at sequential addresses.

An automatic reloading function and prescaler division ratio of timer D are selected by timer mode register D (TMD). Timer D is initialized to the value set in timer load register D (TDR) by software, and is then incremented by one every clock input. If an input clock is applied to timer D after it has reached $FF, an overflow is generated. In this case, if the automatic reloading function is enabled, timer D is initialized to its initial value; if reloading is disabled, the timer is initialized to $00. The overflow sets the timer D interrupt request flag (IFTD: $021, bit 0).

Timer D has a variable-duty pulse output (TOD), whose output waveform depends on the states of timer mode register D (TMD) and timer load register D (TDR) as shown in figure 27. For pulse output, the RB_1/TOD pin must be specified as TOD by port mode register B (PMRB).

Timer Mode Register D (TMD: $010): Four-bit write-only register which selects the automatic reloading function and the prescaler division ratio for timer D as shown in figure 28. It is initialized to $0 by MCU reset.

Changes made to TMD are valid from the second instruction cycle after the write instruction is executed. Timer D must be programmed so that it is initialized by a write instruction to timer load register D (TDR) after a mode change becomes valid.

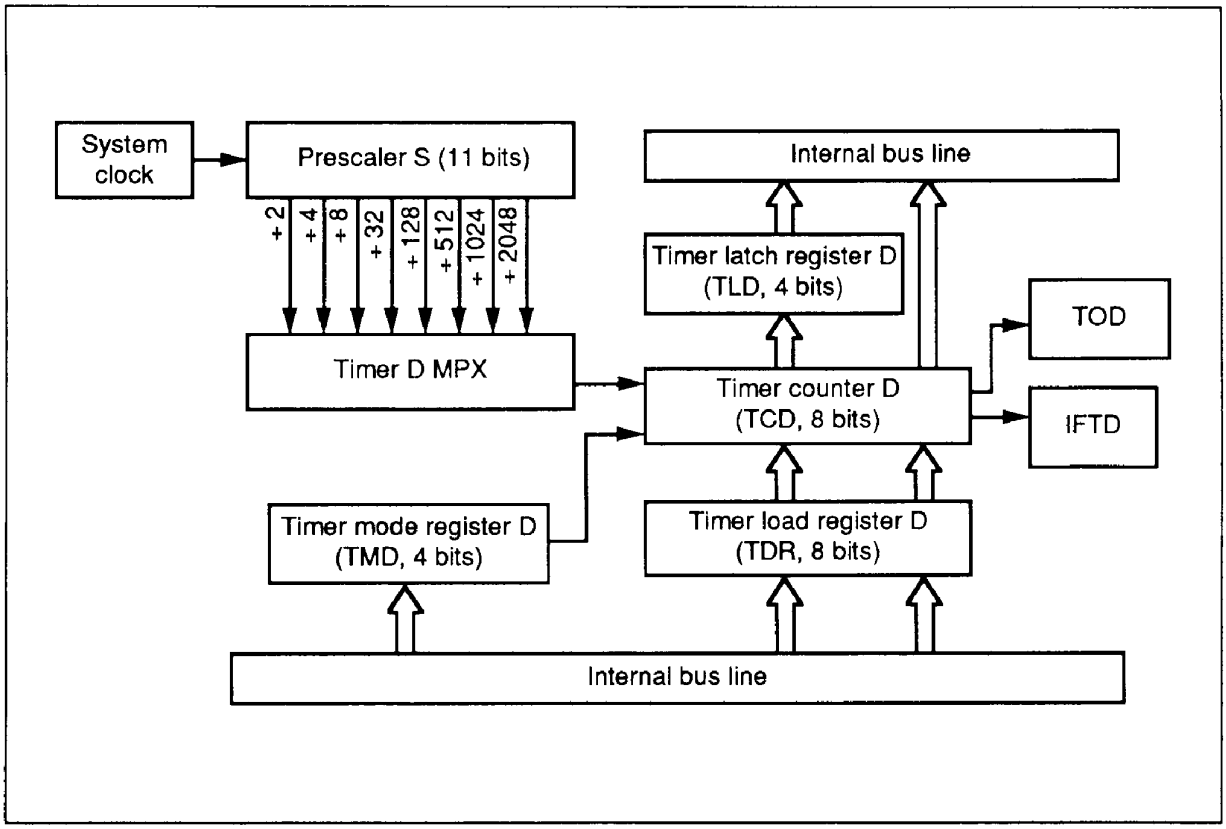


Figure 26 Block Diagram of Timer D

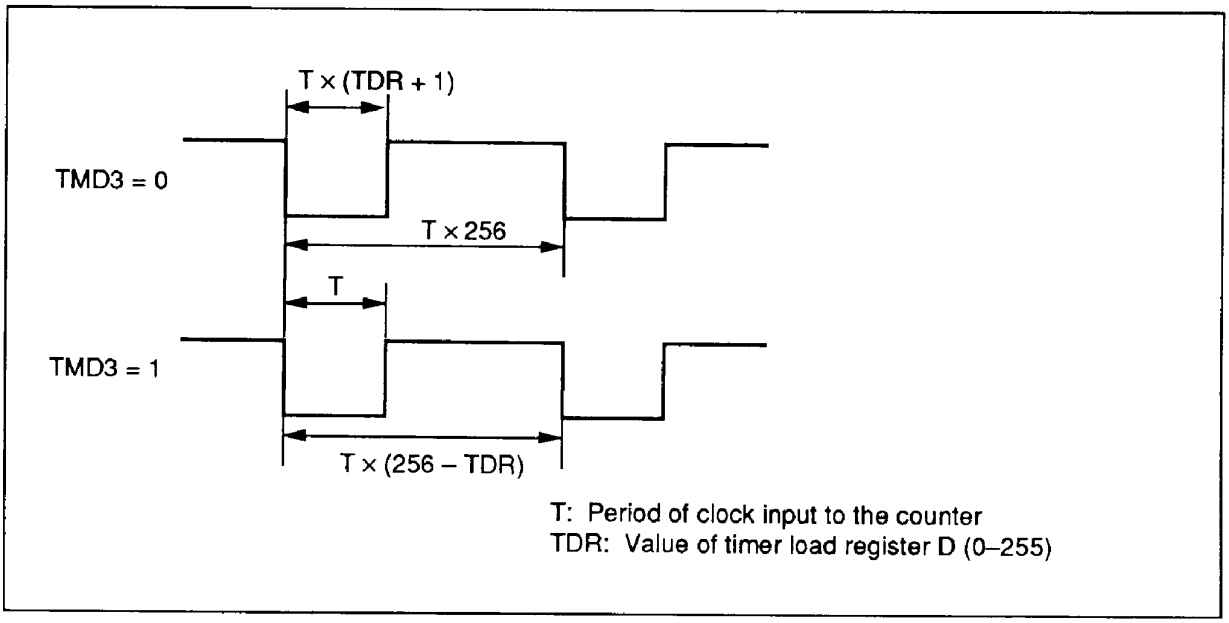
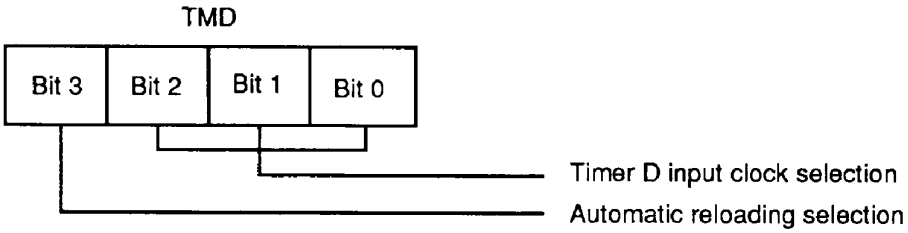


Figure 27 Variable-Duty Pulse Output Waveform



Bit 2	Bit 1	Bit 0	Input Clock Period
0	0	0	2048 t_{cyc}
0	0	1	1024 t_{cyc}
0	1	0	512 t_{cyc}
0	1	1	128 t_{cyc}
1	0	0	32 t_{cyc}
1	0	1	8 t_{cyc}
1	1	0	4 t_{cyc}
1	1	1	2 t_{cyc}

Bit 3	Automatic Reloading Function
0	Disabled
1	Enabled

Figure 28 Timer Mode Register D

Timer E: Outputs two variable-duty pulses (PWM). The duty ratio can be selected by the setting of the load register (figure 30). To write data into the load register, timer buffer register E must be written to first. Data written to the buffer register is transferred to the load register by an overflow from the prescaler. Since the two channels use the same buffer register, the destination load register is selected by the bit 2 setting of the timer mode register (TME). The completion of data transfer from the buffer register to the load register can be checked by reading bit 3 of TME.

Timer Mode Register E (TME: $025): Four-bit register including three write-only bits and one read-only bit which selects the port and the load register and indicates the buffer register status.

Timer Buffer Register E (TBEL: $026, TBEU: $027): Eight-bit write-only register. The lower digit must be written first. When the upper digit is written, bit 3 of timer mode register E is automatically set to 1. When the data in timer mode register E is loaded to the load register, bit 3 of timer mode register E is automatically reset to 0.

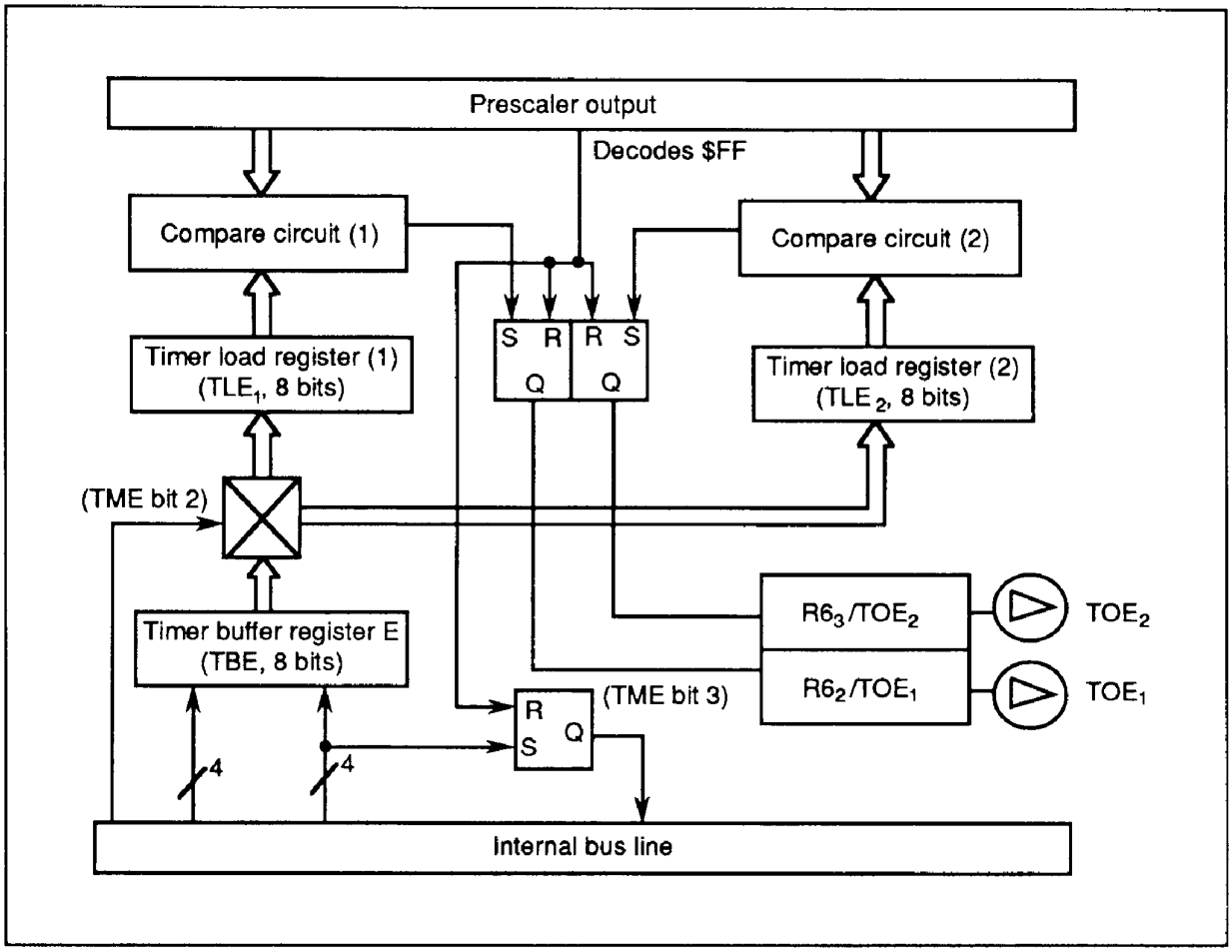


Figure 29 Block Diagram of Timer E

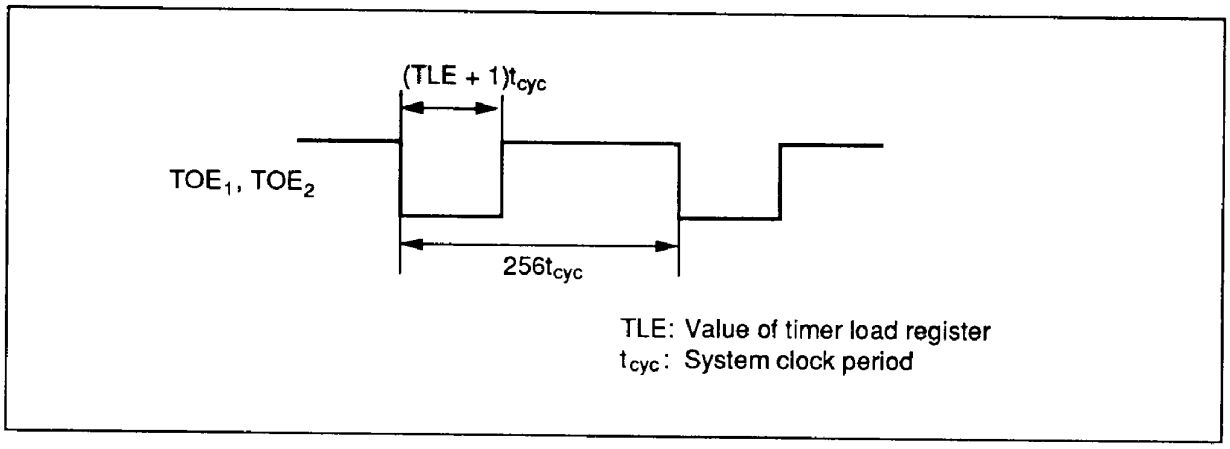
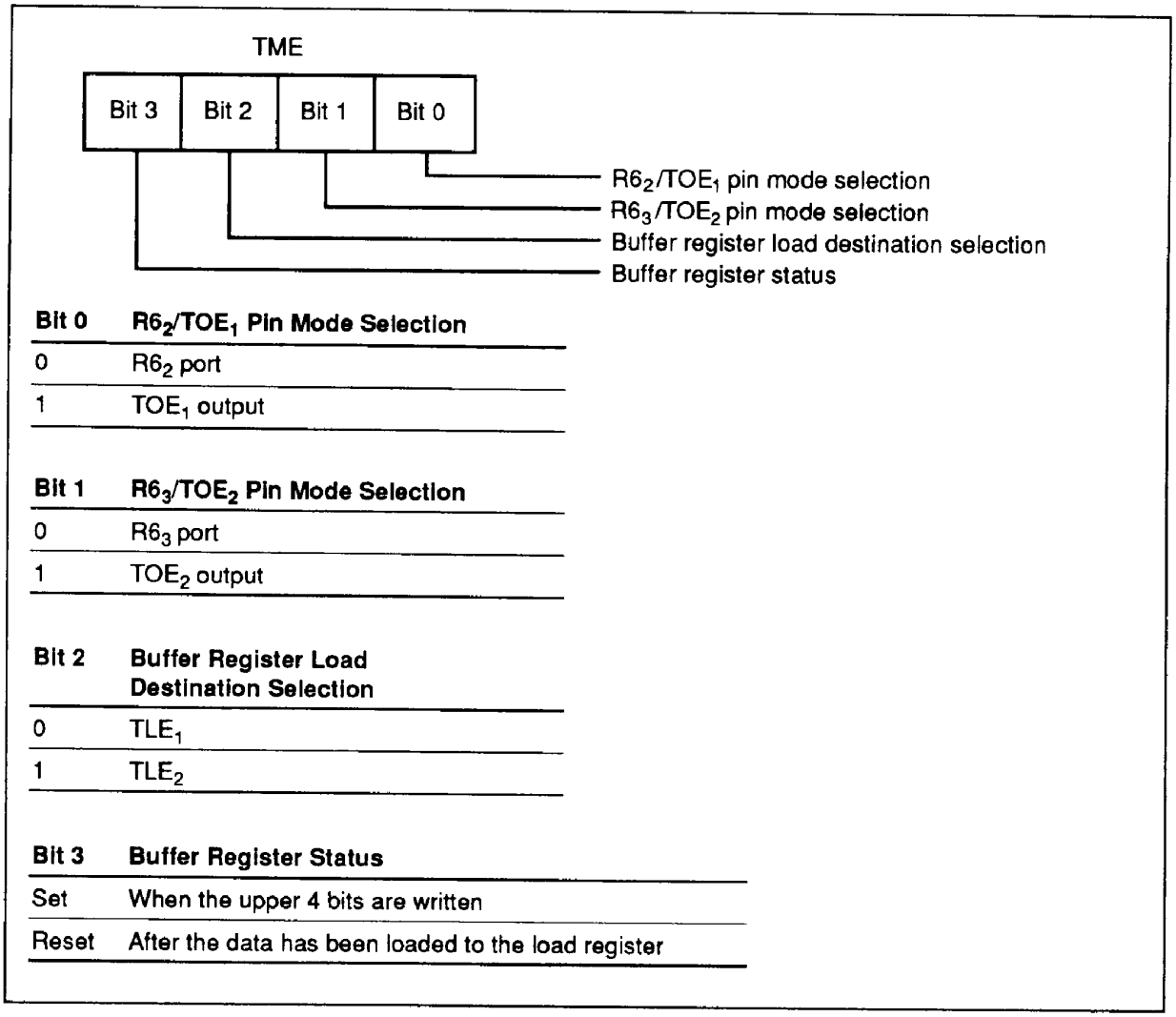


Figure 30 Variable-Duty Pulse Output Waveform



Bit 0	$R6_2/TOE_1$ Pin Mode Selection
0	$R6_2$ port
1	TOE_1 output

Bit 1	$R6_3/TOE_2$ Pin Mode Selection
0	$R6_3$ port
1	TOE_2 output

Bit 2	Buffer Register Load Destination Selection
0	TLE_1
1	TLE_2

Bit 3	Buffer Register Status
Set	When the upper 4 bits are written
Reset	After the data has been loaded to the load register

Figure 31 Timer Mode Register E

Input Capture Timer: Eight-bit counter and 8-bit input capture register. Free-running counter operation or input capture operation can be selected by setting the input capture status register.

When the free-running counter operation is selected, the counter is incremented by one every prescaler clock input, whose division ratio is specified by the input capture control register. If an overflow is generated from the counter, the input capture interrupt request flag is set, and the counter is initialized to \$00. It is then incremented.

When the input capture operation is selected, the count of the 8-bit counter is loaded into the input capture register by every trigger edge input of ICT_0 or ICT_1. At this point, the input capture interrupt request flag and input capture status flag are set and the counter is initialized to \$00, and is then incremented. An external trigger input while the status flag is 1 or an overflow from the counter (when the counter continues to increment without receiving trigger input) sets bit 3 of the status register.

Input Capture Control Register (ICC: \$017): Four-bit write-only register which selects the pin function and the prescaler division ratio.

Input Capture Status Register (ICSR: \$018): Four-bit register which selects the input capture operation and the trigger input edge, and holds the operation status.

Input Capture Register (ICRL: \$019, ICRU: \$01A): Eight-bit read-only register which loads the contents of the counter by a trigger edge input of ICT_0 or ICT_1.

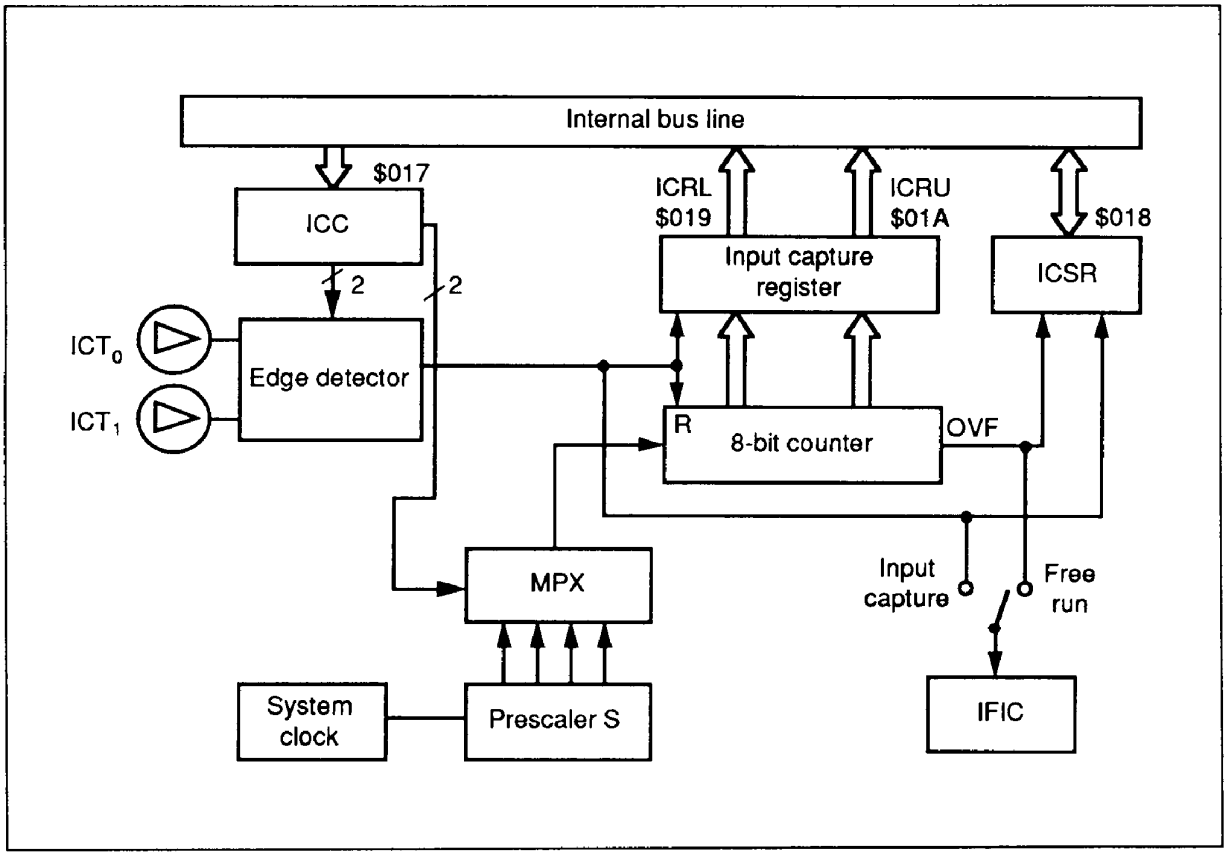
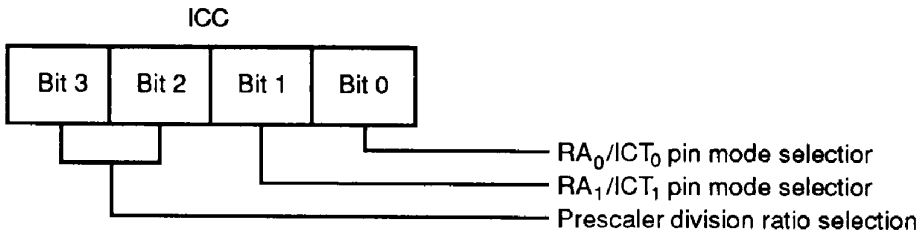


Figure 32 Block Diagram of Input Capture Timer



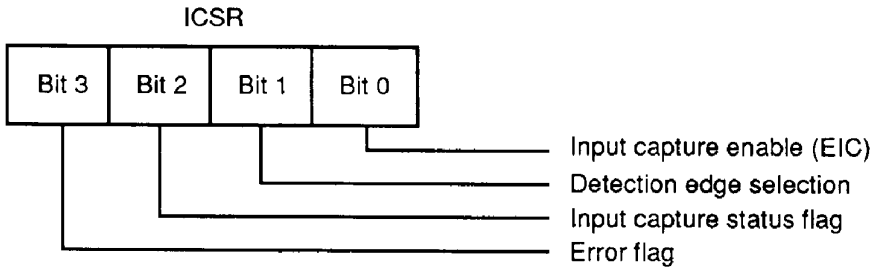
Bit 0	RA_0/ICT_0 Pin Mode Selection
0	RA_0 port
1	ICT_0 input

Bit 1	RA_1/ICT_1 Pin Mode Selection
0	RA_1 port
1	ICT_1 input

Bit 3	Bit 2	Prescaler Division Ratio
0	0	÷128
0	1	÷32
1	0	÷8
1	1	÷2

Note: Setting both bits 0 and 1 to 1 is inhibited.

Figure 33 Input Capture Control Register



Bit 0	Input Capture Enable (EIC)
0	Free-running counter operation enabled
1	Input capture operation enabled

Bit 1	Detection Edge Selection
0	Rising edge
1	Falling edge

Bit 2	Input Capture Status Flag
Set	When executing the input capture operation by external trigger input

Note: Read enabled. Only zero write enabled.

Bit 3	Error Flag
Set	By an external trigger input while the status flag is 1. By an overflow from the counter.

Note: Read enabled. Only zero write enabled.

Figure 34 Input Capture Status Register

Output Compare Timer: A 16-bit counter and 16-bit register. The output compare timer outputs a wave whose form changes at a specified timing. This timing to change the waveform can be selected as an overflow from the 16-bit counter, an input edge of $\overline{INT}_4$, or a trigger by software. An output of 1, an output of 0, or a toggle (inversion of the previous output value) can be selected as the output of pin TOG.

Timer counter G, the counter for output compare, is a 16-bit counter. The system clock or the system clock divided by 2 can be selected as the clock source. Timer counter G is a reloading counter. At the time of a counter overflow, an $\overline{INT}_4$ edge input, or a software trigger, the contents of timer load register G are loaded into timer counter G. An output compare interrupt is generated at the falling edge of $\overline{INT}_4$ or a counter overflow, depending on the selection set with bit 3 of the output compare control register.

When selecting a software trigger, set both bits 2 and 3 of the output compare control register to 1. At the same time the bits are set, pin TOG outputs a specified value and the contents of the load register are loaded into the counter.

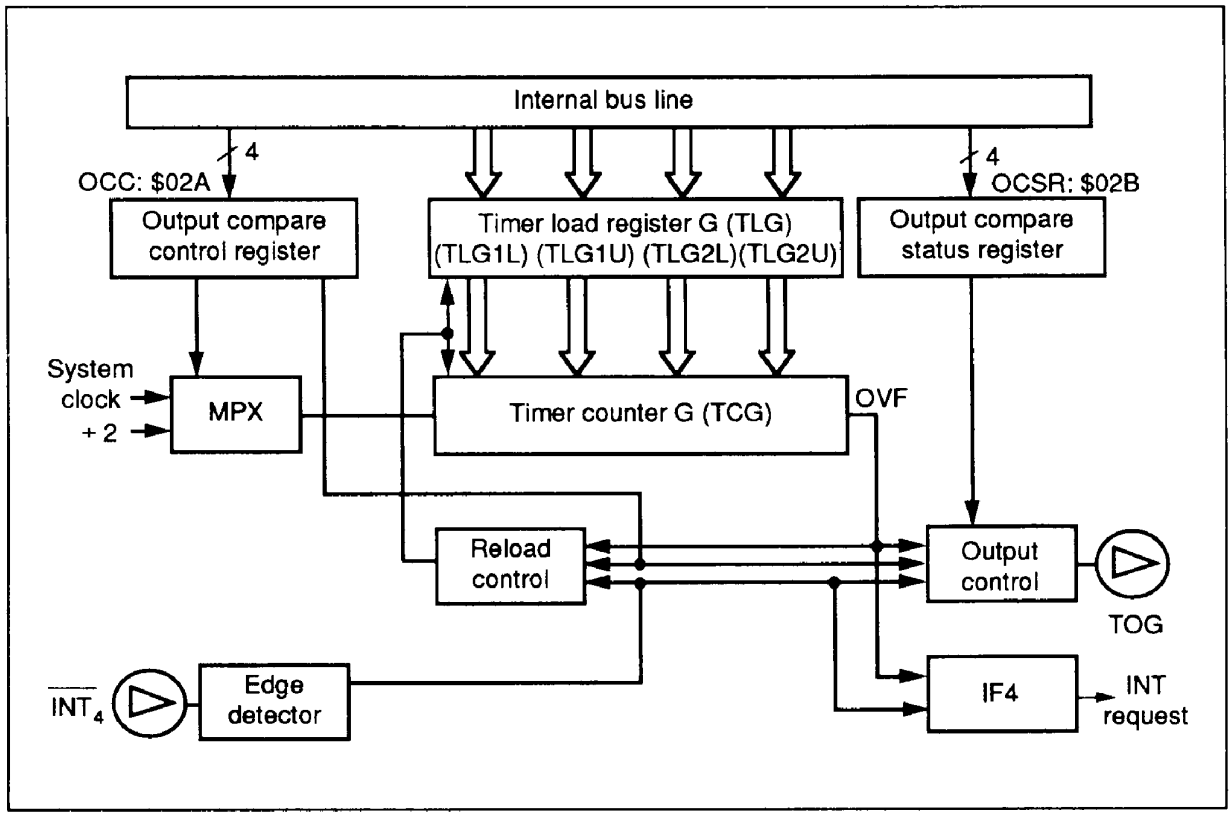
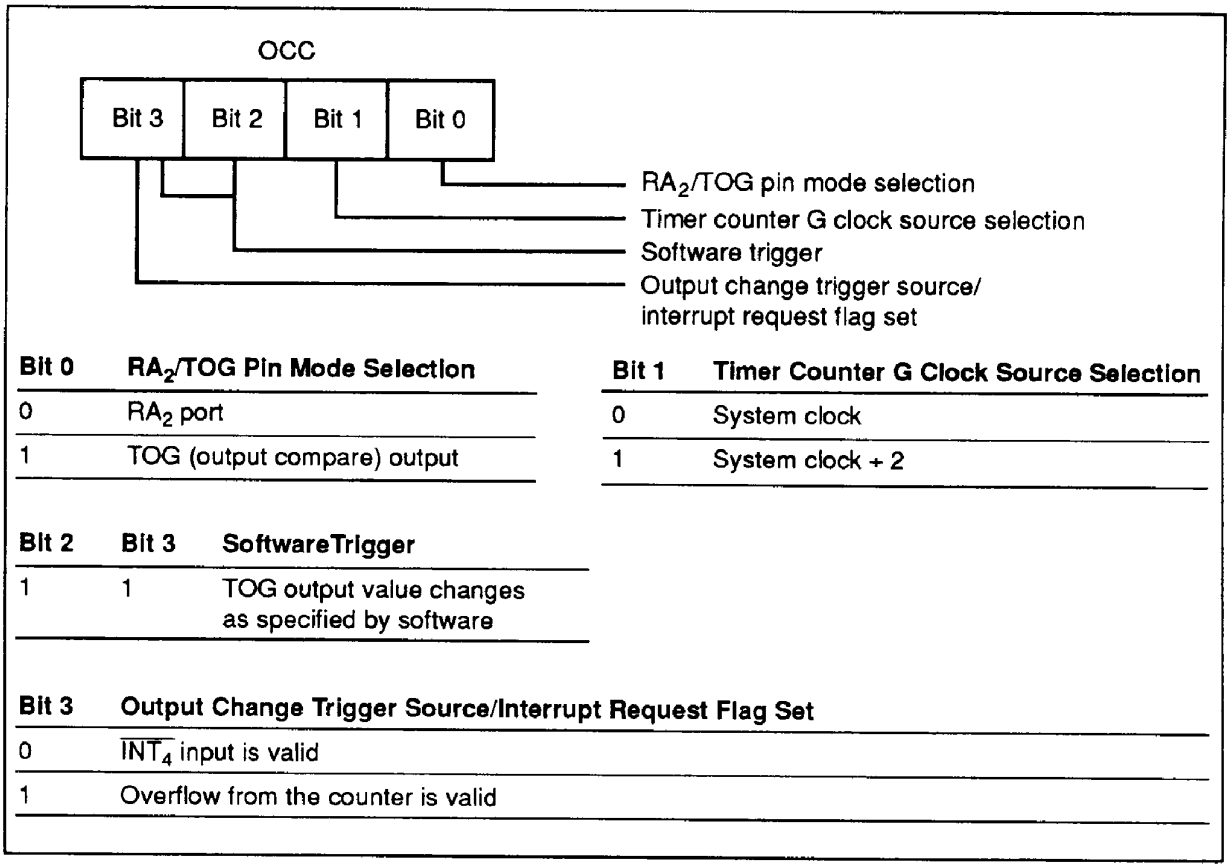


Figure 35 Block Diagram of Output Compare Timer



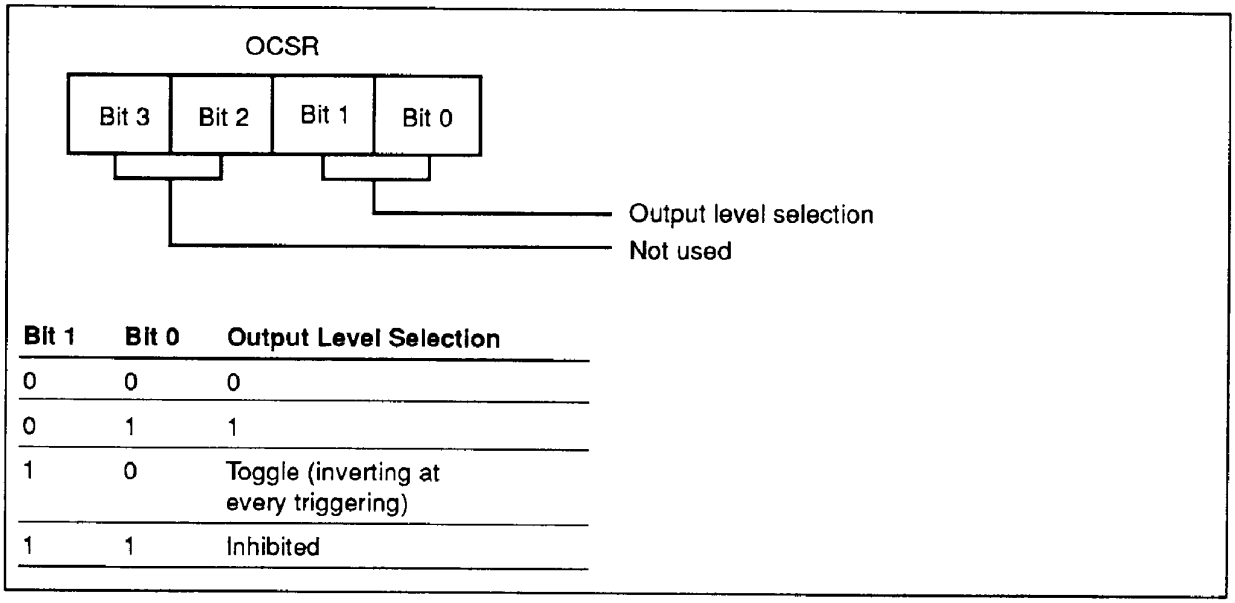
Bit 0	RA_2/TOG Pin Mode Selection
0	RA_2 port
1	TOG (output compare) output

Bit 1	Timer Counter G Clock Source Selection
0	System clock
1	System clock ÷ 2

Bit 2	Bit 3	SoftwareTrigger
1	1	TOG output value changes as specified by software

Bit 3	Output Change Trigger Source/Interrupt Request Flag Set
0	$\overline{INT_4}$ input is valid
1	Overflow from the counter is valid

Figure 36 Output Compare Control Register



Bit 1	Bit 0	Output Level Selection
0	0	0
0	1	1
1	0	Toggle (inverting at every triggering)
1	1	Inhibited

Figure 37 Output Compare Status Register

Buzzer Output Function: Outputs a wave which has a duty ratio of 50% of the clock rate specified by the buzzer control register (BCR). To output a buzzer, the RA_3/BUZZ pin must be fixed as BUZZ by setting bit 3 of the buzzer control register.

Buzzer Control Register (BCR: $029): Four-bit write-only register which selects the port and the output wave frequency.

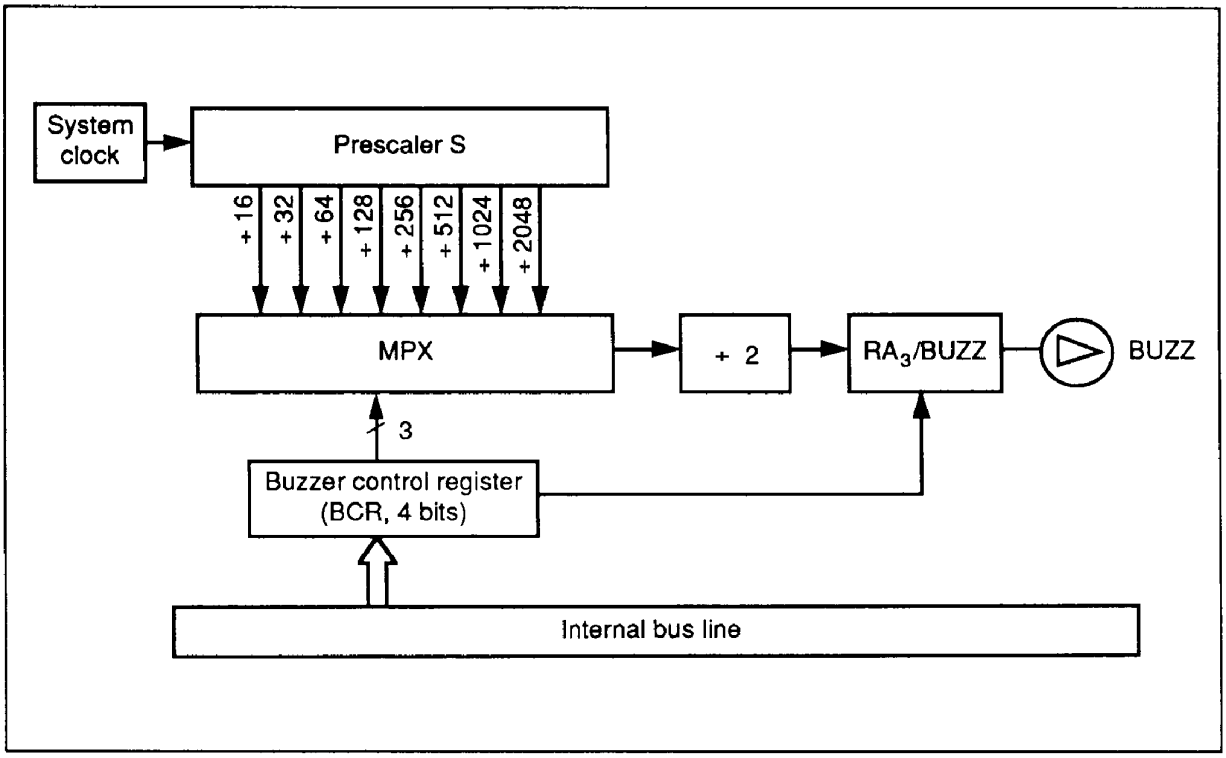
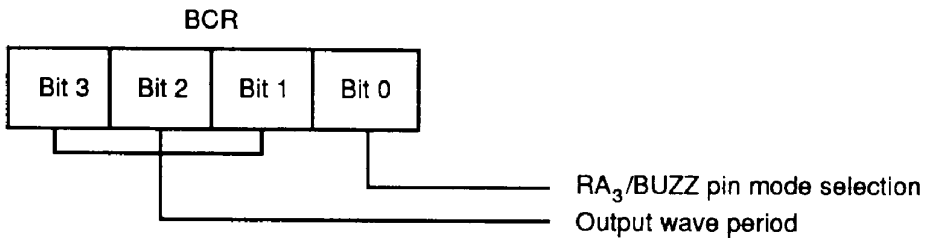


Figure 38 Block Diagram of Buzzer Output



Bit 0	RA_3/BUZZ Pin Mode Selection
0	RA_3 port
1	BUZZ output

Bit 3	Bit 2	Bit 1	Output Wave Period
0	0	0	4096 t_{cyc}
0	0	1	2048 t_{cyc}
0	1	0	1024 t_{cyc}
0	1	1	512 t_{cyc}
1	0	0	256 t_{cyc}
1	0	1	128 t_{cyc}
1	1	0	64 t_{cyc}
1	1	1	32 t_{cyc}

Figure 39 Buzzer Control Register

Serial Interface

The MCU has two clock-synchronous 8-bit serial interfaces (serial interface 1 and serial interface 2). The clock source is a prescaler, which is also used by the timers.

Serial Interface 1: Used to serially transmit and receive 8-bit data. It consists of serial data register 1 (SR1), serial mode register 1 (SMR1), port mode register A (PMRA), an octal counter, and a multiplexer as shown in figure 40. The $R9_0/\overline{SCK_1}$ pin and the transmit clock are controlled by writing data to SMR1. The transmit clock shifts the contents of SR1, which can be read and written to by software. In this way, 8-bit data is transferred.

Serial interface 1 is activated by the STS instruction. The octal counter is reset to $0 by the STS instruction, it starts counting at the falling edge of the transmit clock ($\overline{SCK_1}$), and it increments at the rising edge of the clock. When the eighth transmit clock signal is input (serial interface 1 is reset) or when serial transmission is discontinued (octal counter is reset), the serial 1 interrupt request flag (IFS1) is set.

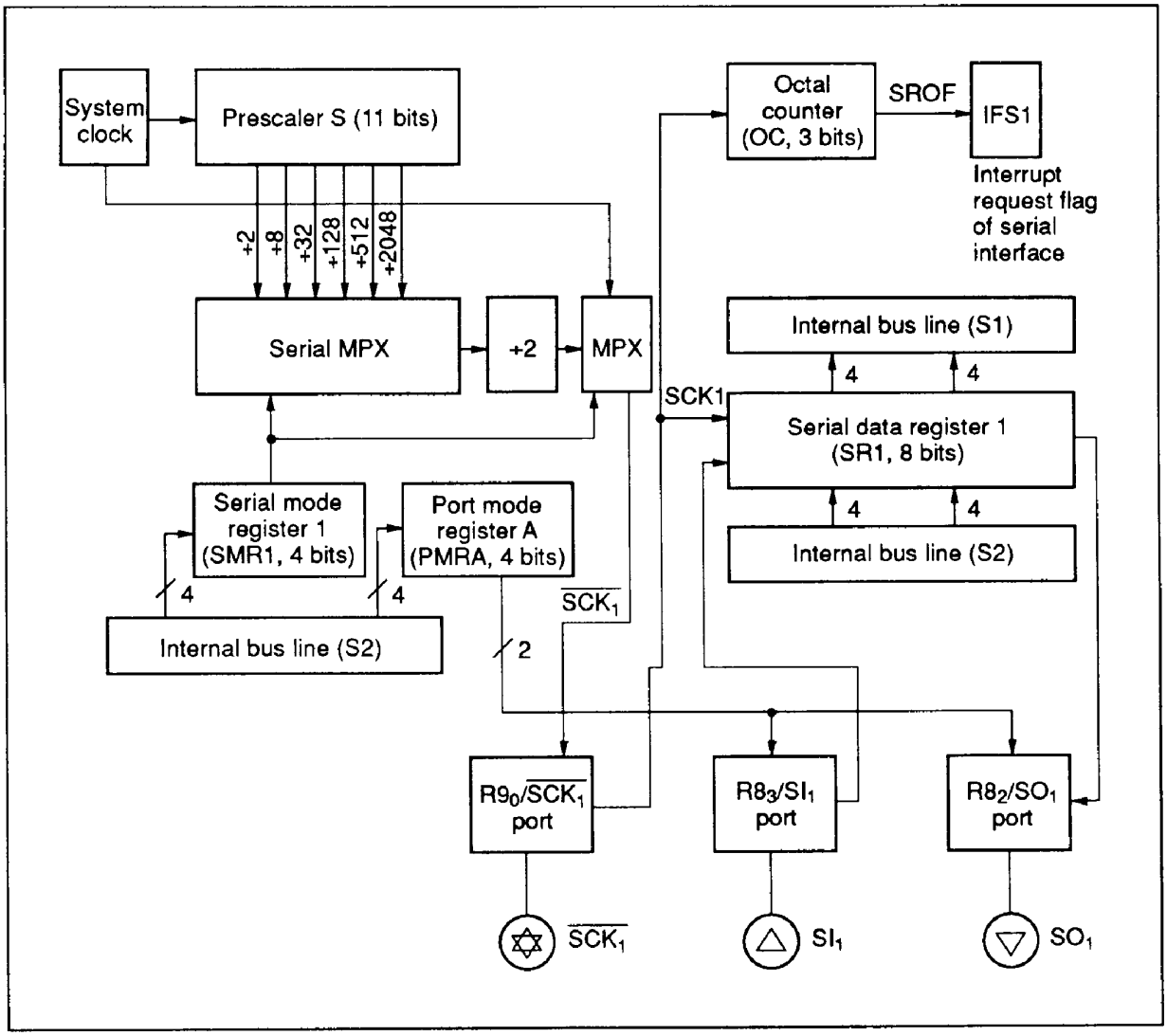
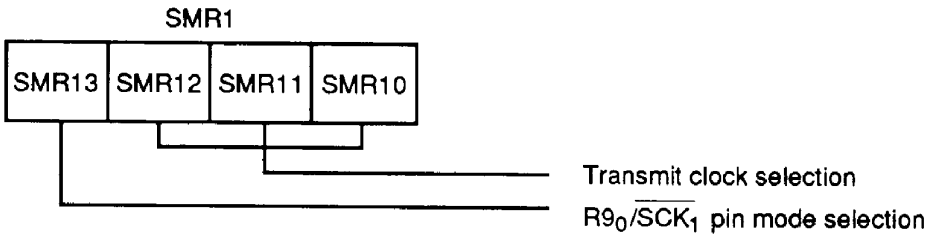


Figure 40 Serial Interface 1 Block Diagram

Serial Mode Register 1 (SMR1: $005): Four-bit write-only register which controls the $R9_0/\overline{SCK_1}$ pin, transmit clock, and prescaler division ratio for serial interface 1 as shown in figure 41. Writing to SMR1 initializes serial interface 1.

A write signal input to SMR1 discontinues the input of the transmit clock to serial data register 1 (SR1) and the octal counter. Therefore, if a write occurs during data transmission, the octal counter is reset to $0 to stop transmission, and, at the same time, the serial 1 interrupt request flag (IFS1) is set.

The contents of the serial mode register are not valid until the second instruction cycle after the write instruction execution. The user must program the STS instruction to be executed after this instruction cycle. The serial mode register is initialized to $0 by MCU reset.



SMR13	$R9_0/\overline{SCK_1}$ Pin
0	$R9_0$ port input/output pin
1	$\overline{SCK_1}$ input/output pin

			Transmit Clock			
SMR12	SMR11	SMR10	$R9_0/\overline{SCK_1}$ Pin	Clock Source	Prescaler Division Ratio	Transmit Clock Period
0	0	0	$\overline{SCK_1}$ output	Prescaler	÷ 2048	4096 t_{cyc}
0	0	1	$\overline{SCK_1}$ output	Prescaler	÷ 512	1024 t_{cyc}
0	1	0	$\overline{SCK_1}$ output	Prescaler	÷ 128	256 t_{cyc}
0	1	1	$\overline{SCK_1}$ output	Prescaler	÷ 32	64 t_{cyc}
1	0	0	$\overline{SCK_1}$ output	Prescaler	÷ 8	16 t_{cyc}
1	0	1	$\overline{SCK_1}$ output	Prescaler	÷ 2	4 t_{cyc}
1	1	0	$\overline{SCK_1}$ output	System clock		t_{cyc}
1	1	1	$\overline{SCK_1}$ input	External clock		

Figure 41 Serial Mode Register 1

Serial Data Register 1 (SR1L: $006, SR1U: $007): Eight-bit read/write register separated into lower and upper digits located at sequential addresses. Data in this register is output from the SO_1 pin LSB first, synchronously with the falling edge of the transmit clock, and data is input to the LSB first through the SI_1 pin at the rising edge of the transmit clock. Input/output timing is shown in figure 42.

Data cannot be read or written during serial data transmission. If data is read or written during transmission, it cannot be guaranteed.

Selecting and Changing Operating Modes: The operating modes of serial interface 1 are shown in table 30. The combination of port mode register A (PMRA) and serial mode register 1 (SMR1) must be specified as shown in the table. To change the operating mode of serial interface 1, internally initialize serial interface 1 by writing to SMR1.

Table 30 Operating Modes of Serial Interface 1

SMR1	PMRA		
Bit 3	Bit 1	Bit 0	Operating Mode
1	0	0	Continuous clock output mode
1	0	1	Transmit mode
1	1	0	Receive mode
1	1	1	Transmit/receive mode

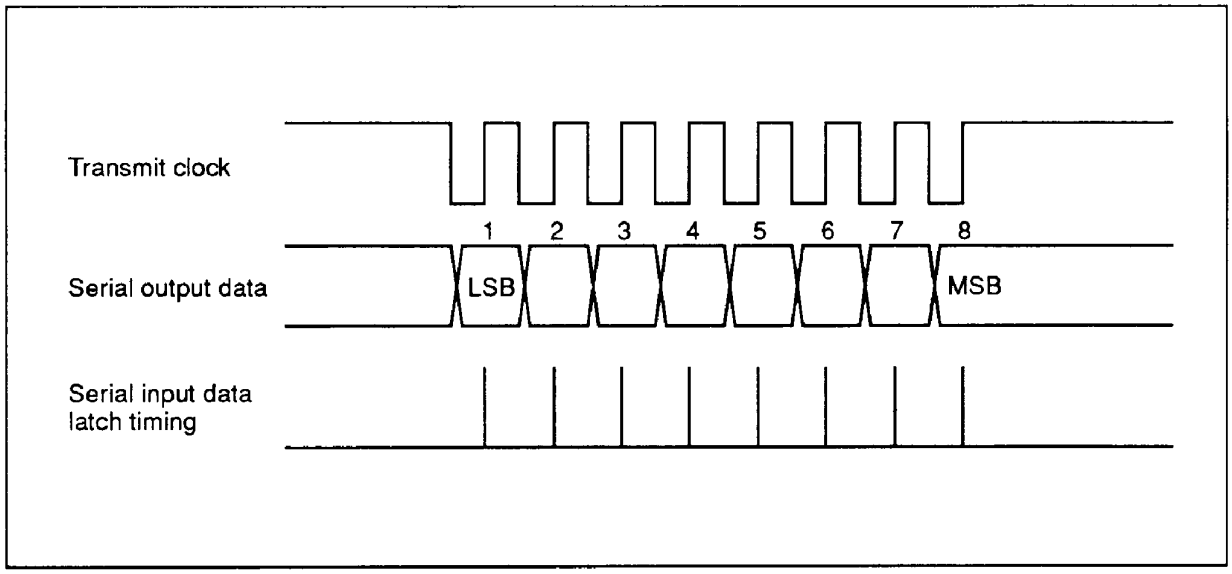


Figure 42 Serial Interface 1 Timing

Serial Interface 1 Operation: Three operating modes are provided for serial interface 1; transitions between them are shown in figure 43.

In STS wait state, serial interface 1 is initialized and the transmit clock is ignored. If the STS instruction is then executed, serial interface 1 enters transmit clock wait state.

In transmit clock wait state, input of the transmit clock increments the octal counter, shifts serial data register 1 (SR1), and starts serial transmission. However, note that if continuous clock output mode is selected, the transmit clock is continuously output, but data is not transmitted.

During transmission, the input of eight clocks or the execution of the STS instruction sets the octal counter to 000, and serial interface 1 enters transmit clock wait state. If an external transmit clock is further applied, serial interface 1 enters the transfer state. In this state, if the internal clock has been selected, the serial 1 interrupt flag is set, serial interface 1 enters STS instruction wait state, and serial transmission is stopped after the eighth clock is output.

If port mode register A (PMRA) is written to in transmit clock wait state or during transmission, serial mode register 1 (SMR1) must be written to, to initialize serial interface 1, after which serial interface 1 enters STS wait state.

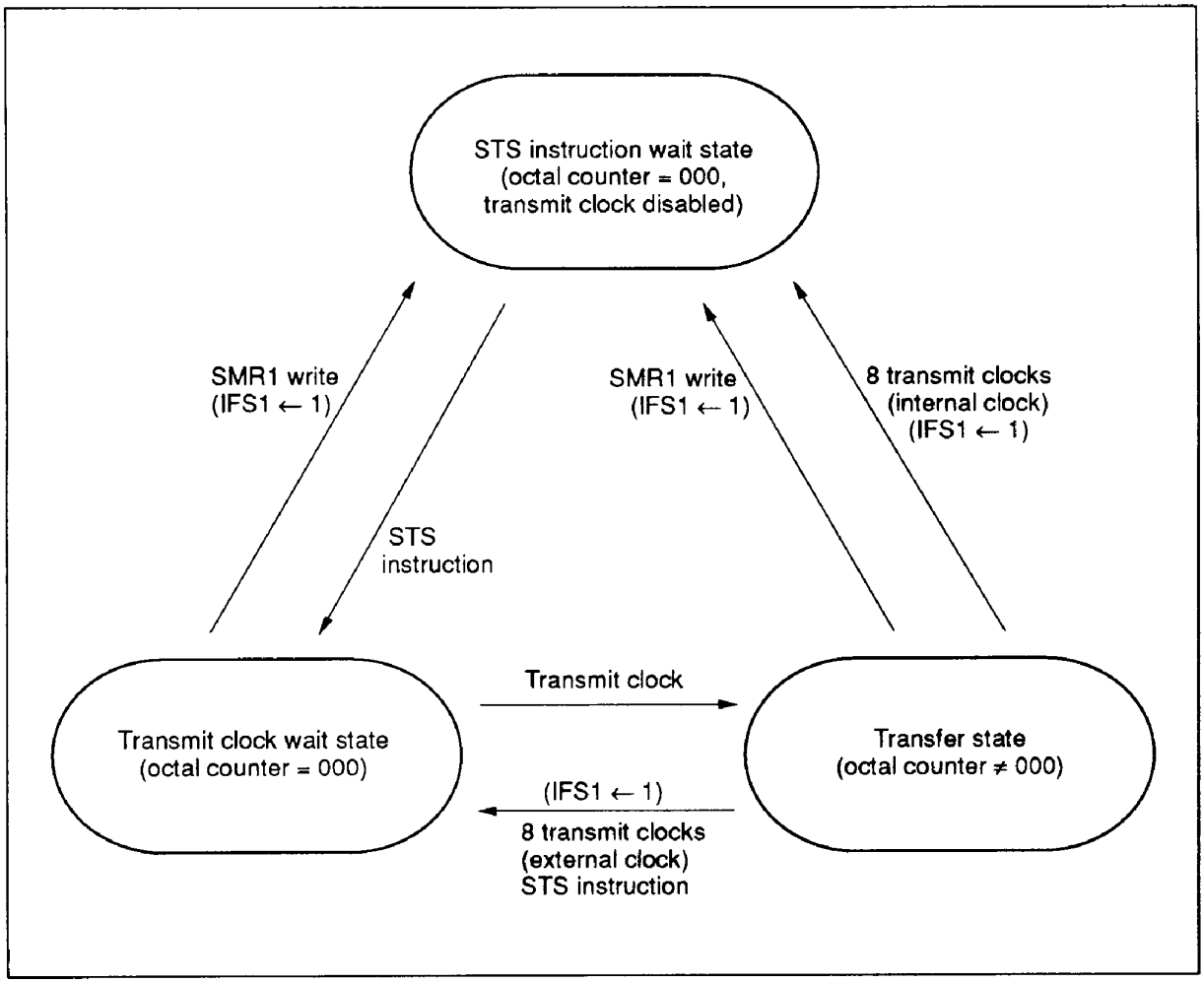


Figure 43 Serial Interface 1 Mode Transitions

Transmit Clock Error Detection: Serial interface 1 will malfunction if a spurious pulse caused by external noise conflicts with a normal transmit clock. Such errors can be detected as shown in figure 44.

If more than eight transmit clocks are input in transmit clock wait state, serial interface 1's state changes to transfer state, transmit clock wait state, then back to transfer state.

When serial interface 1 is set to STS wait state by writing data to SMR1 during transmission after the serial 1 interrupt request flag (IFS1) has been reset, the flag is set again.

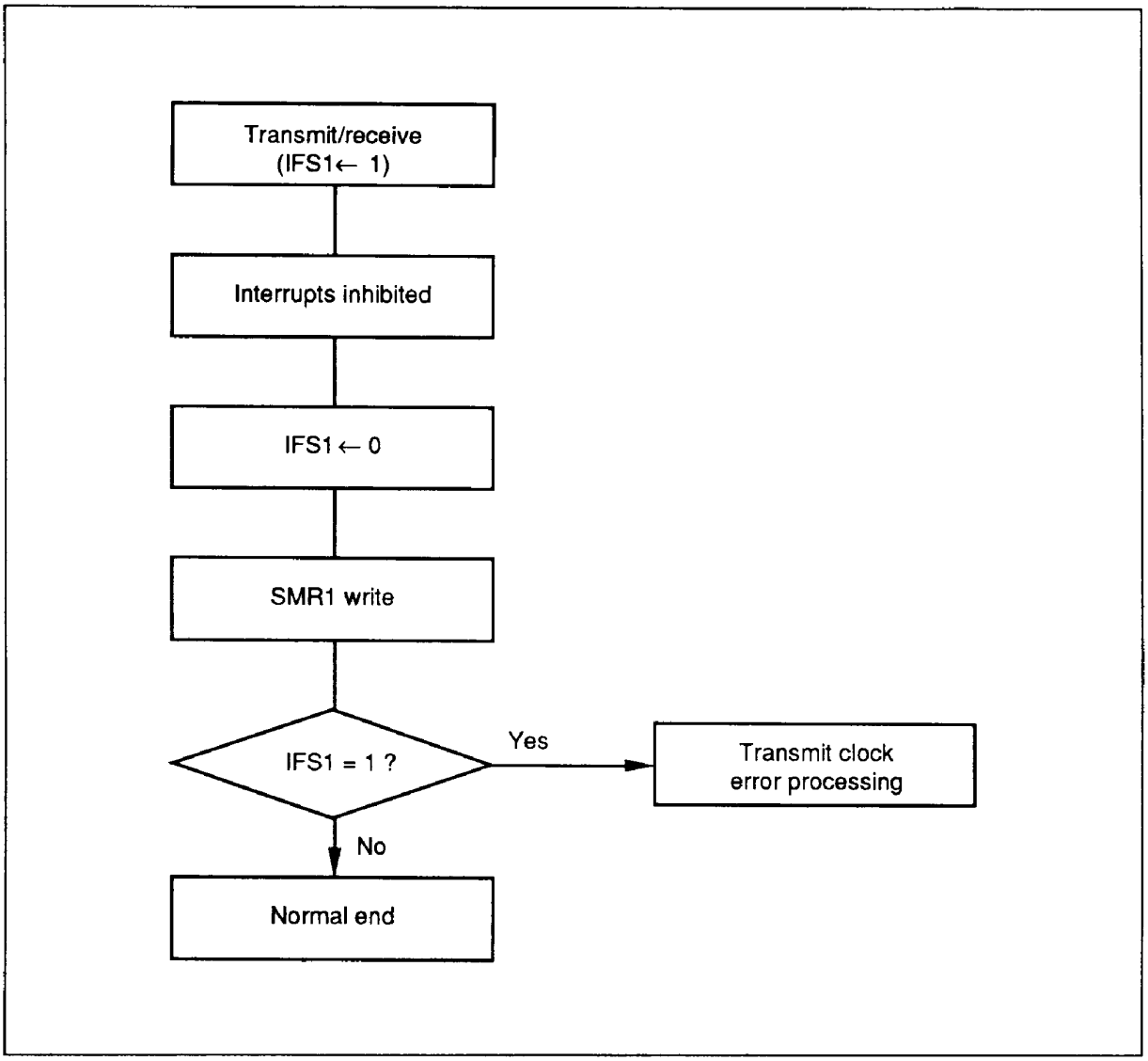


Figure 44 Transmit Clock Error Detection

Serial Interface 2: Used to serially transmit and receive 8-bit data. It consists of serial data register 2 (SR2), serial mode register 2 (SMR2), port mode register B (PMRB), an octal counter, and a multiplexer as shown in figure 45. The $R9_1/\overline{SCK_2}$ pin and the transmit clock are controlled by writing data to SMR2. The transmit clock shifts the contents of the SR2, which can be read and written to by software, and then transmission starts between two MCUs.

Serial interface 2 is activated by a read instruction for SMR2. The octal counter is reset to $0 by the read instruction for SMR2, it starts counting at the falling edge of the transmit clock ($\overline{SCK_2}$), and it increments at the rising edge of the clock. When the eighth transmit clock signal is input (serial interface 2 is reset) or when serial transmission is discontinued (octal counter is reset), the serial 2 interrupt request flag (IFS2) is set.

To start serial interface 2 by an SMR2 read, execute a compare instruction on SMR2 and the accumulator. Note that 0000 is read when write-only register SMR2 is accessed.

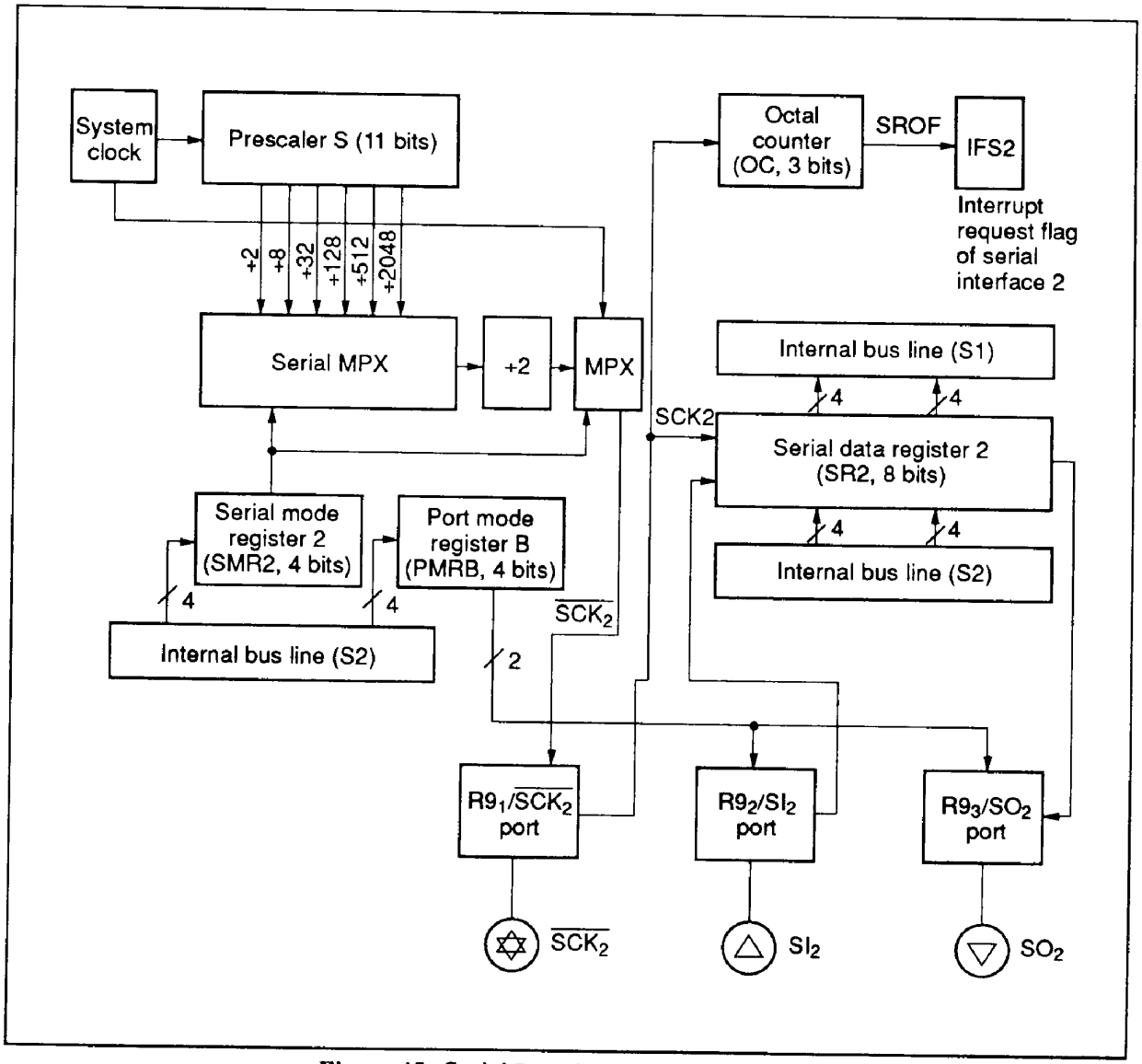
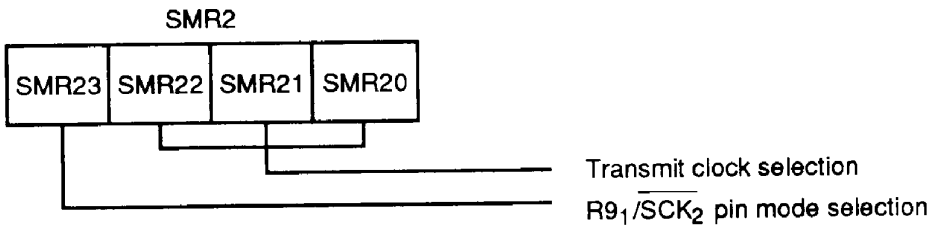


Figure 45 Serial Interface 2 Block Diagram

Serial Mode Register 2 (SMR2: $014): Four-bit write-only register which controls the $R9_1/\overline{SCK_2}$ pin, transmit clock, and prescaler division ratio as shown in figure 46. Writing to SMR2 initializes serial interface 2.

A write signal input to SMR2 discontinues the input of the transmit clock to serial data register 2 (SR2) and the octal counter. Therefore, if a write occurs during data transmission, the octal counter is reset to $0 to stop transmission, and, at the same time, the serial 2 interrupt request flag (IFS2) is set.

The contents of the serial mode register are not valid until the second instruction cycle after the write instruction execution. The user must program the SMR2 read instruction to be executed after this instruction cycle. The serial mode register is initialized to $0 by MCU reset.



SMR23	$R9_1/\overline{SCK_2}$
0	$R9_1$ port input/output pin
1	$\overline{SCK_2}$ input/output pin

			Transmit Clock			
SMR22	SMR21	SMR20	$R9_1/\overline{SCK_2}$ Pin	Clock Source	Prescaler Division Ratio	Transmit Clock Period
0	0	0	$\overline{SCK_2}$ output	Prescaler	+ 2048	4096 t_{cyc}
0	0	1	$\overline{SCK_2}$ output	Prescaler	+ 512	1024 t_{cyc}
0	1	0	$\overline{SCK_2}$ output	Prescaler	+ 128	256 t_{cyc}
0	1	1	$\overline{SCK_2}$ output	Prescaler	+ 32	64 t_{cyc}
1	0	0	$\overline{SCK_2}$ output	Prescaler	+ 8	16 t_{cyc}
1	0	1	$\overline{SCK_2}$ output	Prescaler	+ 2	4 t_{cyc}
1	1	0	$\overline{SCK_2}$ output	System clock		t_{cyc}
1	1	1	$\overline{SCK_2}$ input	External clock		

Figure 46 Serial Mode Register 2

Serial Data Register 2 (SR2L: $015, SR2U: $016): Eight-bit read/write register separated into lower and upper digits located at sequential addresses. Data in this register is output from the SO_2 pin LSB first, synchronously with the falling edge of the transmit clock, and data is input, LSB first through the SI_2 pin at the rising edge of the transmit clock. Input/output timing is shown in figure 47.

Data cannot be read or written during serial data transmission. If data is read or written during transmission, it cannot be guaranteed.

Selecting and Changing Operating Modes: Table 31 lists the operating modes of serial interface 2. The combination of port mode register B (PMRB) and serial mode register 2 (SMR2) must be specified as shown in the table. To change the operating mode of serial interface 2, internally initialize serial interface 2 by writing to SMR2.

Table 31 Operating Modes of Serial Interface 2

SMR2	PMRB		
Bit 3	Bit 1	Bit 0	Operating Mode
1	0	0	Continuous clock output mode
1	0	1	Transmit mode
1	1	0	Receive mode
1	1	1	Transmit/receive mode

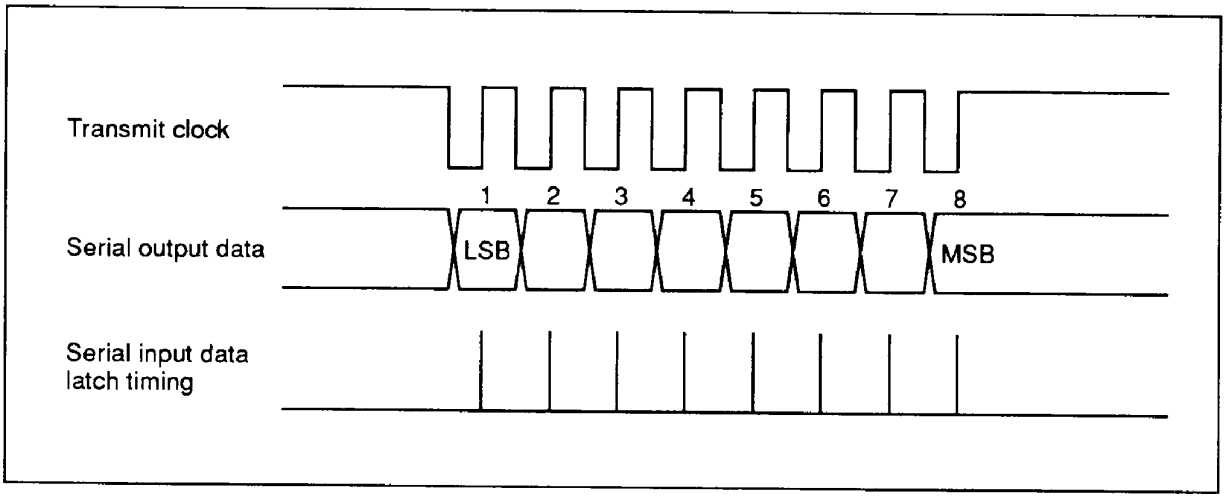


Figure 47 Serial Interface 2 Timing

Serial Interface 2 Operation: Three operating modes are provided for serial interface 2; transitions between them are shown in figure 48.

In SMR2 read wait state, serial interface 2 is initialized and the transmit clock is ignored. If an SMR2 read is executed, serial interface 2 enters transmit clock wait state.

In transmit clock wait state, input of the transmit clock increments the octal counter, shifts serial data register 2 (SR2), and starts serial transmission. However, note that if continuous clock output mode is selected, the transmit clock is continuously output, but data is not transmitted.

During transmission, the input of 8 clocks or a SMR2 read sets the octal counter to 000, and serial interface 2 enters transmit clock wait state. If an external transmit clock is further applied, serial interface 2 enters transfer state. If the internal clock has been selected, the serial 2 interrupt flag is set, serial interface 2 enters SMR2 read wait state, and serial transmisson is stopped after the eighth clock is output.

If port mode register B (PMRB) is written to in transmit clock wait state or during transmission, SMR2 must be written to, to initialize serial interface 2, after which serial interface 2 enters SMR2 read (serial start) wait state.

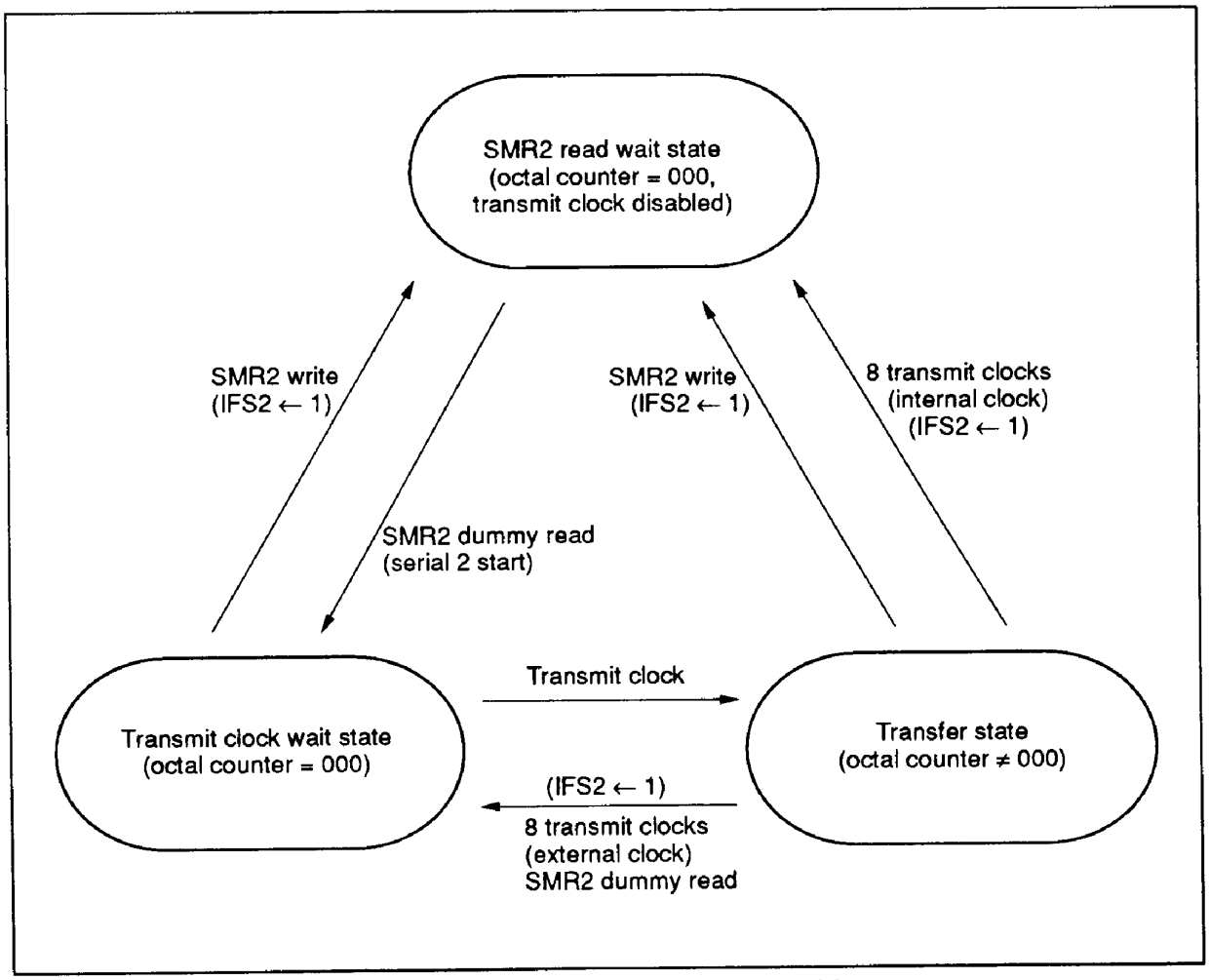


Figure 48 Serial Interface 2 Mode Transitions

Transmit Clock Error Detection: Serial interface 2 will malfunction if a spurious pulse caused by external noise conflicts with a normal transmit clock. Such errors can be detected as shown in figure 49.

If more than eight transmit clocks are input in transmit clock wait state, serial interface 2's state changes to transfer state, transmit clock wait state, then back to transfer state.

When serial interface 2 is set to SMR2 read wait state by writing data to SMR2 at transfer state after the serial interface 2 interrupt request flag (IFS2) has been reset, the flag is set again.

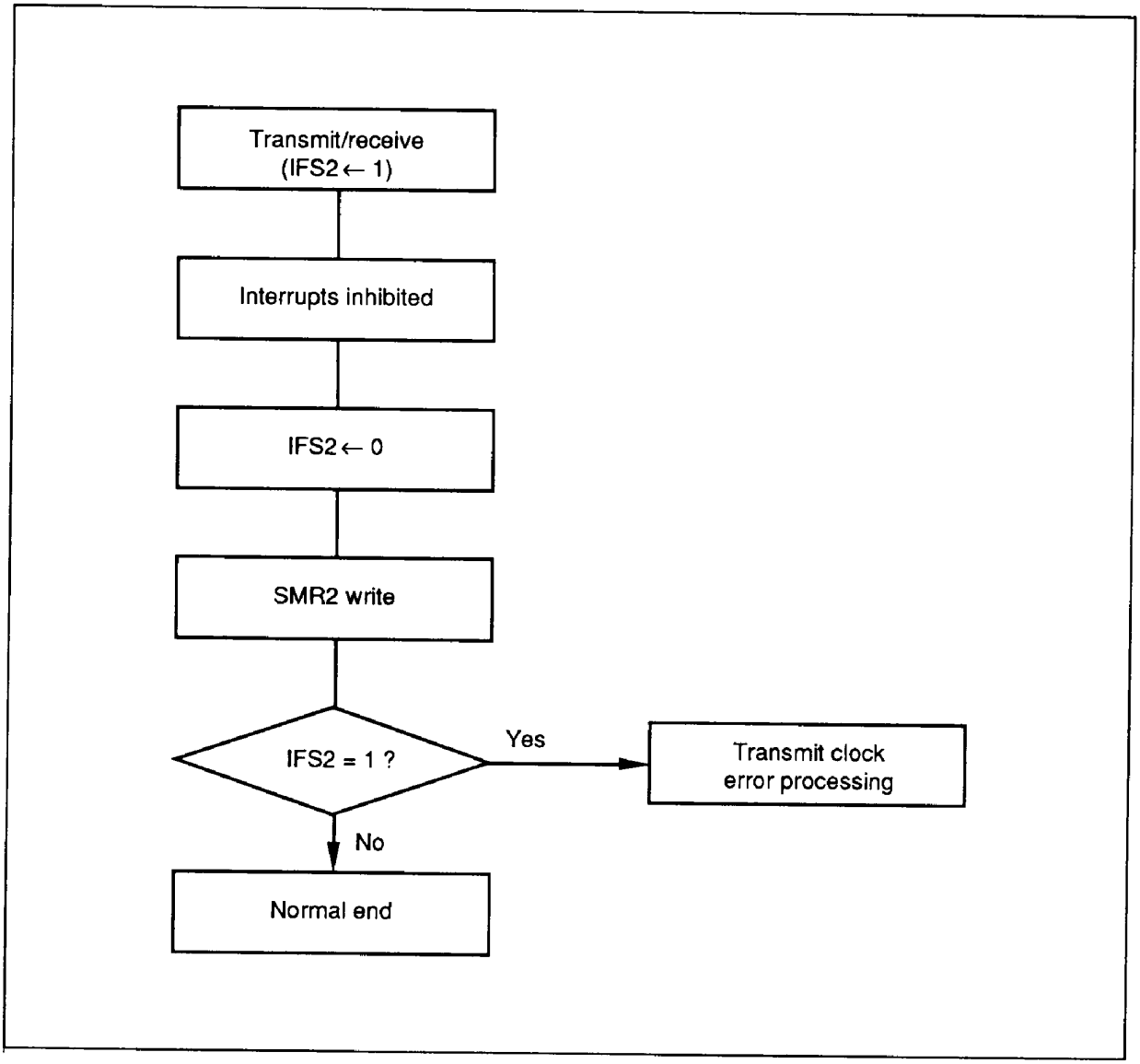


Figure 49 Transmit Clock Error Detection

A/D Converter

The MCU has an 8-bit A/D converter of serial comparison type. It has eight input channels. The block diagram is shown in figure 50.

A/D Control Register (ADCR: $01B): Selects the analog input pin or digital input port and selects one of eight analog input channels. The eight input pins (RC_0/AN_0–RC_3/AN_3, RD_0/AN_4–RD_3/AN_7) must not include analog input mode pins and port input mode pins at the same time; all the pins must be set to the same mode. When selecting analog input mode for these pins, select without pull-up MOS option for the pins.

A/D Status Register (ADSR: $01F): A/D conversion is started by setting 1 to the A/D start flag. At conversion completion, the converted data is set to the A/D data register and the A/D start flag is reset.

A/D Mode Register (AMR: $01C): Two-bit write-only register which selects the A/D conversion speed.

A/D Data Register (ADRL: $01D, ADRU: $01E): Eight-bit read-only register separated into lower and upper digits. Eight-bit A/D converted data is set to the register at conversion completion, and is held until the next conversion starts. Data read during conversion is invalid. The register cannot be cleared by MCU reset.

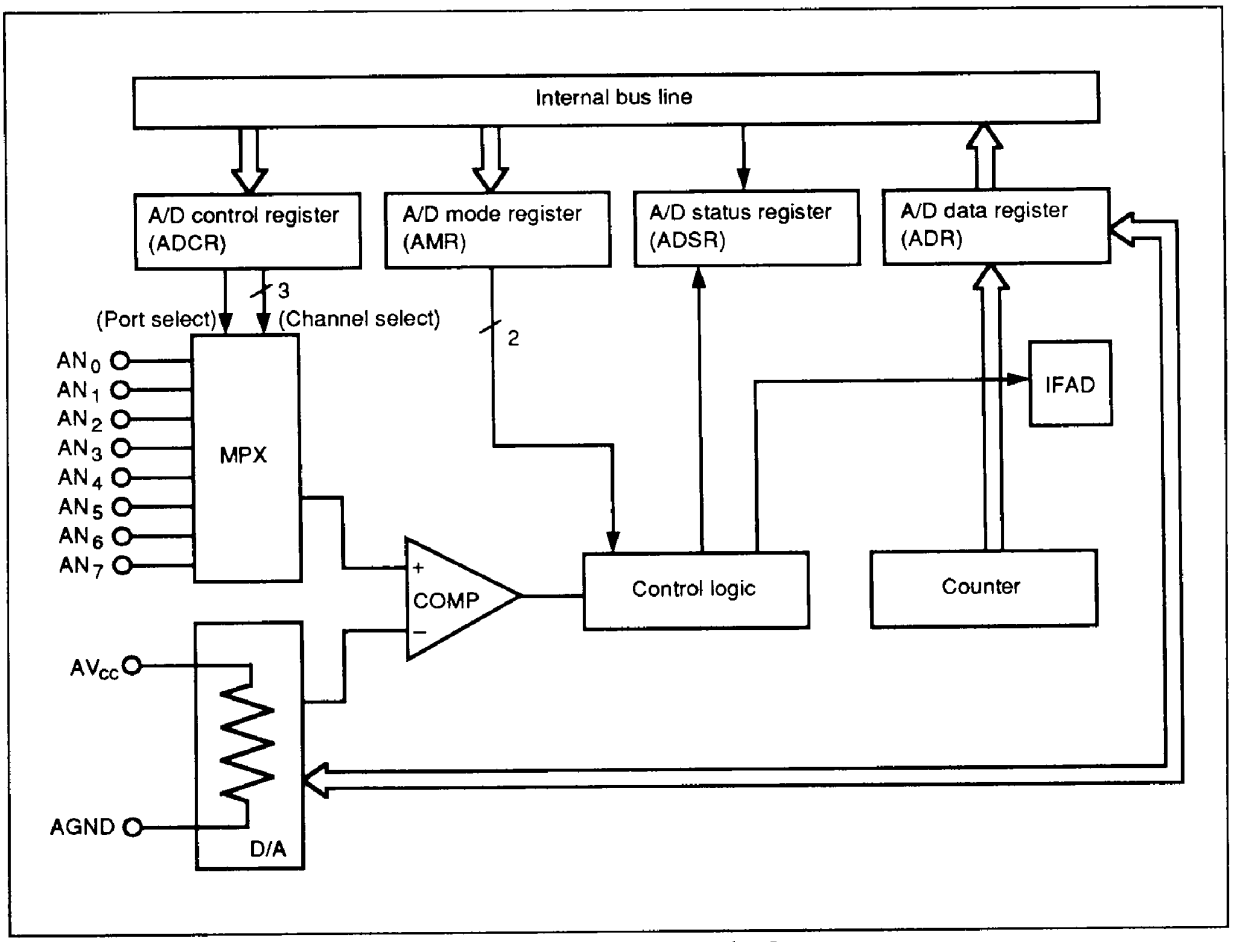


Figure 50 Block Diagram of A/D Converter

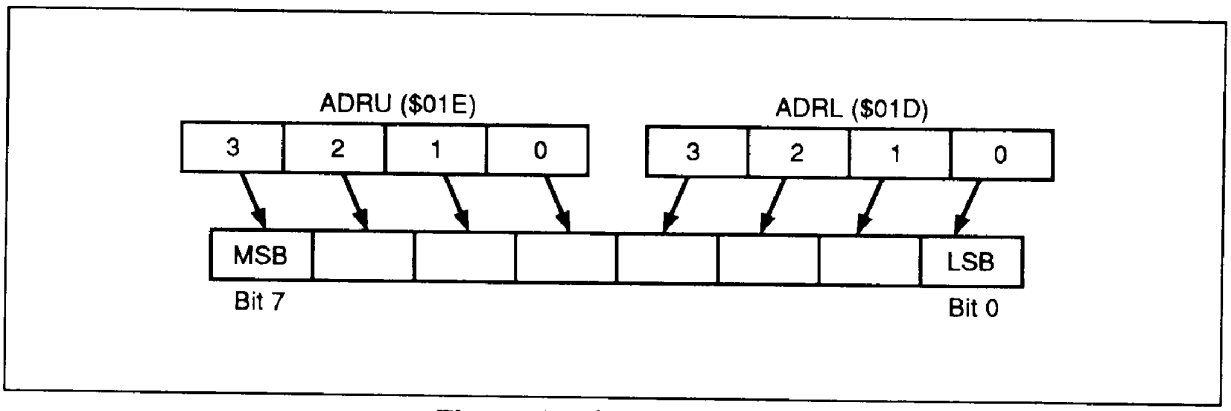
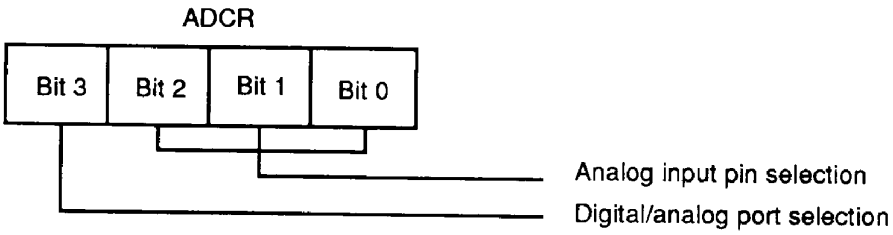


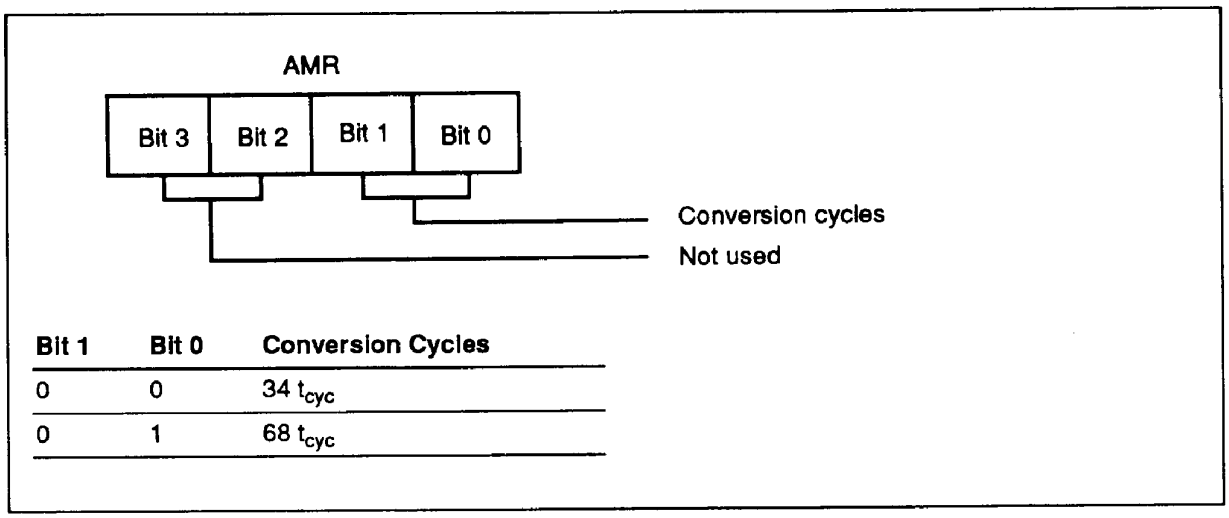
Figure 51 A/D Data Register



Bit 2	Bit 1	Bit 0	Analog Input Pin Selection
0	0	0	AN_0
0	0	1	AN_1
0	1	0	AN_2
0	1	1	AN_3
1	0	0	AN_4
1	0	1	AN_5
1	1	0	AN_6
1	1	1	AN_7

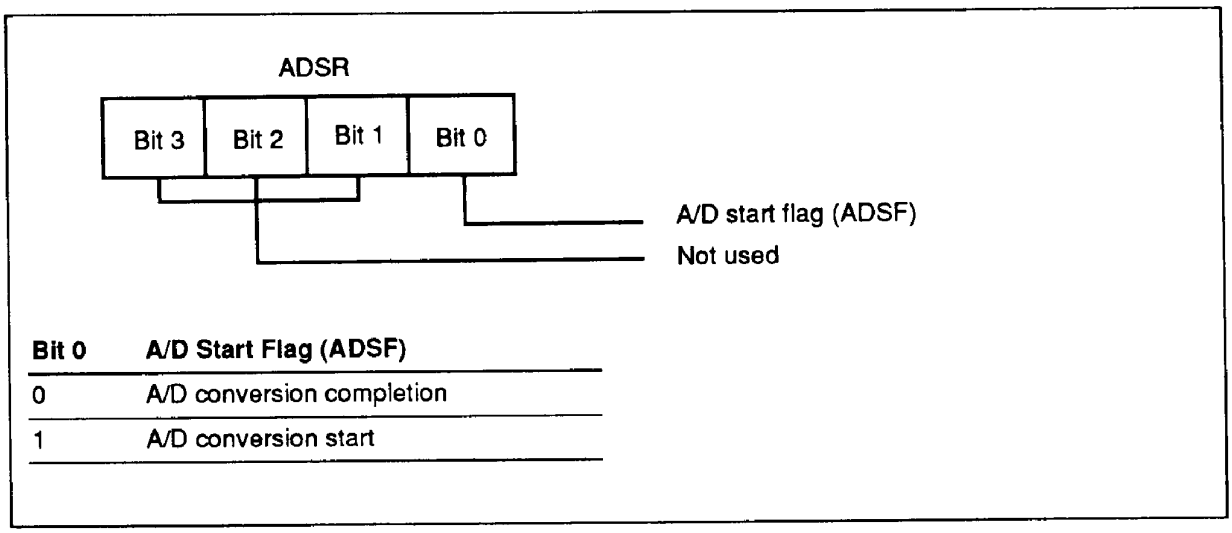
Bit 3	Digital/Analog Selection
0	Digital input pins (RC_0–RC_3, RD_0–RD_3)
1	Analog input pins (AN_0–AN_7)

Figure 52 A/D Control Register



Bit 1	Bit 0	Conversion Cycles
0	0	34 t_{cyc}
0	1	68 t_{cyc}

Figure 53 A/D Mode Register



Bit 0	A/D Start Flag (ADSF)
0	A/D conversion completion
1	A/D conversion start

Figure 54 A/D Status Register

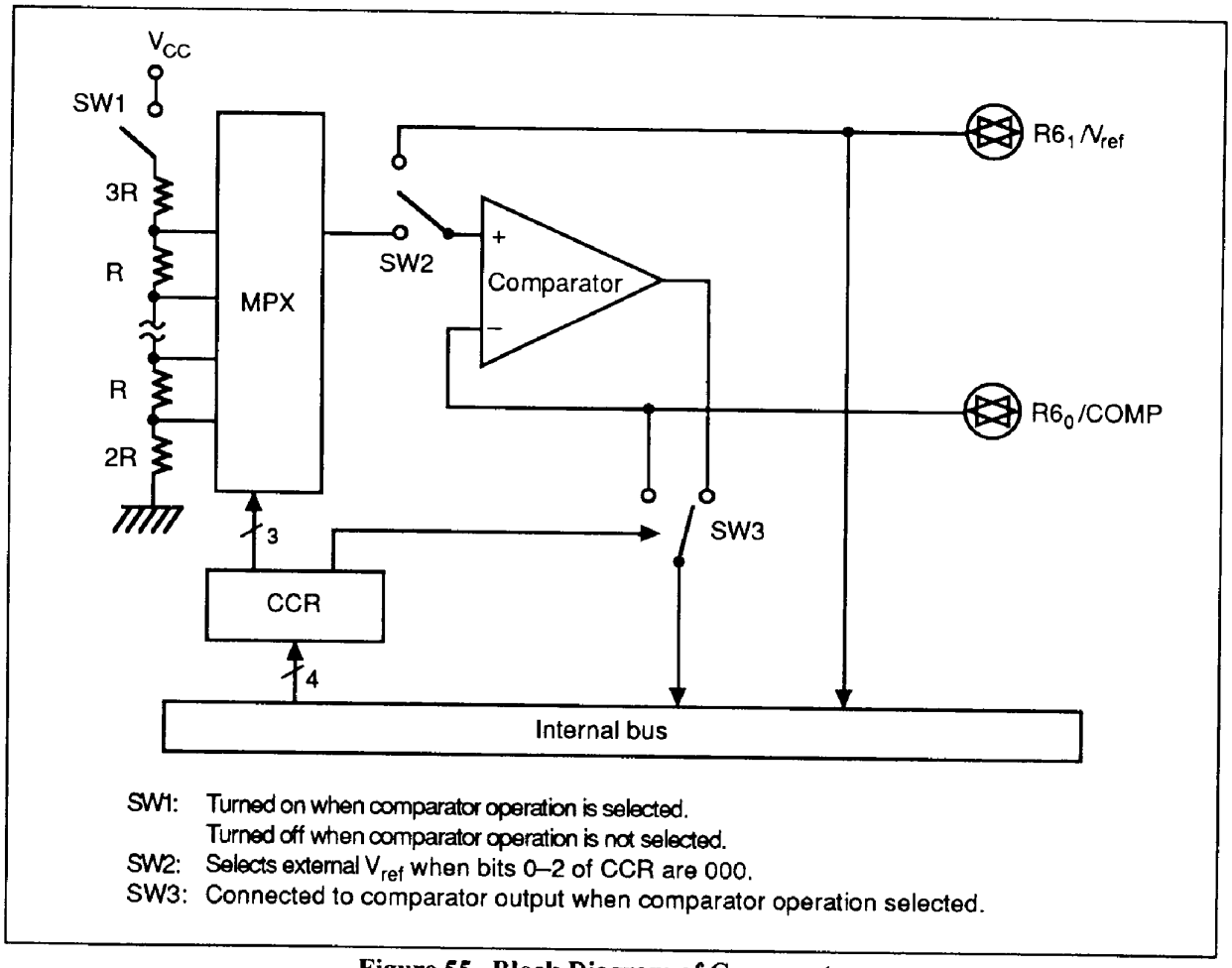
Comparator

The block diagram of the comparator is shown in figure 55. The comparator compares input voltage with the reference voltage. Internal voltage or external input voltage can be selected as the reference. Internal reference voltage is selected from seven levels. When bits 0, 1, and 2 of the compare control register are 0, external reference voltage is input.

The LAR instruction executes a voltage comparison. When the COMP input voltage is higher than the reference voltage, data 0 is read from port $R6_0$.

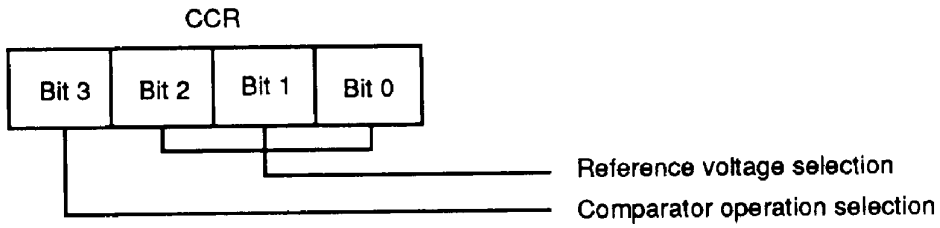
The power supply for the comparator is the digital V_{CC} and GND. When using the comparator, select with pull-up MOS option for pins $R6_0$ and $R6_1$.

Compare Control Register (CCR: $03E): Four-bit write-only register which enables comparator operation and selects internal reference voltage sources.



SW1: Turned on when comparator operation is selected.
Turned off when comparator operation is not selected.
SW2: Selects external V_{ref} when bits 0–2 of CCR are 000.
SW3: Connected to comparator output when comparator operation selected.

Figure 55 Block Diagram of Comparator



Bit 2	Bit 1	Bit 0	Reference Voltage Selection
0	0	0	External V_{ref}
0	0	1	2/11 V_{CC}
0	1	0	3/11 V_{CC}
0	1	1	4/11 V_{CC}
1	0	0	5/11 V_{CC}
1	0	1	6/11 V_{CC}
1	1	0	7/11 V_{CC}
1	1	1	8/11 V_{CC}

Bit 3	Comparator Operation Selection
1	Analog compare mode: comparator operation selected (comparator output is read by the read instruction)
0	Digital input mode: comparator operation not selected ($R6_0$ port is read by the read instruction)

Figure 56 Compare Control Register

Programmable ROM (HD4074719)

The HD4074719 is a ZTAT™ microcomputer with built-in PROM that can be programmed in PROM mode.

PROM Mode Pin Description

Pin Number		MCU Mode		PROM Mode		Pin Number		MCU Mode		PROM Mode	
FP-80B	FP-80A	Pin Name	I/O	Pin Name	I/O	FP-80B	FP-80A	Pin Name	I/O	Pin Name	I/O
1	79	RD_1/AN_5	I			31	29	$R0_2$	I/O	A_3	I
2	80	RD_2/AN_6	I			32	30	$R0_3$	I/O	A_4	I
3	1	RD_3/AN_7	I			33	31	$R1_0$	I/O	A_5	I
4	2	AGND		GND		34	32	$R1_1$	I/O	A_6	I
5	3	RESET	I	RESET	I	35	33	$R1_2$	I/O	A_7	I
6	4	OSC_1	I	GND		36	34	$R1_3$	I/O	A_8	I
7	5	OSC_2	O			37	35	$R2_0$	I/O	A_0	I
8	6	GND		GND		38	36	$R2_1$	I/O	A_{10}	I
9	7	CL_1	I	GND		39	37	$R2_2$	I/O	A_{11}	I
10	8	CL_2	O			40	38	$R2_3$	I/O	A_{12}	I
11	9	TEST	I	TEST	I	41	39	$R3_0$	I/O	A_{13}	I
12	10	V_{CC}		V_{CC}		42	40	$R3_1$	I/O	A_{14}	I
13	11	D_0	I/O			43	41	$R3_2$	I/O		
14	12	D_1	I/O			44	42	$R3_3$	I/O		
15	13	D_2	I/O			45	43	$R4_0$	I/O		
16	14	D_3	I/O			46	44	$R4_1$	I/O		
17	15	D_4	I/O			47	45	$R4_2$	I/O		
18	16	D_5	I/O			48	46	$R4_3$	I/O		
19	17	D_6	I/O			49	47	$R5_0$	I		
20	18	D_7	I/O			50	48	$R5_1$	I	V_{CC}	
21	19	D_8	I/O			51	49	$R5_2$	I	V_{PP}	
22	20	D_9	I/O			52	50	$R5_3$	I	A_9	I
23	21	D_{10}	I/O			53	51	$R6_0$/COMP	I/O	$\overline{CE}$	I
24	22	D_{11}	I/O			54	52	$R6_1/V_{ref}$	I/O	$\overline{OE}$	I
25	23	D_{12}	I/O			55	53	$R6_2/TOE_1$	I/O	V_{CC}	
26	24	D_{13}	I/O			56	54	$R6_3/TOE_2$	I/O	V_{CC}	
27	25	D_{14}	I/O			57	55	$R7_0/\overline{INT}_0$	I/O	O_0	I/O
28	26	D_{15}	I/O			58	56	$R7_1/\overline{INT}_1$	I/O	O_1	I/O
29	27	$R0_0$	I/O	A_1	I	59	57	$R7_2/\overline{INT}_2$	I/O	O_2	I/O
30	28	$R0_1$	I/O	A_2	I	60	58	$R7_3/\overline{INT}_3$	I/O	O_3	I/O

Notes: 1. I/O: Input/output pin, I: Input pin, O: Output pin

2. O_0–O_4 each have 2 pins; connect each pair together for use.

Pin Number		MCU Mode		PROM Mode		Pin Number		MCU Mode		PROM Mode	
FP-80B	FP-80A	Pin Name	I/O	Pin Name	I/O	FP-80B	FP-80A	Pin Name	I/O	Pin Name	I/O
61	59	$R8_0/\overline{INT_4}$	I/O	O_4	I/O	71	69	RA_2/TOG	I/O	O_7	I/O
62	60	$R8_1/\overline{INT_5}$	I/O	O_4	I/O	72	70	RA_3/BUZZ	I/O		
63	61	$R8_2/SO_1$	I/O	O_3	I/O	73	71	RB_0/TOC	I/O	$\overline{M_0}$	I
64	62	$R8_3/SI_1$	I/O	O_2	I/O	74	72	RB_1/TOD	I/O	$\overline{M_1}$	I
65	63	$R9_0/\overline{SCK_1}$	I/O	O_1	I/O	75	73	AV_{CC}		V_{CC}	
66	64	$R9_1/\overline{SCK_2}$	I/O	O_0	I/O	76	74	RC_0/AN_0	I		
67	65	$R9_2/SI_2$	I/O			77	75	RC_1/AN_1	I		
68	66	$R9_3/SO_2$	I/O			78	76	RC_2/AN_2	I		
69	67	RA_0/ICT_0	I/O	O_5	I/O	79	77	RC_3/AN_3	I		
70	68	RA_1/ICT_1	I/O	O_6	I/O	80	78	RD_0/AN_4	I		

Notes: 1. I/O: Input/output pin, I: Input pin, O: Output pin

2. O_0–O_4 each have 2 pins; connect each pair together for use.

PROM Mode Pin Functions

V_{PP}: Applies the programming voltage (12.5 V ± 0.3 V) to the built-in PROM.

$\overline{CE}$: Inputs a control signal to enable PROM programming and verification.

$\overline{OE}$: Inputs a data output control signal for verification.

A_0–A_{14}: Address input pins of the built-in PROM.

O_0–O_7: Data bus input pins of the built-in PROM.

$\overline{M}_0$, $\overline{M}_1$: Used to set PROM mode. The MCU is set to the PROM mode by pulling $\overline{M}_0$, $\overline{M}_1$, and $\overline{TEST}$ low, and RESET high.

The pin arrangement in PROM mode is shown in figure 57.

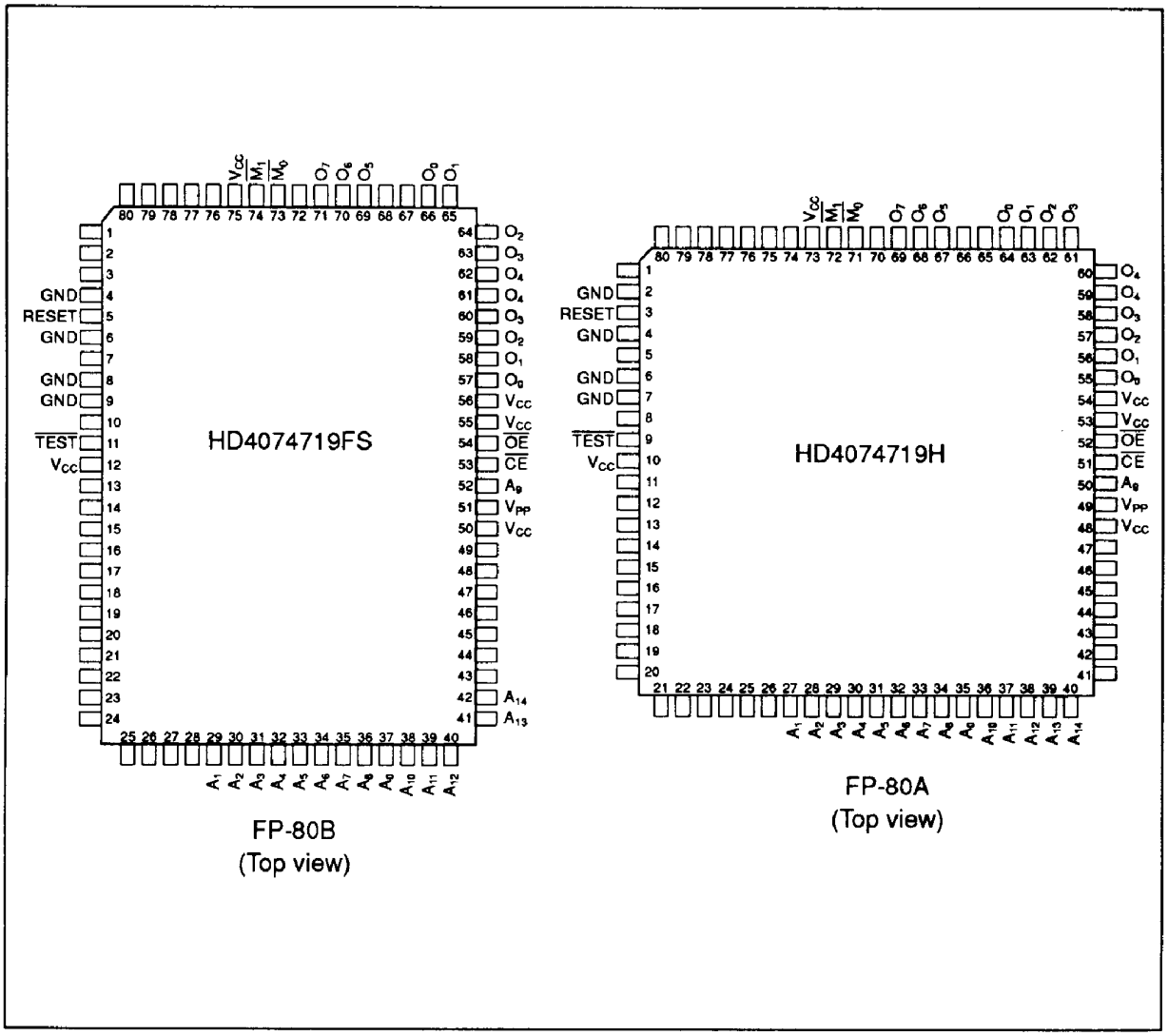


Figure 57 Pin Arrangement in PROM Mode

Programming the Built-In PROM

The MCU's built-in PROM is programmed in PROM mode which is set by pulling $\overline{TEST}$, $\overline{M_0}$, and $\overline{M_1}$ low, and RESET high as shown in figure 58. In PROM mode, the MCU stops, and the PROM is programmed in the same way as a 27256 EPROM using a standard PROM programmer and an 80-to-28-pin socket adapter. Recommended PROM programmers and socket adapters are listed in table 33.

Since an HMCS400-series instruction is ten bits long, the MCU has a built-in conversion circuit for a general-purpose PROM programmer. This circuit splits each instruction into lower 5 bits and upper 5 bits that are read from or written to two consecutive addresses, as shown in figure 59. This means that if, for example, 16 Kwords of built-in PROM are to be programmed by a general-purpose PROM programmer, a 32-Kbyte address space ($0000–$7FFF) must be specified.

Programming and Verification: The built-in PROM of the MCU can be programmed at high-speed programming sequence without voltage stress or damage to data reliability.

Programming and verification modes are selected as shown in table 32, the memory map in PROM mode is shown in figure 59, the programming flowchart is shown in figure 60, and a timing chart of PROM programming and verification is shown in figure 61.

For details of PROM programming, refer to the Notes on PROM Programming section.

Warnings

1. Always specify addresses $0000 to $7FFF when programming with a PROM programmer. If address $8000 or higher is accessed, the PROM may not be programmed or verified correctly. Set all data in unused addresses to $FF.

   Note that the plastic-package version cannot be erased and reprogrammed.

2. Make sure that the PROM programmer, socket adapter, and LSI are inserted correctly (in the correct direction), otherwise overcurrents may damage the LSI. Before starting programming, make sure that the LSI is firmly fixed in the socket adapter and the socket adapter is firmly fixed onto the programmer.

3. PROM programmers have two voltage settings (V_{PP}): 12.5 V and 21 V. Remember that ZTAT™ devices require a V_{PP} of 12.5 V—the 21 V setting will damage them. 12.5 V is the Intel's 27256 setting.

Table 32 PROM Mode Selection

	Pin			
Mode	$\overline{CE}$	$\overline{OE}$	V_{PP}	O_0–O_7
Programming	Low	High	V_{PP}	Data input
Verification	High	Low	V_{PP}	Data output
Programming inhibited	High	High	V_{PP}	High impedance

Table 33 Recommended PROM Programmers and Socket Adapters

PROM Programmer		Socket Adapter		
Manufacturer	**Model Name**	**Package**	**Manufacturer**	**Model Name**
DATA I/O Corp.	29B Unisite	FP-80A	Hitachi	HS471ESH01H
		FP-80B	Hitachi	HS471ESF01H
AVAL Data Corp.	PKW-1000	FP-80A	Hitachi	HS471ESH01H
	PKW-3100	FP-80B	Hitachi	HS471ESF01H

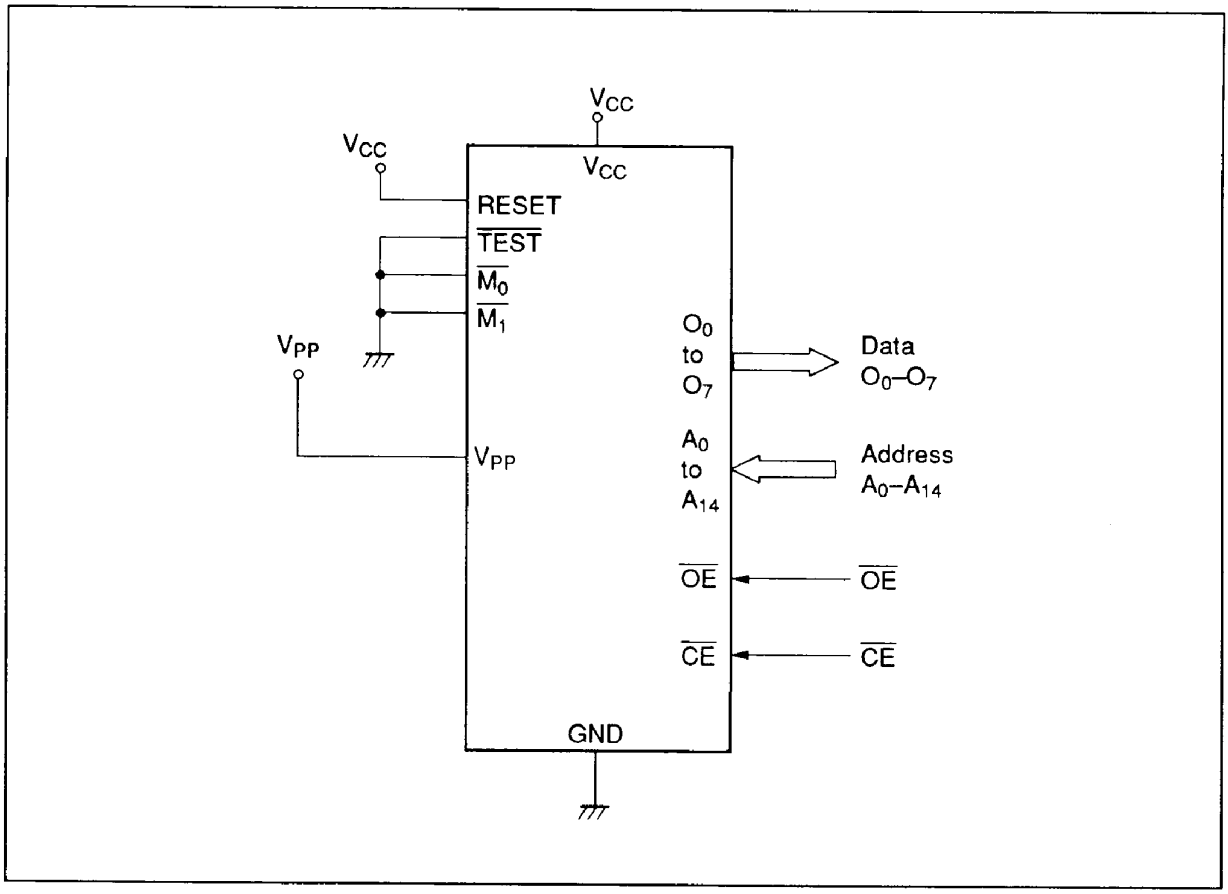


Figure 58 Connections for PROM Mode

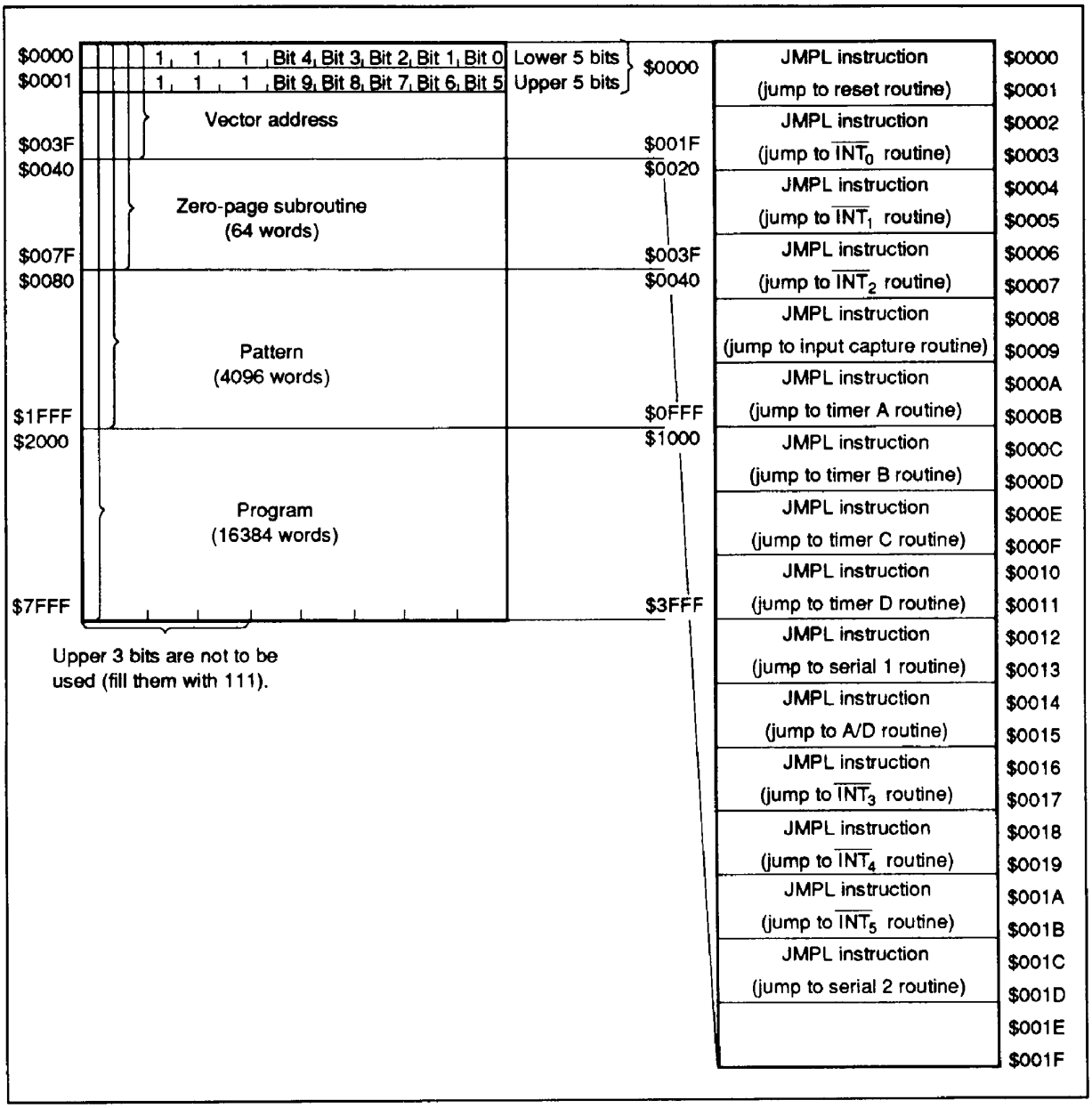


Figure 59 Memory Map in PROM Mode

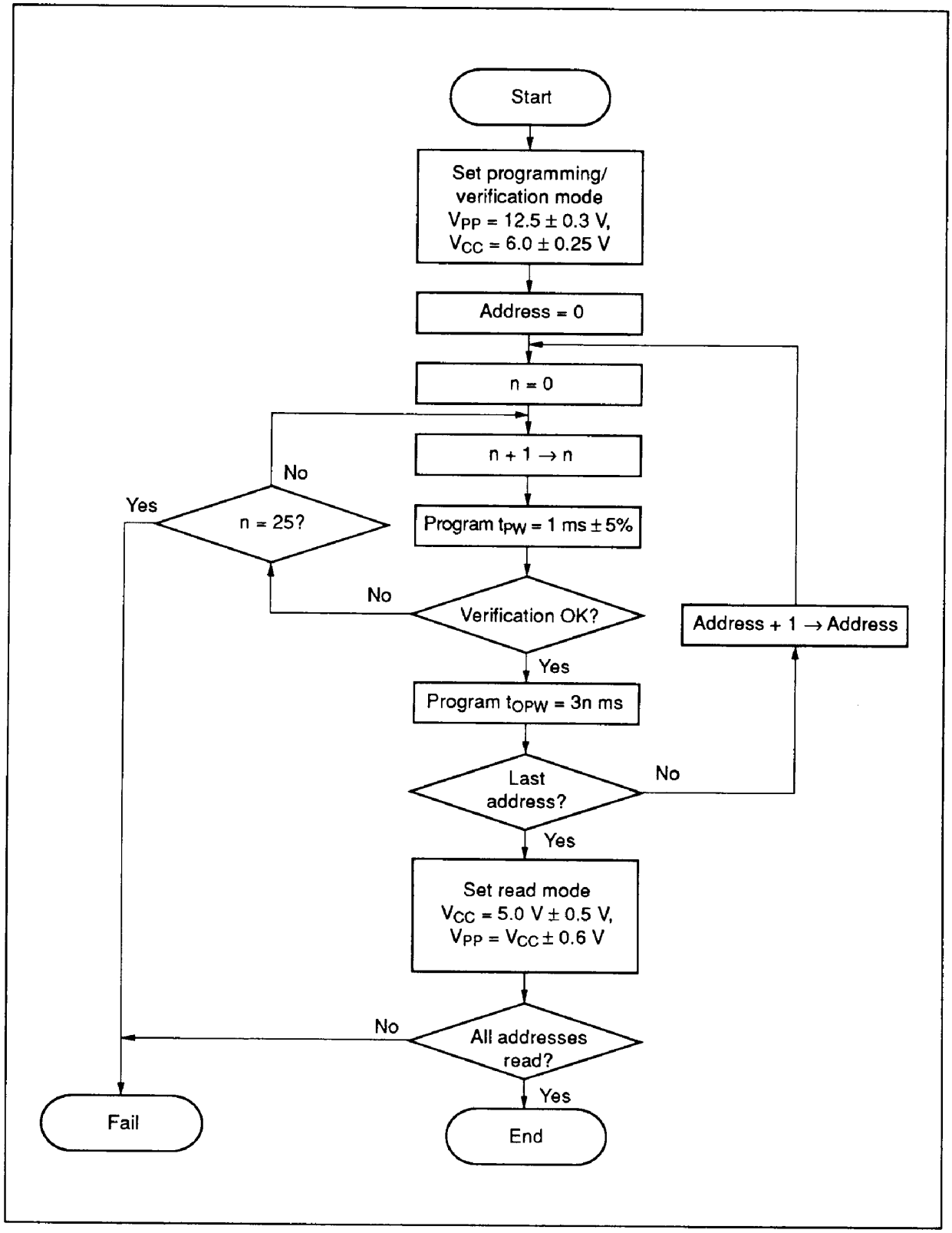


Figure 60 High-Speed Programming Flowchart

Programming and Verification Electrical Characteristics

DC Characteristics (V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, GND = 0.0 V, T_a = 25°C ± 5°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition
Input high voltage	V_{IH}	O_0–O_7, A_0–A_{14}, $\overline{OE}$, $\overline{CE}$	2.2	—	V_{CC} + 0.3	V	
Input low voltage	V_{IL}	O_0–O_7, A_0–A_{14}, $\overline{OE}$, $\overline{CE}$	–0.3	—	0.8	V	
Output high voltage	V_{OH}	O_0–O_7	2.4	—	—	V	I_{OH} = –200 µA
Output low voltage	V_{OL}	O_0–O_7	—	—	0.4	V	I_{OL} = 1.6 mA
Input leakage current	$\|I_{IL}\|$	O_0–O_7, A_0–A_{14}, $\overline{OE}$, $\overline{CE}$	—	—	2	µA	V_{in} = 5.25 V/ 0.5 V
V_{CC} current	I_{CC}		—	—	30	mA	
V_{PP} current	I_{PP}		—	—	40	mA	

AC Characteristics (V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, GND = 0.0 V, T_a = 25°C ± 5°C, unless otherwise specified)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Address setup time	t_{AS}	2	—	—	µs	Refer to figure 61
$\overline{OE}$ setup time	t_{OES}	2	—	—	µs	
Data setup time	t_{DS}	2	—	—	µs	
Address hold time	t_{AH}	0	—	—	µs	
Data hold time	t_{DH}	2	—	—	µs	
Output disable delay time	t_{DF}[Note]	—	—	130	ns	
V_{PP} setup time	t_{VPS}	2	—	—	µs	
Program pulse width	t_{PW}	0.95	1.0	1.05	ms	
$\overline{CE}$ pulse width during overprogramming	t_{OPW}	2.85	—	78.75	ms	
V_{CC} setup time	t_{VCS}	2	—	—	µs	
Data output delay time	t_{OE}	0	—	500	ns	

Note: t_{DF} is defined at the point where the output level can no longer be referenced after output goes to high-impedance state.

Switching characteristics
Input pulse level: 0.8 V to 2.2 V
Input rise/fall time: ≤ 20 ns
Input timing reference levels: 1.0 V, 2.0 V
Output timing reference levels: 0.8 V, 2.0V

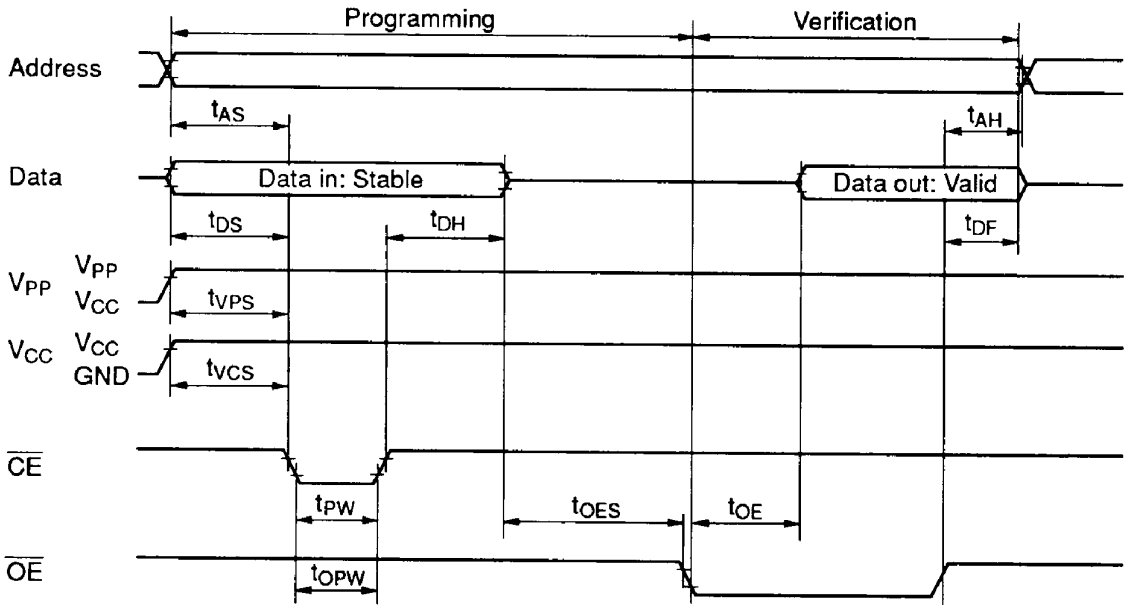


Figure 61 PROM Programming/Verification Timing

Notes on PROM Programming

Principles of Programming/Erasure: A memory cell in a ZTAT™ microcomputer is the same as an EPROM cell: it is programmed by applying a high voltage between its control gate and drain to inject hot electrons into its floating gate. These electrons are stable, surrounded by an energy barrier formed by an SiO_2 film. The change in threshold voltage of a memory cell with a charged floating gate makes the corresponding bit appear as 0; a cell whose floating gate is not charged appears as 1 (figure 62).

The charge in a memory cell may decrease with time. This decrease is usually due to the following causes:

- Ultraviolet light excites electrons, allowing them to escape. This effect is the basis of the erasure principle.
- Heat excites trapped electrons, allowing them to escape.
- High voltages between control gate and drain may erase electrons.

If the oxide film covering a floating gate is defective, the electron erasure rate will be greater. However, electron erasure does not often occur because defective devices are detected and removed during screening tests.

PROM Programming: PROM memory cells must be programmed under specific voltage and timing conditions. The higher the programming voltage V_{PP} and the longer the programming pulse t_{pw} is applied, the more electrons are injected into the floating gates. However, if V_{PP} exceeds specifications, the pn junctions may be permanently damaged. Pay particular attention to overshooting in the PROM programmer. In addition, note that negative voltage noise will produce a parasitic transistor effect that may reduce breakdown voltages.

The ZTAT™ microcomputer is electrically connected to the PROM programmer by a socket adapter. Therefore, note the following points:

- Check that the socket adapter is firmly mounted on the PROM programmer.
- Do not touch the socket adapter or the LSI during the programming. Touching them may affect the quality of the contacts, which will cause programming errors.

PROM Reliability after Programming: In general, semiconductor devices retain their reliability, provided that some initial defects can be excluded. These initial defects can be detected and rejected by screening. Baking devices under high-temperature conditions is one method of screening that can rapidly eliminate data-hold defects in memory cells. (Refer to the Principles of Programming/ Erasure section.)

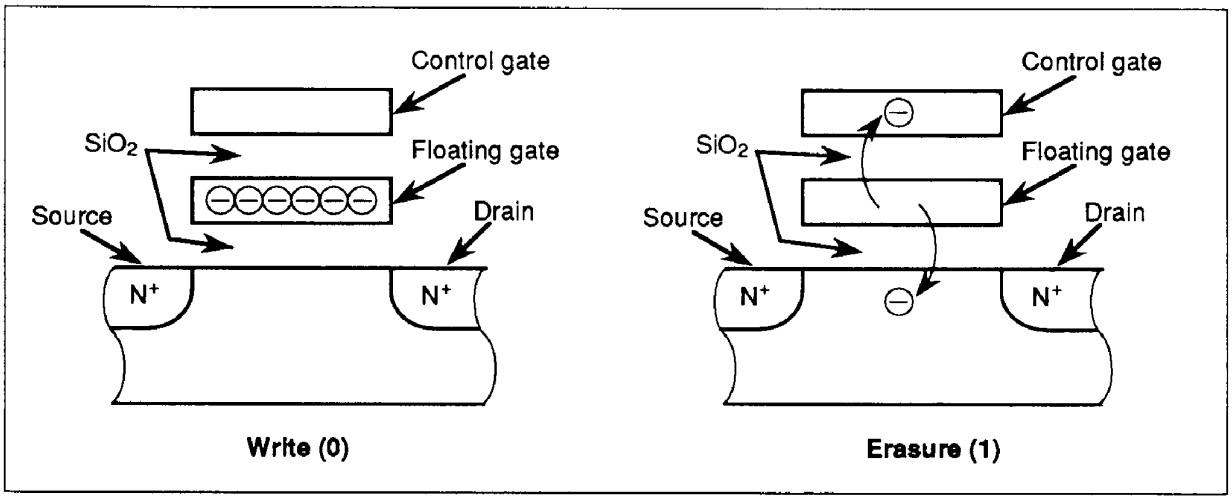


Figure 62 Cross-Sections of a EPROM Cell

ZTAT™ microcomputer devices are highly reliable because they have been subjected to such a screening method during the wafer fabrication process, but it is recommended that each device be exposed to 150°C at one atmosphere for at least 48 hours after it is programmed, to ensure its best performance. The recommended screening process is shown in figure 63.

Note: If programming errors occur continuously during PROM programming, suspend programming and check for problems in the PROM programmer or socket adapter. If programming verification indicates errors in programming or after high-temperature exposure, please inform Hitachi.

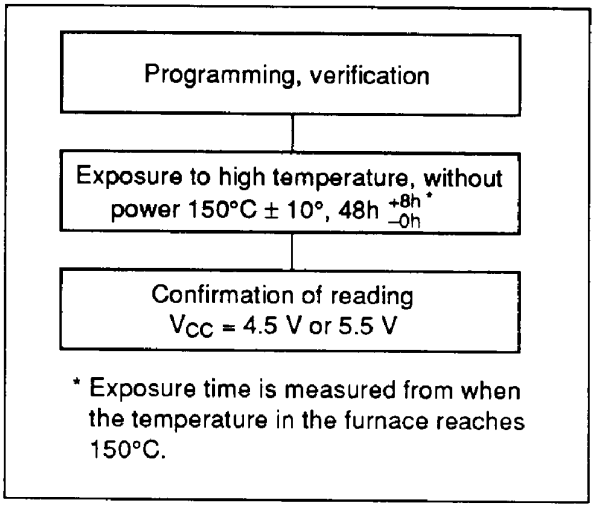


Figure 63 Recommended Screening Procedure

Addressing Modes

RAM Addressing Modes

The MCU has three RAM addressing modes, as shown in figure 64 and described below.

Register Indirect Addressing Mode: The contents of the W, X, and Y registers (10 bits in total) are used as a RAM address.

Direct Addressing Mode: A direct addressing instruction consists of two words. The first word contains the opcode, and the contents of the second word (10 bits) are used as a RAM address.

Memory Register Addressing Mode: The memory registers (MR), located in 16 digits from $040 to $04F, are accessed with the LAMR and XMRA instructions.

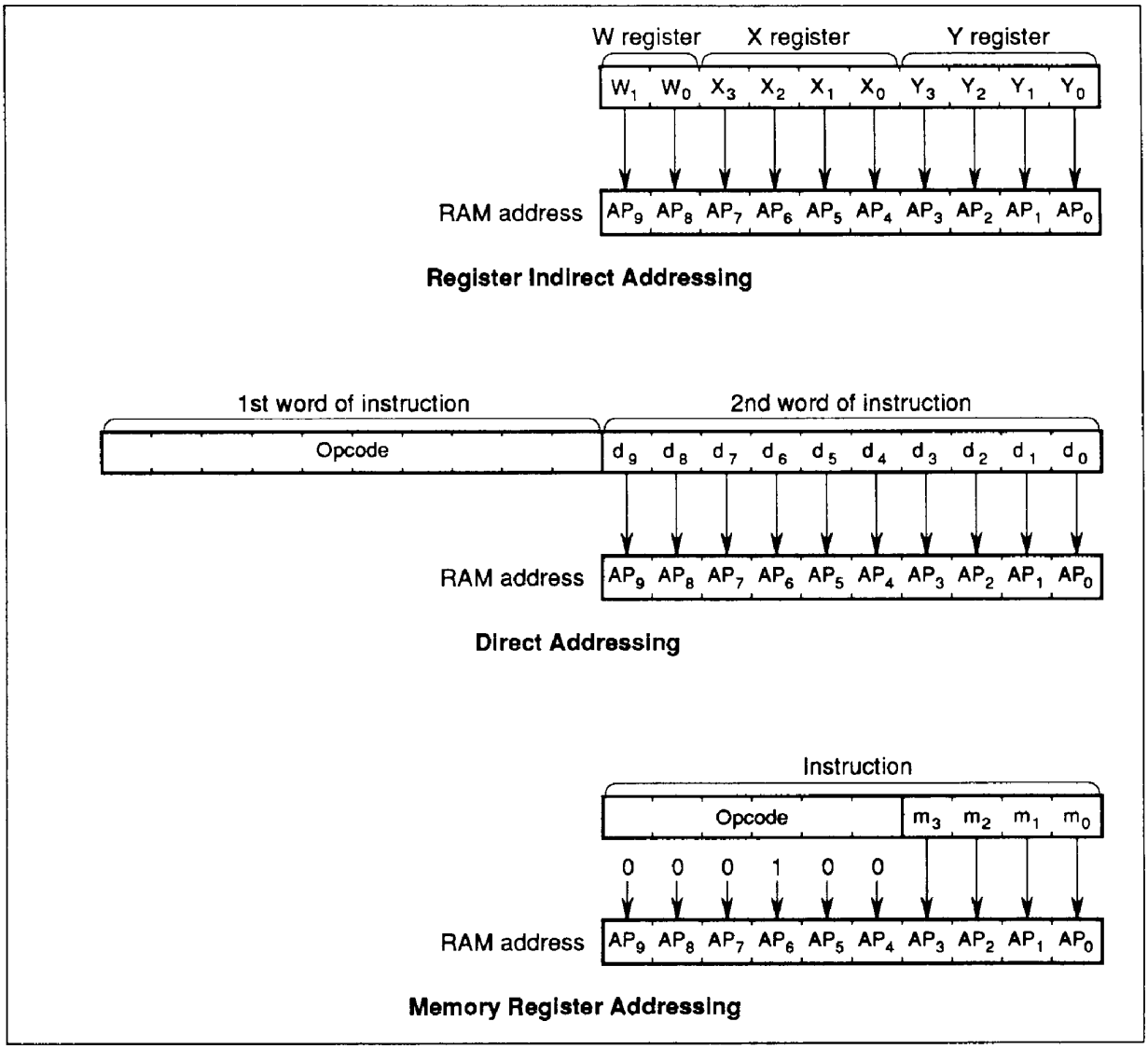


Figure 64 RAM Addressing Modes

ROM Addressing Modes and the P Instruction

The MCU has four ROM addressing modes, as shown in figure 65, and the P instruction shown in figure 66.

Direct Addressing Mode: A program can branch to any address in the ROM memory space by executing the JMPL, BRL, or CALL instruction. Each of these instructions replaces the 14 program counter bits (PC_{13}–PC_0) with 14-bit immediate data.

Current Page Addressing Mode: The MCU has 64 pages of ROM with 256 words per page. A program can branch to any address in the current page by executing the BR instruction. This instruction replaces the eight low-order bits of the program counter (PC_7–PC_0) with eight-bit immediate data. If the BR instruction is on a page boundary (address 256n + 255), executing that instruction transmits the PC contents to the next physical page, as shown in figure 67. This means that the execution of the BR instruction on a page boundary will make the program branch to the next page.

Note that the HMCS400-series cross macroassembler has an automatic paging feature for ROM pages.

Zero-Page Addressing Mode: A program can branch to the zero-page subroutine area located at $0000–$003F by executing the CAL instruction. When the CAL instruction is executed, 6 bits of immediate data are placed in the six low-order bits of the program counter (PC_5–PC_0), and 0s are placed in the eight high-order bits (PC_{13}–PC_6).

Table Data Addressing Mode: A program can branch to an address determined by the contents of four-bit immediate data, the accumulator, and the B register by executing the TBR instruction.

P Instruction: ROM data addressed in table data addressing mode can be referenced by the P instruction as shown in figure 65. If bit 8 of the ROM data is 1, eight bits of ROM data are written to the accumulator and the B register. If bit 9 is 1, eight bits of ROM data are written to the R1 and R2 port output registers. If both bits 8 and 9 are 1, ROM data is written to the accumulator and the B register, and also to the R1 and R2 port output registers at the same time.

The P instruction has no effect on the program counter.

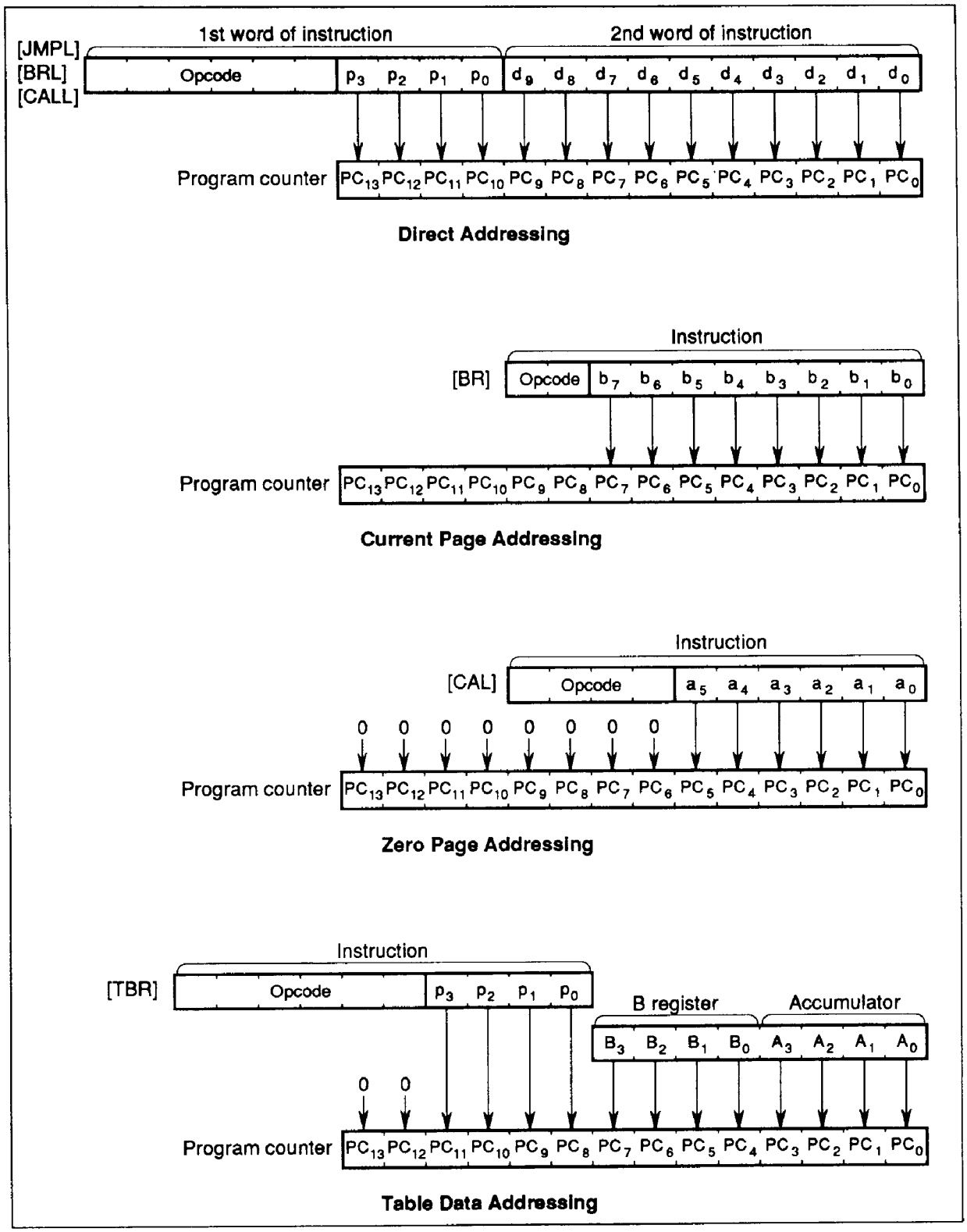


Figure 65 ROM Addressing Modes

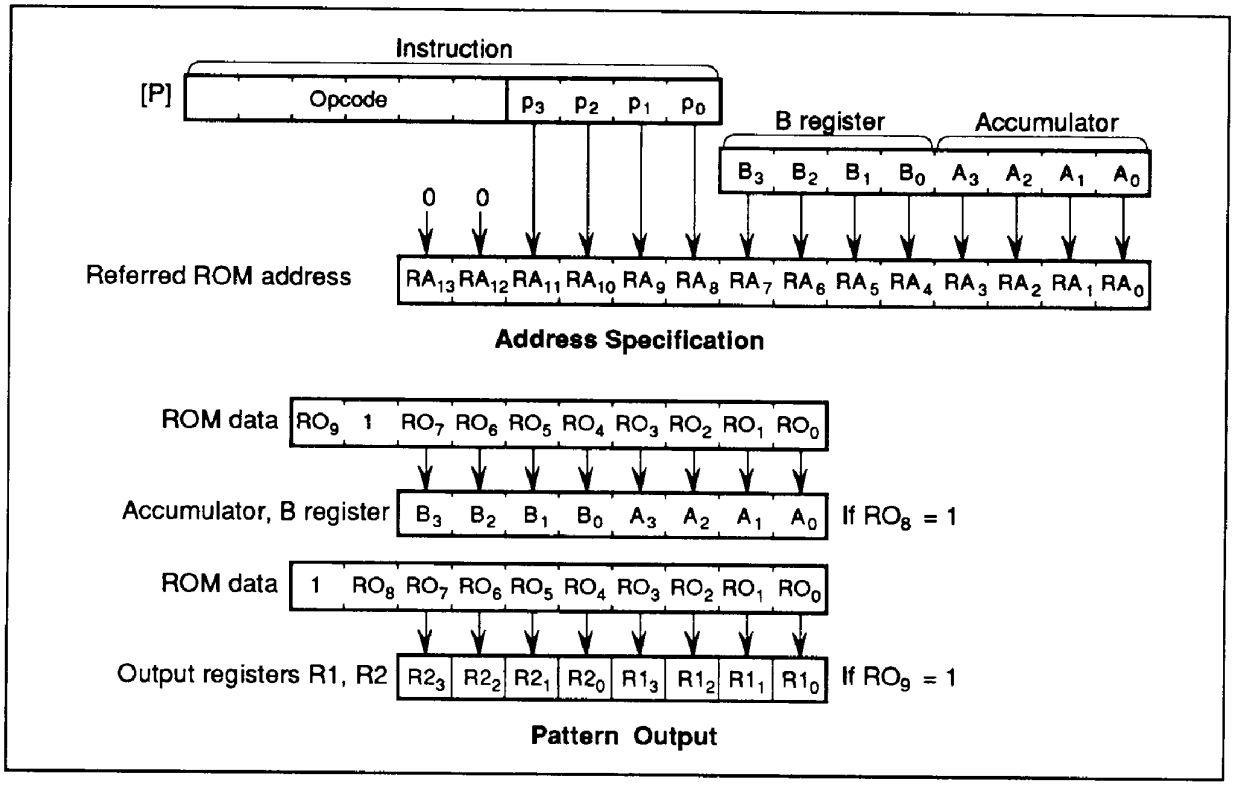


Figure 66 P Instruction

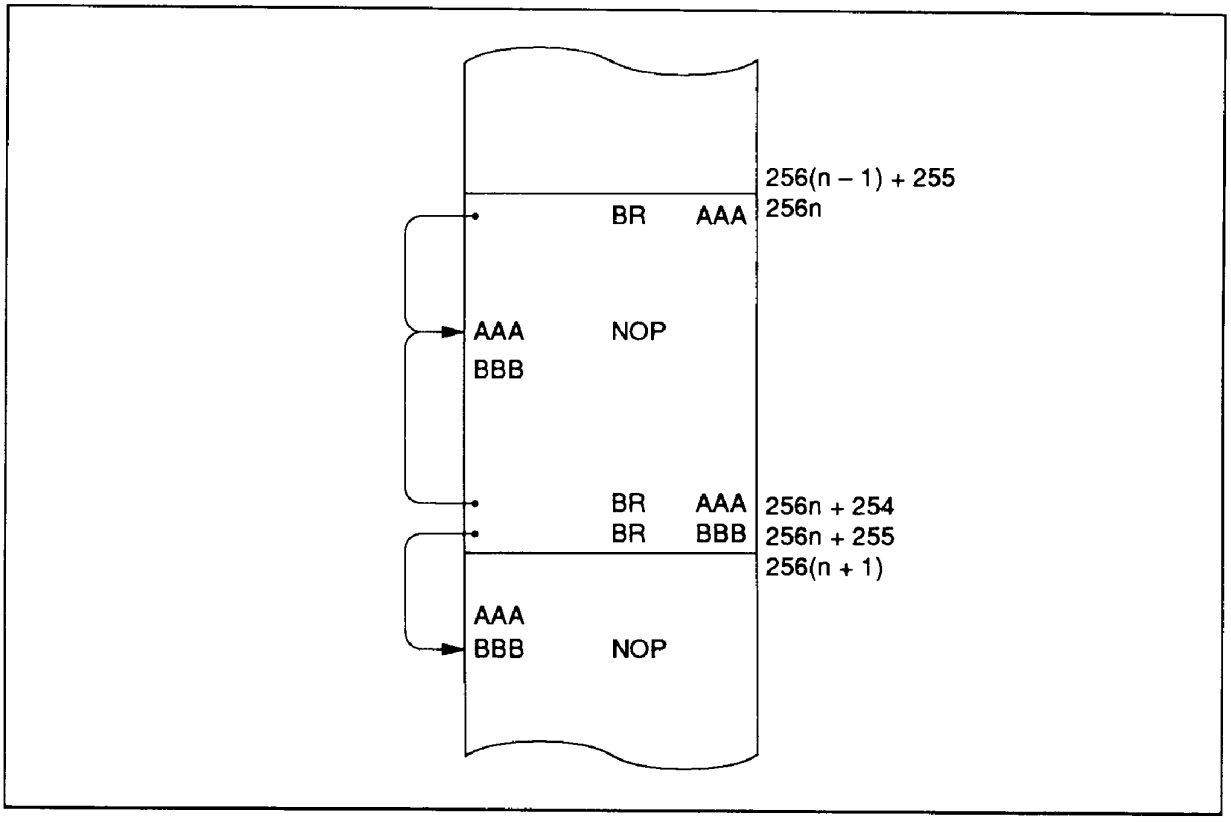


Figure 67 Branching when Branch Destination is on a Page Boundary

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Notes
Supply voltage	V_{CC}	–0.3 to +7.0	V	
Programming voltage	V_{PP}	–0.3 to +14.0	V	12
Pin voltage	V_T	–0.3 to V_{CC} + 0.3	V	3
		V_{CC} – 45 to V_{CC} + 0.3	V	4
Total permissible input current	ΣI_o	50	mA	5
Total permissible output current	$-\Sigma I_o$	150	mA	6
Maximum input current	I_o	15	mA	7, 8
Maximum output current	$-I_o$	4	mA	9, 10
		30	mA	9, 11
Operating temperature	T_{opr}	–20 to +75	°C	
Storage temperature	T_{stg}	–55 to +125	°C	
Storage temperature (bias)	T_{bias}	–25 to +80	°C	12

Notes:
1. Permanent damage may occur if these absolute maximum ratings are exceeded. Normal operation must be under the conditions stated in the electrical characteristics tables. If these conditions are exceeded, the LSI may malfunction or its reliability may be affected.
2. All voltages are with respect to GND.
3. Standard pins.
4. High-voltage pins.
5. The total permissible input current is the total of input currents simultaneously flowing in from all I/O pins to GND.
6. The total permissible output current is the total of output currents simultaneously flowing out from V_{CC} to all I/O pins.
7. The maximum input current is the maximum current flowing from any I/O pin to GND.
8. Applies to R5–RD.
9. The maximum output current is the maximum current flowing from V_{CC} to any I/O pin.
10. Applies to R6–RB.
11. Applies to D0–D15 and R0–R4.
12. Applies to HD4074719.

HD404719 Electrical Characteristics

DC Characteristics (V_{CC} = 3.0 to 6.0 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20° to +75°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	RESET, $\overline{SCK_1}$, $\overline{SCK_2}$, $\overline{INT_0}$–$\overline{INT_5}$	0.85V_{CC}	—	V_{CC} + 0.3	V		
		SI_1, SI_2	0.7V_{CC}	—	V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.5	—	V_{CC} + 0.3	V	V_{CC} = 3.5 to 6.0 V	
			V_{CC} – 0.3	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	RESET, $\overline{SCK_1}$, $\overline{SCK_2}$, $\overline{INT_0}$–$\overline{INT_5}$	–0.3	—	0.2V_{CC}	V		
		SI_1, SI_2	–0.3	—	0.3V_{CC}	V		
		OSC_1	–0.3	—	0.5	V	V_{CC} = 3.5 to 6.0 V	
			–0.3	—	0.3	V		
Output high voltage	V_{OH}	$\overline{SCK_1}$, $\overline{SCK_2}$, SO_1, SO_2, BUZZ, TOC, TOD, TOE_1, TOE_2, TOG	V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 1.0 mA, V_{CC} = 3.5 to 6.0 V	
			V_{CC} – 0.5	—	—	V	$-I_{OH}$ = 0.5 mA, V_{CC} = 3.5 to 6.0 V	
							$-I_{OH}$ = 0.3 mA	
Output low voltage	V_{OL}	$\overline{SCK_1}$, $\overline{SCK_2}$, SO_1, SO_2, BUZZ, TOC, TOD, TOE_1, TOE_2, TOG	—	—	0.4	V	I_{OL} = 1.6 mA, V_{CC} = 3.5 to 6.0 V	
							I_{OL} = 0.4 mA	
I/O leakage current	$\|I_{IL}\|$	RESET, $\overline{SCK_1}$, $\overline{SCK_2}$, SI_1, SI_2, SO_1, SO_2, BUZZ, OSC_1, TOC, TOD, TOE_1, TOE_2, TOG	—	—	1	µA	V_{in} = 0 V to V_{CC}	1

Notes: 1. Excluding output buffer current.

DC Characteristics (V_{CC} = 3.0 to 6.0 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20° to +75°C, unless otherwise specified) (cont)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Current dissipation in active mode	I_{CC}	V_{CC}	—	—	8.0	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz, digital input mode	2, 5
			—	—	4.5	mA	V_{CC} = 3 V, f_{OSC} = 2 MHz, digital input mode	2, 5
	I_{CMP}		—	—	12.0	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz, analog input mode	3, 5
			—	—	7.0	mA	V_{CC} = 3 V, f_{OSC} = 2 MHz, analog input mode	3, 5
Current dissipation in standby mode	I_{SBY}	V_{CC}	—	—	3.0	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	4, 5
			—	—	1.5	mA	V_{CC} = 3 V, f_{OSC} = 2 MHz	4, 5
Current dissipation in subactive mode	I_{SUB}	V_{CC}	—	—	70	µA	$V_{in\ (\overline{TEST})}$ = V_{CC} – 0.3 V to V_{CC} $V_{in\ (RESET)}$ = 0 to 0.3 V, V_{CC} = 3 V, 32.768-kHz crystal oscillator	6, 7
Current dissipation in watch mode	I_{WATCH}	V_{CC}	—	—	15	µA	$V_{in\ (\overline{TEST})}$ = V_{CC} – 0.3 V to V_{CC}, $V_{in\ (RESET)}$ = 0 to 0.3 V, V_{CC} = 3 V, 32.768-kHz crystal oscillator	6, 7, 8
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	—	10	µA	$V_{in\ (\overline{TEST})}$ = V_{CC} – 0.3 V to V_{CC}, $V_{in\ (RESET)}$ = 0 to 0.3 V, no 32.768-kHz oscillator	6
Watch mode retaining voltage	V_{WATCH}	V_{CC}	3.5	—	6.0	V	V_{CC} = 3.5 to 6.0 V	7, 8
			3.0	—	6.0	V		
Stop mode retaining voltage	V_{STOP}	V_{CC}	2	—	—	V	No 32.768-kHz oscillator	

Refer to notes on next page.

DC Characteristics (V_{CC} = 3.0 to 6.0 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20° to +75°C, unless otherwise specified) (cont)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IHA}	$R6_0$/COMP	V_{ref} + 0.1	—	—	V	Analog compare mode	
Input low voltage	V_{ILA}	$R6_0$/COMP	—	—	V_{ref} – 0.1	V	Analog compare mode	
Range of analog input reference voltage	V_{ref}	$R6_1/V_{ref}$	0	—	V_{CC} – 1.2	V		
Allowable error of internal reference voltage	V_{OFS}		–100	—	+100	mV	V_{OFS} = reference voltage – V_{ref}	9

Notes: 2. I_{CC} is the source current when no I/O current is flowing while the MCU is in reset state.
Test conditions: MCU: Reset
Pins: RESET, $\overline{TEST}$ at V_{CC}
$R5_1$–RD at V_{CC}
D_0–D_{15}, R0–R3, R4, $R5_0$ at V_{disp}

3. I_{CMP} is the source current when no I/O current is flowing while the $R6_0$/COMP pin is in analog input mode.
TEST conditions: Pins: $R6_0$/COMP, $R6_1/V_{ref}$ at GND

4. I_{SBY} is the source current when no I/O current is flowing while the MCU timer is in operation.
Test conditions: MCU: I/O same as at reset
Standby mode
Pins: RESET at GND
$\overline{TEST}$ at V_{CC}
$R5_1$–RD at V_{CC}
D_0–D_{15}, R0–R3, R4, $R5_0$ at V_{disp}

5. Power dissipation, while the MCU is operating or in standby mode, is in proportion to f_{OSC}. The value of the dissipation current when f_{OSC} = χ MHz is given by the following equation:
Maximum value (f_{OSC} = χ MHz) = $\chi/4 \times$ maximum value (f_{OSC} = 4 MHz)

6. Source current when no I/O current is flowing.
Test conditions: Pins: $R5_1$–RD at V_{CC}
D_0–D_{15}, R0–R4, $R5_0$ at GND

7. Applies when '32-kHz CPU operation' is selected as an optional function.

8. Applies when 'no 32-kHz CPU operation with clock time base' is selected as an optional function.

9. The reference voltage is the expected internal V_{ref} voltage selected by the compare control register (CCR).
Example: when CCR = $9, reference voltage is $2/11 \times V_{CC}$.

A/D Converter (V_{CC} = 3.0 to 6.0 V, AGND = GND, T_a = –20° to +75°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Analog supply voltage	AV_{CC}	AV_{CC}	V_{CC} – 0.3	V_{CC}	V_{CC} + 0.3	V		
Analog input voltage	AV_{in}	AN_0–AN_7	AGND	—	AV_{CC}	V		1
Current between AV_{CC} and AGND	AI_{CC}	AV_{CC}	—	—	150	µA	AV_{CC} = 5V, $V_{in\ (\overline{RESET})}$ = 0 to 0.3 V, $V_{in\ (\overline{TEST})}$ = V_{CC} – 0.3 V to V_{CC}	
	AI_{STOP}	AV_{CC}	—	—	10	µA	$V_{in\ (\overline{RESET})}$ = 0 to 0.3 V, $V_{in\ (\overline{TEST})}$ = V_{CC} – 0.3 V to V_{CC}, stop mode, no 32.768-kHz oscillator	
Analog input capacitance	C_{ain}	AN_0–AN_7	—	—	30	pF		
Resolution			—	—	8	Bit		
Number of input channels			0	—	8	Channel		
Absolute error			—	—	±2.5	LSB	T_a = 25°C, AV_{CC} = 5 V	

Notes: 1. Select without pull-up MOS option for pins RC and RD when using these pins as analog input pins.

Input/Output Characteristics for Standard Pins (V_{CC} = 3.0 to 6.0 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20° to + 75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	$R5_1$–RD	$0.7V_{CC}$	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	$R5_1$–RD	–0.3	—	$0.3V_{CC}$	V		
Output high voltage	V_{OH}	R6–RB	V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 1.0 mA, V_{CC} = 3.5 to 6.0 V	
			V_{CC} – 0.5	—	—	V	$-I_{OH}$ = 0.5 mA, V_{CC} = 3.5 to 6.0 V	
							$-I_{OH}$ = 0.3 mA	
Output low voltage	V_{OL}	R6–RB	—	—	0.4	V	I_{OL} = 1.6 mA, V_{CC} = 3.5 to 6.0 V	
							I_{OL} = 0.4 mA	
Input/output leakage current	$\|I_{IL}\|$	R6–RD, $R5_1$–$R5_3$	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Pull-up MOS current	I_p	$R5_1$–RD	30	80	160	µA	V_{CC} = 5 V, V_{in} = 0 V	2
			10	30	60		V_{CC} = 3 V, V_{in} = 0 V	

Notes: 1. Excluding output buffer current.
2. Applies to I/O pins selected as with pull-up MOS by mask option.

Input/Output Characteristics for High-Voltage Pins (V_{CC} = 3.0 to 6.0 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20° to + 75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	D_0–D_{15}, $R5_0$, R0–R4	0.7V_{CC}	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_0–D_{15}, $R5_0$, R0–R4	V_{CC} – 40	—	0.3V_{CC}	V		
Output high voltage	V_{OH}	D_0–D_{15}, R0–R4	V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 15 mA, V_{CC} = 4 V to 6 V	
			V_{CC} – 2.0	—	—	V	$-I_{OH}$ = 10 mA, V_{CC} = 4 V to 6 V	
			V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 4 mA	
Output low voltage	V_{OL}	D_0–D_{15}, R0–R4	—	—	V_{CC} – 37	V	V_{disp} = V_{CC} – 40 V	1
			—	—	V_{CC} – 37	V	150 kΩ at V_{CC} – 40 V	2
Input/output leakage current	$\|I_{IL}\|$	D_0–D_{15}, $R5_0$, R0–R4	—	—	20	µA	V_{in} = V_{CC} – 40 V to V_{CC}	3
Pull-down MOS current	I_d	D_0–D_{15}, R0–R4	200	400	800	µA	V_{disp} = V_{CC} – 35 V, V_{in} = V_{CC}	1

Notes: 1. Applied to I/O pins selected as with pull-up MOS by mask option.
2. Applied to I/O pins selected as without pull-up MOS (PMOS open drain) by mask option.
3. Pull-up MOS current and output buffer current are excluded.

AC Characteristics (V_{CC} = 3.0 to 6.0 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20° to +75°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Oscillation frequency (1/4 division)	f_{OSC}	OSC_1, OSC_2	1.6	4	4.5	MHz	V_{CC} = 3.5 to 6.0 V	
			1.6	2	2.25	MHz		
Oscillation frequency (1/8 division)	f_{CL}	CL_1, CL_2	—	32.768	—	kHz		
Instruction cycle time	t_{cyc}		0.89	1	2.5	µs	V_{CC} = 3.5 to 6.0 V	
			1.78	2	2.5	µs		
Instruction cycle time	t_{SUBcyc}		—	244.14	—	µs		6
Oscillation stabilization time (crystal oscillator)	t_{RC}	OSC_1, OSC_2	—	—	40	ms	V_{CC} = 3.5 to 6.0 V	1
			—	—	60	ms		1
Oscillation stabilization time (ceramic oscillator)	t_{RC}	OSC_1, OSC_2	—	—	20	ms	V_{CC} = 3.5 to 6.0 V	1
			—	—	60	ms		1
Oscillation stabilization time	t_{RC}	CL_1, CL_2	—	—	2	s		2
External clock high width	t_{CPH}	OSC_1	92	—	—	ns	V_{CC} = 3.5 to 6.0 V	3
			203	—	—	ns		3
External clock low width	t_{CPL}	OSC_1	92	—	—	ns	V_{CC} = 3.5 to 6.0 V	3
			203	—	—	ns		3
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns	V_{CC} = 3.5 to 6.0 V	3
			—	—	20	ns		3
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns	V_{CC} = 3.5 to 6.0 V	3
			—	—	20	ns		3
$\overline{INT_0}$ high width	t_{I0H}	$\overline{INT_0}$	2	—	—	t_{cyc}/ t_{SUBcyc}		4, 6
$\overline{INT_0}$ low width	t_{I0L}	$\overline{INT_0}$	2	—	—	t_{cyc}/ t_{SUBcyc}		4, 6
$\overline{INT}$ high width	t_{I1H}	$\overline{INT_1}$–$\overline{INT_5}$	2	—	—	t_{cyc}		4
$\overline{INT}$ low width	t_{I1L}	$\overline{INT_1}$–$\overline{INT_5}$	2	—	—	t_{cyc}		4

AC Characteristics (V_{CC} = 3.0 to 6.0 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20° to +75°C, unless otherwise specified) (cont)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
RESET high width	t_{RSTH}	RESET	2	—	—	t_{cyc}		5
Input capacitance	C_{in}	All pins	—	—	30	pF	f = 1 MHz, V_{in} = 0 V	
Analog comparator stabilization time	t_{cstb}	$R6_0$/COMP	—	—	2	t_{cyc}		7

Notes:
1. The oscillation stabilization time is the period required for the oscillator to stabilize after V_{CC} reaches 3.0 V (3.5 V if V_{CC} = 3.5 to 6.0 V) at power-on or after RESET input goes high after stop mode is cancelled (figure 68). At power-on and when stop mode is cancelled, RESET must remain high for at least t_{RC} to ensure the oscillation stabilization time. If using an oscillator, contact the oscillator manufacturer to determine the circuit constants, since the stabilization time depends on the circuit constants and stray capacitances.
2. The oscillation stabilization time is the period required for the oscillator to stabilize after V_{CC} reaches 3.0 V at power-on (figure 69). If using a crystal oscillator, contact the manufacturer to determine the circuit constants, since the stabilization time depends on the circuit constants and stray capacitances.
3. Refer to figure 70.
4. Refer to figure 71.
5. Refer to figure 72. The MCU will malfunction if noise interferes with the falling edge of the RESET signal when releasing from reset state. The reset circuit must be sufficiently evaluated in the application system.
6. The t_{SUBcyc} unit applies when the MCU is in watch or subactive mode.
   t_{SUBcyc} = 244.14 µs (32.768-kHz crystal)
7. The analog comparator stabilization time is the period required for the analog comparator to stabilize and to read correct data after pin $R6_0$ switches to analog input mode.

Serial Interface Timing Characteristics (V_{CC} = 3.0 to 6.0 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20° to +75°C)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Output transmit clock cycle time	t_{Scyc}	$\overline{SCK_1}$, $\overline{SCK_2}$	1	—	—	t_{cyc}	Load shown in figure 74	1, 2
Output transmit clock high width	t_{SCKH}	$\overline{SCK_1}$, $\overline{SCK_2}$	0.4	—	—	t_{Scyc}		1, 2
Output transmit clock low width	t_{SCKL}	$\overline{SCK_1}$, $\overline{SCK_2}$	0.4	—	—	t_{Scyc}		1, 2
Output transmit clock rise time	t_{SCKr}	$\overline{SCK_1}$, $\overline{SCK_2}$	—	—	80	ns		1, 2
Output transmit clock fall time	t_{SCKf}	$\overline{SCK_1}$, $\overline{SCK_2}$	—	—	80	ns		1, 2
Input transmit clock cycle time	t_{Scyc}	$\overline{SCK_1}$, $\overline{SCK_2}$	2	—	—	t_{cyc}		1
Input transmit clock high width	t_{SCKH}	$\overline{SCK_1}$, $\overline{SCK_2}$	0.4	—	—	t_{Scyc}		1
Input transmit clock low width	t_{SCKL}	$\overline{SCK_1}$, $\overline{SCK_2}$	0.4	—	—	t_{Scyc}		1
Input transmit clock rise time	t_{SCKr}	$\overline{SCK_1}$, $\overline{SCK_2}$	—	—	80	ns		1
Input transmit clock fall time	t_{SCKf}	$\overline{SCK_1}$, $\overline{SCK_2}$	—	—	80	ns		1
Serial output data delay time	t_{DSO}	SO_1, SO_2	—	—	600	ns	Load shown in figure 74	1, 2
Serial input data setup time	t_{SSI}	SI_1, SI_2	200	—	—	ns		1
Serial input data hold time	t_{HSI}	SI_1, SI_2	400	—	—	ns		1

Notes: 1. Refer to figure 73.
2. Refer to figure 74.

Serial Interface Timing Characteristics (V_{CC} = 3.5 to 6.0 V)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Output transmit clock cycle time	t_{Scyc}	$\overline{SCK_1}$, $\overline{SCK_2}$	1	—	—	t_{cyc}	Load shown in figure 74	1, 2
Output transmit clock high width	t_{SCKH}	$\overline{SCK_1}$, $\overline{SCK_2}$	0.4	—	—	t_{Scyc}		1, 2
Output transmit clock low width	t_{SCKL}	$\overline{SCK_1}$, $\overline{SCK_2}$	0.4	—	—	t_{Scyc}		1, 2
Output transmit clock rise time	t_{SCKr}	$\overline{SCK_1}$, $\overline{SCK_2}$	—	—	40	ns		1, 2
Output transmit clock fall time	t_{SCKf}	$\overline{SCK_1}$, $\overline{SCK_2}$	—	—	40	ns		1, 2
Input transmit clock cycle time	t_{Scyc}	$\overline{SCK_1}$, $\overline{SCK_2}$	2	—	—	t_{cyc}		1
Input transmit clock high width	t_{SCKH}	$\overline{SCK_1}$, $\overline{SCK_2}$	0.4	—	—	t_{Scyc}		1
Input transmit clock low width	t_{SCKL}	$\overline{SCK_1}$, $\overline{SCK_2}$	0.4	—	—	t_{Scyc}		1
Input transmit clock rise time	t_{SCKr}	$\overline{SCK_1}$, $\overline{SCK_2}$	—	—	40	ns		1
Input transmit clock fall time	t_{SCKf}	$\overline{SCK_1}$, $\overline{SCK_2}$	—	—	40	ns		1
Serial output data delay time	t_{DSO}	SO_1, SO_2	—	—	300	ns	Load shown in figure 74	1, 2
Serial input data setup time	t_{SSI}	SI_1, SI_2	100	—	—	ns		1
Serial input data hold time	t_{HSI}	SI_1, SI_2	200	—	—	ns		1

Notes: 1. Refer to figure 73.
2. Refer to figure 74.

HD404439 Electrical Characteristics

DC Characteristics (V_{CC} = 3.0 to 6.0 V, GND = 0.0 V, T_a = –20° to +75°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	RESET, $\overline{SCK_1}$, $\overline{SCK_2}$, $\overline{INT_0}$–$\overline{INT_5}$	0.85V_{CC}	—	V_{CC} + 0.3	V		
		SI_1, SI_2	0.7V_{CC}	—	V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.5	—	V_{CC} + 0.3	V	V_{CC} = 3.5 to 6.0 V	
			V_{CC} – 0.3	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	RESET, $\overline{SCK_1}$, $\overline{SCK_2}$, $\overline{INT_0}$–$\overline{INT_5}$	–0.3	—	0.2V_{CC}	V		
		SI_1, SI_2	–0.3	—	0.3V_{CC}	V		
		OSC_1	–0.3	—	0.5	V	V_{CC} = 3.5 to 6.0 V	
			–0.3	—	0.3	V		
Output high voltage	V_{OH}	$\overline{SCK_1}$, $\overline{SCK_2}$, SO_1, SO_2, BUZZ, TOC, TOD, TOE_1, TOE_2, TOG	V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 1.0 mA, V_{CC} = 3.5 to 6.0 V	
			V_{CC} – 0.5	—	—	V	$-I_{OH}$ = 0.5 mA, V_{CC} = 3.5 to 6.0 V	
							$-I_{OH}$ = 0.3 mA	
Output low voltage	V_{OL}	$\overline{SCK_1}$, $\overline{SCK_2}$, SO_1, SO_2, BUZZ, TOC, TOD, TOE_1, TOE_2, TOG	—	—	0.4	V	I_{OL} = 1.6 mA, V_{CC} = 3.5 to 6.0 V	
							I_{OL} = 0.4 mA	
I/O leakage current	$\|I_{IL}\|$	RESET, $\overline{SCK_1}$, $\overline{SCK_2}$, SI_1, SI_2, SO_1, SO_2, BUZZ, OSC_1, TOC, TOD, TOE_1, TOE_2, TOG	—	—	1	µA	V_{in} = 0 V to V_{CC}	1

Notes: 1. Excluding output buffer current.

DC Characteristics (V_{CC} = 3.0 to 6.0 V, GND = 0.0 V, T_a = –20° to +75°C, unless otherwise specified) (cont)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Current dissipation in active mode	I_{CC}	V_{CC}	—	—	8.0	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz, digital input mode	2, 5
			—	—	4.5	mA	V_{CC} = 3 V, f_{OSC} = 2 MHz, digital input mode	2, 5
	I_{CMP}		—	—	12.0	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz, analog input mode	3, 5
			—	—	7.0	mA	V_{CC} = 3 V, f_{OSC} = 2 MHz, 1/4 division ratio, analog input mode	3, 5
Current dissipation in standby mode	I_{SBY}	V_{CC}	—	—	3.0	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	4, 5
			—	—	1.5	mA	V_{CC} = 3 V, f_{OSC} = 2 MHz	4, 5
Current dissipation in subactive mode	I_{SUB}	V_{CC}	—	—	70	µA	$V_{in\ (\overline{TEST})}$ = V_{CC} – 0.3 V to V_{CC} $V_{in\ (RESET)}$ = 0 to 0.3 V, V_{CC} = 3 V, 32.768-kHz crystal oscillator	6, 7
Current dissipation in watch mode	I_{WATCH}	V_{CC}	—	—	15	µA	$V_{in\ (\overline{TEST})}$ = V_{CC} – 0.3 V to V_{CC}, $V_{in\ (RESET)}$ = 0 to 0.3 V, V_{CC} = 3 V, 32.768-kHz crystal oscillator	6, 7, 8
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	—	10	µA	$V_{in\ (\overline{TEST})}$ = V_{CC} – 0.3 V to V_{CC}, $V_{in\ (RESET)}$ = 0 to 0.3 V, no 32.768-kHz oscillator	6
Watch mode retaining voltage	V_{WATCH}	V_{CC}	3.5	—	6.0	V	V_{CC} = 3.5 to 6.0 V	6, 7, 8
			3.0	—	6.0	V		
Stop mode retaining voltage	V_{STOP}	V_{CC}	2	—	—	V	No 32.768-kHz oscillator	

DC Characteristics (V_{CC} = 3.0 to 6.0 V, GND = 0.0 V, T_a = –20° to +75°C, unless otherwise specified) (cont)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IHA}	$R6_0$/COMP	V_{ref} + 0.1	—	—	V	Analog compare mode	
Input low voltage	V_{ILA}	$R6_0$/COMP	—	—	V_{ref} – 0.1	V	Analog compare mode	
Range of analog input reference voltage	V_{ref}	$R6_1/V_{ref}$	0	—	V_{CC} – 1.2	V		
Allowable error of internal reference voltage	V_{OFS}		–100	—	+100	mV	V_{OFS} = reference voltage – V_{ref}	9

Notes: 2. I_{CC} is the source current when no I/O current is flowing while the MCU is in reset state.
Test conditions: MCU: Reset
Pins: RESET, $\overline{TEST}$ at V_{CC}
$R5_1$–RD at V_{CC}
D_0–D_{15}, R0–R3, R4, $R5_0$ at GND

3. I_{CMP} is the source current when no I/O current is flowing while the $R6_0$/COMP pin is in analog input mode.
TEST conditions: Pins: $R6_0$/COMP, $R6_1/V_{ref}$ at GND

4. I_{SBY} is the source current when no I/O current is flowing while the MCU timer is in operation.
Test conditions: MCU: I/O same as at reset
Standby mode
Pins: RESET at GND
$\overline{TEST}$ at V_{CC}
$R5_1$–RD at V_{CC}
D_0–D_{15}, R0–R3, R4, $R5_0$ at GND

5. Power dissipation, while the MCU is operating or in standby mode, is in proportion to f_{OSC}. The value of the dissipation current when $f_{OSC} = \chi$ MHz is given by the following equation:
Maximum value ($f_{OSC} = \chi$ MHz) = $\chi/4 \times$ maximum value (f_{OSC} = 4 MHz)

6. Source current when no I/O current is flowing.
Test conditions: Pins: $R5_1$–RD at V_{CC}
D_0–D_{15}, R0–R4, $R5_0$ at GND

7. Applies when '32-kHz CPU operation' is selected as an optional function.

8. Applies when 'no 32-kHz CPU operation with clock time base' is selected as an optional function.

9. The reference voltage is the expected internal V_{ref} voltage selected by the compare control register (CCR).

A/D Converter (V_{CC} = 3.0 to 6.0 V, AGND = GND, T_a = –20° to +75°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Analog supply voltage	AV_{CC}	AV_{CC}	V_{CC} – 0.3	V_{CC}	V_{CC} + 0.3	V		
Analog input voltage	AV_{in}	AN_0–AN_7	AGND	—	AV_{CC}	V		1
Current between AV_{CC} and AGND	AI_{CC}	AV_{CC}	—	—	150	µA	AV_{CC} = 5 V, $V_{in\ (\overline{RESET})}$ = 0 to 0.3 V, $V_{in\ (\overline{TEST})}$ = V_{CC} – 0.3 V to V_{CC}	
	AI_{STOP}	AV_{CC}	—	—	10	µA	$V_{in\ (\overline{RESET})}$ = 0 to 0.3 V, $V_{in\ (\overline{TEST})}$ = V_{CC} – 0.3 V to V_{CC}, stop mode, no 32.768-kHz oscillator	
Analog input capacitance	C_{ain}	AN_0–AN_7	—	—	30	pF		
Resolution			—	—	8	Bit		
Number of input channels			0	—	8	Channel		
Absolute error			—	—	±2.5	LSB	T_a = 25°C, AV_{CC} = 5 V	

Notes: 1. Select without pull-up MOS option for pins RC and RD when using these pins as analog input pins.

Input/Output Characteristics for Standard Pins (V_{CC} = 3.0 to 6.0 V, GND = 0.0 V, T_a = –20 °to + 75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	$R5_1$–RD	$0.7V_{CC}$	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	$R5_1$–RD	–0.3	—	$0.3V_{CC}$	V		
Output high voltage	V_{OH}	R6–RB	V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 1.0 mA, V_{CC} = 3.5 to 6.0 V	
			V_{CC} – 0.5	—	—	V	$-I_{OH}$ = 0.5 mA, V_{CC} = 3.5 to 6.0 V	
							$-I_{OH}$ = 0.3 mA	
Output low voltage	V_{OL}	R6–RB	—	—	0.4	V	I_{OL} = 1.6 mA, V_{CC} = 3.5 to 6.0 V	
							I_{OL} = 0.4 mA	
Input/output leakage current	$\|I_{IL}\|$	$R5_1$–RD	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
Pull-up MOS current	I_p	$R5_1$–RD	30	80	160	µA	V_{CC} = 5 V, V_{in} = 0 V	2
			10	30	60		V_{CC} = 3 V, V_{in} = 0 V	

Notes: 1. Excluding pull-up MOS current and output buffer current.
2. Applies to I/O pins selected as with pull-up MOS by mask option.

Input/Output Characteristics for Open-Drain PMOS Pins (V_{CC} = 3.0 to 6.0 V, GND = 0.0 V, T_a = –20° to + 75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	D_0–D_{15}, $R5_0$, R0–R4	$0.7V_{CC}$	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_0–D_{15}, $R5_0$, R0–R4	–0.3	—	$0.3V_{CC}$	V		
Output high voltage	V_{OH}	D_0–D_{15}, R0–R4	V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 15 mA, V_{CC} = 4 V to 6 V	
			V_{CC} – 2.0	—	—	V	$-I_{OH}$ = 10 mA, V_{CC} = 4 V to 6 V	
			V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 4 mA	
Input/output leakage current	$\|I_{IL}\|$	D_0–D_{15}, $R5_0$, R0–R4	—	—	4	µA	V_{in} = 0 V to V_{CC}	1

Notes: 1. Excluding output buffer current.

AC Characteristics (V_{CC} = 3.0 to 6.0 V, GND = 0.0 V, T_a = –20° to +75°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Oscillation frequency (1/4 division)	f_{OSC}	OSC_1, OSC_2	1.6	4	4.5	MHz	V_{CC} = 3.5 to 6.0 V	
			1.6	2	2.25	MHz		
Oscillation frequency (1/8 division)	f_{CL}	CL_1, CL_2	—	32.768	—	kHz		
Instruction cycle time	t_{cyc}		0.89	1	2.5	µs	V_{CC} = 3.5 to 6.0 V	
			1.78	2	2.5	µs		
Instruction cycle time	t_{SUBcyc}		—	244.14	—	µs		6
Oscillation stabilization time (crystal oscillator)	t_{RC}	OSC_1, OSC_2	—	—	40	ms	V_{CC} = 3.5 to 6.0 V	1
			—	—	60	ms		1
Oscillation stabilization time (ceramic oscillator)	t_{RC}	OSC_1, OSC_2	—	—	20	ms	V_{CC} = 3.5 to 6.0 V	1
			—	—	60	ms		1
Oscillation stabilization time	t_{RC}	CL_1, CL_2	—	—	2	s		2
External clock high width	t_{CPH}	OSC_1	92	—	—	ns	V_{CC} = 3.5 to 6.0 V	3
			203	—	—	ns		3
External clock low width	t_{CPL}	OSC_1	92	—	—	ns	V_{CC} = 3.5 to 6.0 V	3
			203	—	—	ns		3
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns	V_{CC} = 3.5 to 6.0 V	3
			—	—	20	ns		3
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns	V_{CC} = 3.5 to 6.0 V	3
			—	—	20	ns		3
$\overline{INT_0}$ high width	t_{I0H}	$\overline{INT_0}$	2	—	—	t_{cyc}/ t_{SUBcyc}		4, 6
$\overline{INT_0}$ low width	t_{I0L}	$\overline{INT_0}$	2	—	—	t_{cyc}/ t_{SUBcyc}		4, 6
$\overline{INT}$ high width	t_{I1H}	$\overline{INT_1}$–$\overline{INT_5}$	2	—	—	t_{cyc}		4
$\overline{INT}$ low width	t_{I1L}	$\overline{INT_1}$–$\overline{INT_5}$	2	—	—	t_{cyc}		4

AC Characteristics (V_{CC} = 3.0 to 6.0 V, GND = 0.0 V, T_a = –20° to +75°C, unless otherwise specified) (cont)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
RESET high width	t_{RSTH}	RESET	2	—	—	t_{cyc}		5
Input capacitance	C_{in}	All pins	—	—	30	pF	f = 1 MHz, V_{in} = 0 V	
Analog comparator stabilization time	t_{cstb}	$R6_0$/COMP	—	—	2	t_{cyc}		7

Notes:
1. The oscillation stabilization time is the period required for the oscillator to stabilize after V_{CC} reaches 3.0 V (3.5 V if V_{CC} = 3.5 to 6.0 V) at power-on or after RESET input goes high after stop mode is cancelled (figure 68). At power-on and when stop mode is cancelled, RESET must remain high for at least t_{RC} to ensure the oscillation stabilization time. If using an oscillator, contact the oscillator manufacturer to determine the circuit constants, since the stabilization time depends on the circuit constants and stray capacitances.
2. The oscillation stabilization time is the period required for the oscillator to stabilize after V_{CC} reaches 3.0 V at power-on (figure 69). If using a crystal oscillator, contact the manufacturer to determine the circuit constants, since the stabilization time depends on the circuit constants and stray capacitances.
3. Refer to figure 70.
4. Refer to figure 71.
5. Refer to figure 72. The MCU will malfunction if noise conflicts with the falling edge of the RESET signal when releasing from reset state. The reset circuit must be sufficiently evaluated in the application system.
6. The t_{SUBcyc} unit applies when the MCU is in watch or subactive mode.
   t_{SUBcyc} = 244.14 µs (32.768-kHz crystal)
7. The analog comparator stabilization time is the period required for the analog comparator to stabilize and to read correct data after pin $R6_0$ switches to analog input mode.

Serial Interface Timing Characteristics (V_{CC} = 3.0 to 6.0 V, GND = 0.0 V, T_a = –20° to +75°C)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Output transmit clock cycle time	t_{Scyc}	$\overline{SCK}_1$, $\overline{SCK}_2$	1	—	—	t_{cyc}	Load shown in figure 74	1, 2
Output transmit clock high width	t_{SCKH}	$\overline{SCK}_1$, $\overline{SCK}_2$	0.4	—	—	t_{Scyc}		1, 2
Output transmit clock low width	t_{SCKL}	$\overline{SCK}_1$, $\overline{SCK}_2$	0.4	—	—	t_{Scyc}		1, 2
Output transmit clock rise time	t_{SCKr}	$\overline{SCK}_1$, $\overline{SCK}_2$	—	—	80	ns		1, 2
Output transmit clock fall time	t_{SCKf}	$\overline{SCK}_1$, $\overline{SCK}_2$	—	—	80	ns		1, 2
Input transmit clock cycle time	t_{Scyc}	$\overline{SCK}_1$, $\overline{SCK}_2$	2	—	—	t_{cyc}		1
Input transmit clock high width	t_{SCKH}	$\overline{SCK}_1$, $\overline{SCK}_2$	0.4	—	—	t_{Scyc}		1
Input transmit clock low width	t_{SCKL}	$\overline{SCK}_1$, $\overline{SCK}_2$	0.4	—	—	t_{Scyc}		1
Input transmit clock rise time	t_{SCKr}	$\overline{SCK}_1$, $\overline{SCK}_2$	—	—	80	ns		1
Input transmit clock fall time	t_{SCKf}	$\overline{SCK}_1$, $\overline{SCK}_2$	—	—	80	ns		1
Serial output data delay time	t_{DSO}	SO_1, SO_2	—	—	600	ns	Load shown in figure 74	1, 2
Serial input data setup time	t_{SSI}	SI_1, SI_2	200	—	—	ns		1
Serial input data hold time	t_{HSI}	SI_1, SI_2	400	—	—	ns		1

Notes: 1. Refer to figure 73.
2. Refer to figure 74.

Serial Interface Timing Characteristics (V_{CC} = 3.5 to 6.0 V)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Output transmit clock cycle time	t_{Scyc}	$\overline{SCK}_1$, $\overline{SCK}_2$	1	—	—	t_{cyc}	Load shown in figure 74	1, 2
Output transmit clock high width	t_{SCKH}	$\overline{SCK}_1$, $\overline{SCK}_2$	0.4	—	—	t_{Scyc}		1, 2
Output transmit clock low width	t_{SCKL}	$\overline{SCK}_1$, $\overline{SCK}_2$	0.4	—	—	t_{Scyc}		1, 2
Output transmit clock rise time	t_{SCKr}	$\overline{SCK}_1$, $\overline{SCK}_2$	—	—	40	ns		1, 2
Output transmit clock fall time	t_{SCKf}	$\overline{SCK}_1$, $\overline{SCK}_2$	—	—	40	ns		1, 2
Input transmit clock cycle time	t_{Scyc}	$\overline{SCK}_1$, $\overline{SCK}_2$	2	—	—	t_{cyc}		1
Input transmit clock high width	t_{SCKH}	$\overline{SCK}_1$, $\overline{SCK}_2$	0.4	—	—	t_{Scyc}		1
Input transmit clock low width	t_{SCKL}	$\overline{SCK}_1$, $\overline{SCK}_2$	0.4	—	—	t_{Scyc}		1
Input transmit clock rise time	t_{SCKr}	$\overline{SCK}_1$, $\overline{SCK}_2$	—	—	40	ns		1
Input transmit clock fall time	t_{SCKf}	$\overline{SCK}_1$, $\overline{SCK}_2$	—	—	40	ns		1
Serial output data delay time	t_{DSO}	SO_1, SO_2	—	—	300	ns	Load shown in figure 74	1, 2
Serial input data setup time	t_{SSI}	SI_1, SI_2	100	—	—	ns		1
Serial input data hold time	t_{HSI}	SI_1, SI_2	200	—	—	ns		1

Notes: 1. Refer to figure 73.
2. Refer to figure 74.

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DC Characteristics (V_{CC} = 3.0 to 5.5 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20° to +75°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	RESET, $\overline{SCK_1}$, $\overline{SCK_2}$, $\overline{INT_0}$–$\overline{INT_5}$	0.85V_{CC}	—	V_{CC} + 0.3	V		
		SI_1, SI_2	0.7V_{CC}	—	V_{CC} + 0.3	V		
		OSC_1	V_{CC} – 0.5	—	V_{CC} + 0.3	V	V_{CC} = 3.5 to 5.5 V	
			V_{CC} – 0.3	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	RESET, $\overline{SCK_1}$, $\overline{SCK_2}$, $\overline{INT_0}$–$\overline{INT_5}$	–0.3	—	0.2V_{CC}	V		
		SI_1, SI_2	–0.3	—	0.3V_{CC}	V		
		OSC_1	–0.3	—	0.5	V	V_{CC} = 3.5 to 5.5 V	
			–0.3	—	0.3	V		
Output high voltage	V_{OH}	$\overline{SCK_1}$, $\overline{SCK_2}$, SO_1, SO_2, BUZZ, TOC, TOD, TOE_1, TOE_2, TOG	V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 1.0 mA, V_{CC} = 3.5 to 5.5 V	
			V_{CC} – 0.5	—	—	V	$-I_{OH}$ = 0.5 mA, V_{CC} = 3.5 to 5.5 V	
							$-I_{OH}$ = 0.3 mA	
Output low voltage	V_{OL}	$\overline{SCK_1}$, $\overline{SCK_2}$, SO_1, SO_2, BUZZ, TOC, TOD, TOE_1, TOE_2, TOG	—	—	0.4	V	I_{OL} = 1.6 mA, V_{CC} = 3.5 to 5.5 V	
							I_{OL} = 0.4 mA	
I/O leakage current	$\|I_{IL}\|$	RESET, $\overline{SCK_1}$, $\overline{SCK_2}$, SI_1, SI_2, SO_1, SO_2, BUZZ, OSC_1, TOC, TOD, TOE_1, TOE_2, TOG	—	—	1	µA	V_{in} = 0 V to V_{CC}	1

Notes: 1. Excluding output buffer current.

DC Characteristics (V_{CC} = 3.0 to 5.5 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20° to +75°C, unless otherwise specified) (cont)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Current dissipation in active mode	I_{CC}	V_{CC}	—	—	8.0	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz, digital input mode	2, 5
			—	—	4.5	mA	V_{CC} = 3 V, f_{OSC} = 2 MHz, digital input mode	2, 5
	I_{CMP}		—	—	12.0	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz, analog input mode	3, 5
			—	—	7.0	mA	V_{CC} = 3 V, f_{OSC} = 2 MHz, analog input mode	3, 5
Current dissipation in standby mode	I_{SBY}	V_{CC}	—	—	3.0	mA	V_{CC} = 5 V, f_{OSC} = 4 MHz	4, 5
			—	—	1.5	mA	V_{CC} = 3 V, f_{OSC} = 2 MHz	4, 5
Current dissipation in subactive mode	I_{SUB}	V_{CC}	—	—	150	µA	$V_{in\ (TEST)}$ = V_{CC} –0.3 V to V_{CC} $V_{in\ (RESET)}$ = 0 to 0.3 V, V_{CC} = 3 V, 32.768-kHz crystal oscillator	6
Current dissipation in watch mode	I_{WATCH}	V_{CC}	—	—	15	µA	$V_{in\ (TEST)}$ = V_{CC} – 0.3 V to V_{CC}, $V_{in\ (RESET)}$ = 0 to 0.3 V, V_{CC} = 3 V, 32.768-kHz crystal oscillator	6
Current dissipation in stop mode	I_{STOP}	V_{CC}	—	—	15	µA	$V_{in\ (TEST)}$ = V_{CC} – 0.3 V to V_{CC}, $V_{in\ (RESET)}$ = 0 to 0.3 V, no 32.768-kHz oscillator	6
Watch mode retaining voltage	V_{WATCH}	V_{CC}	3.5	—	5.5	V	V_{CC} = 3.5 to 5.5 V	
			3.0	—	5.5	V		
Stop mode retaining voltage	V_{STOP}	V_{CC}	2	—	—	V	No 32.768-kHz oscillator	

DC Characteristics (V_{CC} = 3.0 to 5.5 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20° to +75°C, unless otherwise specified) (cont)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IHA}	$R6_0$/COMP	V_{ref} + 0.1	—	—	V	Analog compare mode	
Input low voltage	V_{ILA}	$R6_0$/COMP	—	—	V_{ref} – 0.1	V	Analog compare mode	
Range of analog input reference voltage	V_{ref}	$R6_1/V_{ref}$	0	—	V_{CC} – 1.2	V		
Allowable error of internal reference voltage	V_{OFS}		–100	—	+100	mV	V_{OFS} = reference voltage – V_{ref}	7

Notes: 2. I_{CC} is the source current when no I/O current is flowing while the MCU is in reset state.
Test conditions: MCU: Reset
Pins: RESET, TEST at V_{CC}
$R5_1$–RD at V_{CC}
D_0–D_{15}, R0–R4, $R5_0$ at V_{disp}

3. I_{CMP} is the source current when no I/O current is flowing while the $R6_0$/COMP pin is in analog input mode.
Test conditions: $R6_0$/COMP, $R6_1/V_{ref}$ at GND

4. I_{SBY} is the source current when no I/O current is flowing while the MCU timer is in operation.
Test conditions: MCU: I/O same as at reset
Standby mode
Pins: RESET at GND
TEST at V_{CC}
$R5_1$–RD at V_{CC}
D_0–D_{15}, R0–R4, $R5_0$ at V_{disp}

5. Power dissipation, while the MCU is operating or in standby mode, is in proportion to f_{OSC}. The value of the dissipation current when f_{OSC} = χ MHz is given by the following equation: Maximum value (f_{OSC} = χ MHz) = $\chi/4$ × maximum value (f_{OSC} = 4 MHz)

6. The source current when no I/O current is flowing.
Test conditions: Pins: $R5_1$–RD at V_{CC}
D_0–D_{15}, R0–R4, $R5_0$ at V_{disp}

7. The reference voltage is the expected internal V_{ref} voltage selected by the compare control register (CCR).
Example: when CCR = $9, reference voltage is 2/11 × V_{CC}.

A/D Converter (V_{CC} = 3.0 to 5.5 V, AGND = GND, T_a = –20° to +75°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Analog supply voltage	AV_{CC}	AV_{CC}	V_{CC} – 0.3	V_{CC}	V_{CC} + 0.3	V		
Analog input voltage	AV_{in}	AN_0–AN_7	AGND	—	AV_{CC}	V		
Current between AV_{CC} and AGND	AI_{CC}	AV_{CC}	—	—	150	µA	AV_{CC} = 5 V, $V_{in\ (\overline{RESET})}$ = 0 to 0.3 V, $V_{in\ (\overline{TEST})}$ = V_{CC} – 0.3 V to V_{CC}	
	AI_{STOP}	AV_{CC}	—	—	15	µA	$V_{in\ (\overline{RESET})}$ = 0 to 0.3 V, $V_{in\ (\overline{TEST})}$ = V_{CC} – 0.3 V to V_{CC}, stop mode, no 32.768-kHz oscillator	
Analog input capacitance	C_{ain}	AN_0–AN_7	—	—	30	pF		
Resolution			—	—	8	Bit		
Number of input channels			0	—	8	Channel		
Absolute error			—	—	±2.5	LSB	T_a = 25°C, AV_{CC} = 5 V	

Input/Output Characteristics for Standard Pins (V_{CC} = 3.0 to 5.5 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20° to + 75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	$R5_1$–RD	$0.7V_{CC}$	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	$R5_1$–RD	–0.3	—	$0.3V_{CC}$	V		
Output high voltage	V_{OH}	R6–RB	V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 1.0 mA, V_{CC} = 3.5 to 5.5 V	
			V_{CC} – 0.5	—	—	V	$-I_{OH}$ = 0.5 mA, V_{CC} = 3.5 to 5.5 V	
							$-I_{OH}$ = 0.3 mA	
Output low voltage	V_{OL}	R6–RB	—	—	0.4	V	I_{OL} = 1.6 mA, V_{CC} = 3.5 to 5.5 V	
							I_{OL} = 0.4 mA	
Input/output leakage current	$\|I_{IL}\|$	R6–RD, $R5_1$, $R5_3$	—	—	1	µA	V_{in} = 0 V to V_{CC}	1
		$R5_2$			20			

Notes: 1. Excluding output buffer current.

Input/Output Characteristics for High-Voltage Pins (V_{CC} = 3.0 to 5.5 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20° to + 75°C, unless otherwise specified)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	D_0–D_{15}, $R5_0$, R0–R4	$0.7V_{CC}$	—	V_{CC} + 0.3	V		
Input low voltage	V_{IL}	D_0–D_{15}, $R5_0$, R0–R4	V_{CC} – 40	—	$0.3V_{CC}$	V		
Output high voltage	V_{OH}	D_0–D_{15}, R0–R4	V_{CC} – 3.0	—	—	V	$-I_{OH}$ = 15 mA, V_{CC} = 4.0 to 5.5 V	
			V_{CC} – 2.0	—	—	V	$-I_{OH}$ = 10 mA, V_{CC} = 4.0 to 5.5 V	
			V_{CC} – 1.0	—	—	V	$-I_{OH}$ = 4 mA	
Output low voltage	V_{OL}	D_0–D_{15}, R0–R4	—	—	V_{CC} – 37	V	150 kΩ at V_{CC} – 40 V	
Input/output leakage current	$\|I_{IL}\|$	D_0–D_{15}, $R5_0$, R0–R4	—	—	20	µA	V_{in} = V_{CC} – 40 V to V_{CC}	1

Notes: 1. Excluding output buffer current.

AC Characteristics (V_{CC} = 3.0 to 5.5 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20° to +75°C, unless otherwise specified)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
Oscillation frequency (1/4 division)	f_{OSC}	OSC_1, OSC_2	1.6	4	4.5	MHz	V_{CC} = 3.5 to 5.5 V	
			1.6	2	2.25	MHz		
Oscillation frequency (1/8 division)	f_{CL}	CL_1, CL_2	—	32.768	—	kHz		
Instruction cycle time	t_{cyc}		0.89	1	2.5	µs	V_{CC} = 3.5 to 5.5 V	
			1.78	2	2.5	µs		
Instruction cycle time	t_{SUBcyc}		—	244.14	—	µs		7
Oscillation stabilization time (crystal oscillator)	t_{RC}	OSC_1, OSC_2	—	—	40	ms	V_{CC} = 3.5 to 5.5 V	1
			—	—	60	ms		1
Oscillation stabilization time (ceramic oscillator)	t_{RC}	OSC_1, OSC_2	—	—	20	ms	V_{CC} = 3.5 to 5.5 V	1
			—	—	60	ms		1
Oscillation stabilization time	t_{RC}	CL_1, CL_2	—	—	2	s		2
External clock high width	t_{CPH}	OSC_1	92	—	—	ns	V_{CC} = 3.5 to 5.5 V	3
			203	—	—	ns		3
External clock low width	t_{CPL}	OSC_1	92	—	—	ns	V_{CC} = 3.5 to 5.5 V	3
			203	—	—	ns		3
External clock rise time	t_{CPr}	OSC_1	—	—	20	ns	V_{CC} = 3.5 to 5.5 V	3
			—	—	20	ns		3
External clock fall time	t_{CPf}	OSC_1	—	—	20	ns	V_{CC} = 3.5 to 5.5 V	3
			—	—	20	ns		3
$\overline{INT_0}$ high width	t_{I0H}	$\overline{INT_0}$	2	—	—	t_{cyc}/ t_{SUBcyc}		4, 6
$\overline{INT_0}$ low width	t_{I0L}	$\overline{INT_0}$	2	—	—	t_{cyc}/ t_{SUBcyc}		4, 6
$\overline{INT}$ high width	t_{I1H}	$\overline{INT_1}$–$\overline{INT_5}$	2	—	—	t_{cyc}		4
$\overline{INT}$ low width	t_{I1L}	$\overline{INT_1}$–$\overline{INT_5}$	2	—	—	t_{cyc}		4

Refer to notes on the next page.

AC Characteristics (V_{CC} = 3.0 to 5.5 V, GND = 0.0 V, V_{disp} = V_{CC} – 40 V to V_{CC}, T_a = –20° to +75°C, unless otherwise specified) (cont)

Item	Symbol	Pin(s)	Min	Typ	Max	Unit	Test Condition	Notes
RESET high width	t_{RSTH}	RESET	2	—	—	t_{cyc}		5
Input capacitance	C_{in}	$R5_2$	—	—	180	pF	f = 1 MHz, V_{in} = 0 V	
		Others	—	—	30	pF		
Analog comparator stabilization time	t_{cstb}	$R6_0$/COMP	—	—	2	t_{cyc}		7

Notes:
1. The oscillation stabilization time is the period required for the oscillator to stabilize after V_{CC} reaches 3.0 V (3.5 V if V_{CC} = 3.5 to 5.5 V) at power-on or after RESET input goes high after stop mode is cancelled (figure 68). At power-on and when stop mode is cancelled, RESET must remain high for at least t_{RC} to ensure the oscillation stabilization time. If using an oscillator, contact the oscillator manufacturer to determine the circuit constants, since the stabilization time depends on the circuit constants and stray capacitances.
2. The oscillation stabilization time is the period required for the oscillator to stabilize after V_{CC} reaches 3.0 V at power-on (figure 69). If using a crystal oscillator, contact the manufacturer to determine the circuit constants, since the stabilization time depends on the circuit constants and stray capacitances.
3. Refer to figure 70.
4. Refer to figure 71.
5. Refer to figure 72. The MCU will malfunction if noise conflicts with the falling edge of the RESET signal when releasing from reset state. The reset circuit must be sufficiently evaluated in the application system.
6. The t_{SUBcyc} unit applies when the MCU is in watch or subactive mode.
   t_{SUBcyc} = 244.14 µs (32.768-kHz crystal)
7. The analog comparator stabilization time is the period required for the analog comparator to stabilize and to read correct data after pin $R6_0$ switches to analog input mode.

Serial Interface Timing Characteristics (V_{CC} = 3.0 to 5.5 V, GND = 0.0 V, V_{dlsp} = V_{CC} – 40 V to V_{CC}, T_a = –20° to +75°C)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Output transmit clock cycle time	t_{Scyc}	$\overline{SCK_1}$, $\overline{SCK_2}$	1	—	—	t_{cyc}	Load shown in figure 74	1, 2
Output transmit clock high width	t_{SCKH}	$\overline{SCK_1}$, $\overline{SCK_2}$	0.4	—	—	t_{Scyc}		1, 2
Output transmit clock low width	t_{SCKL}	$\overline{SCK_1}$, $\overline{SCK_2}$	0.4	—	—	t_{Scyc}		1, 2
Output transmit clock rise time	t_{SCKr}	$\overline{SCK_1}$, $\overline{SCK_2}$	—	—	80	ns		1, 2
Output transmit clock fall time	t_{SCKf}	$\overline{SCK_1}$, $\overline{SCK_2}$	—	—	80	ns		1, 2
Input transmit clock cycle time	t_{Scyc}	$\overline{SCK_1}$, $\overline{SCK_2}$	2	—	—	t_{cyc}		1
Input transmit clock high width	t_{SCKH}	$\overline{SCK_1}$, $\overline{SCK_2}$	0.4	—	—	t_{Scyc}		1
Input transmit clock low width	t_{SCKL}	$\overline{SCK_1}$, $\overline{SCK_2}$	0.4	—	—	t_{Scyc}		1
Input transmit clock rise time	t_{SCKr}	$\overline{SCK_1}$, $\overline{SCK_2}$	—	—	80	ns		1
Input transmit clock fall time	t_{SCKf}	$\overline{SCK_1}$, $\overline{SCK_2}$	—	—	80	ns		1
Serial output data delay time	t_{DSO}	SO_1, SO_2	—	—	600	ns	Load shown in figure 74	1, 2
Serial input data setup time	t_{SSI}	SI_1, SI_2	200	—	—	ns		1
Serial input data hold time	t_{HSI}	SI_1, SI_2	400	—	—	ns		1

Notes: 1. Refer to figure 73.
2. Refer to figure 74.

Serial Interface Timing Characteristics (V_{CC} = 3.5 to 5.5 V)

Item	Symbol	Pins	Min	Typ	Max	Unit	Test Condition	Notes
Output transmit clock cycle time	t_{Scyc}	$\overline{SCK}_1$, $\overline{SCK}_2$	1	—	—	t_{cyc}	Load shown in figure 74	1, 2
Output transmit clock high width	t_{SCKH}	$\overline{SCK}_1$, $\overline{SCK}_2$	0.4	—	—	t_{Scyc}		1, 2
Output transmit clock low width	t_{SCKL}	$\overline{SCK}_1$, $\overline{SCK}_2$	0.4	—	—	t_{Scyc}		1, 2
Output transmit clock rise time	t_{SCKr}	$\overline{SCK}_1$, $\overline{SCK}_2$	—	—	40	ns		1, 2
Output transmit clock fall time	t_{SCKf}	$\overline{SCK}_1$, $\overline{SCK}_2$	—	—	40	ns		1, 2
Input transmit clock cycle time	t_{Scyc}	$\overline{SCK}_1$, $\overline{SCK}_2$	2	—	—	t_{cyc}		1
Input transmit clock high width	t_{SCKH}	$\overline{SCK}_1$, $\overline{SCK}_2$	0.4	—	—	t_{Scyc}		1
Input transmit clock low width	t_{SCKL}	$\overline{SCK}_1$, $\overline{SCK}_2$	0.4	—	—	t_{Scyc}		1
Input transmit clock rise time	t_{SCKr}	$\overline{SCK}_1$, $\overline{SCK}_2$	—	—	40	ns		1
Input transmit clock fall time	t_{SCKf}	$\overline{SCK}_1$, $\overline{SCK}_2$	—	—	40	ns		1
Serial output data delay time	t_{DSO}	SO_1, SO_2	—	—	300	ns	Load shown in figure 74	1, 2
Serial input data setup time	t_{SSI}	SI_1, SI_2	100	—	—	ns		1
Serial input data hold time	t_{HSI}	SI_1, SI_2	200	—	—	ns		1

Notes: 1. Refer to figure 73.
2. Refer to figure 74.

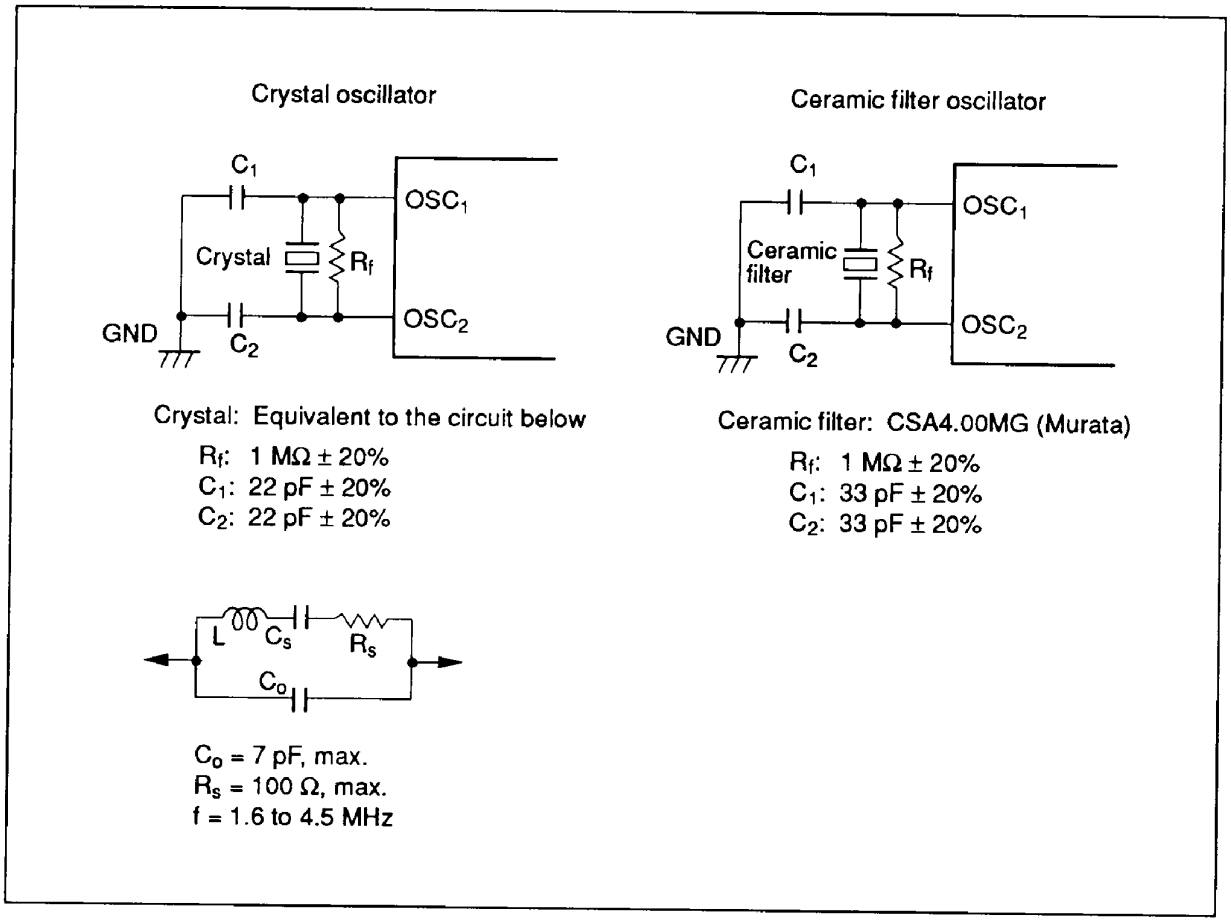


Figure 68 Oscillation Circuits (1)

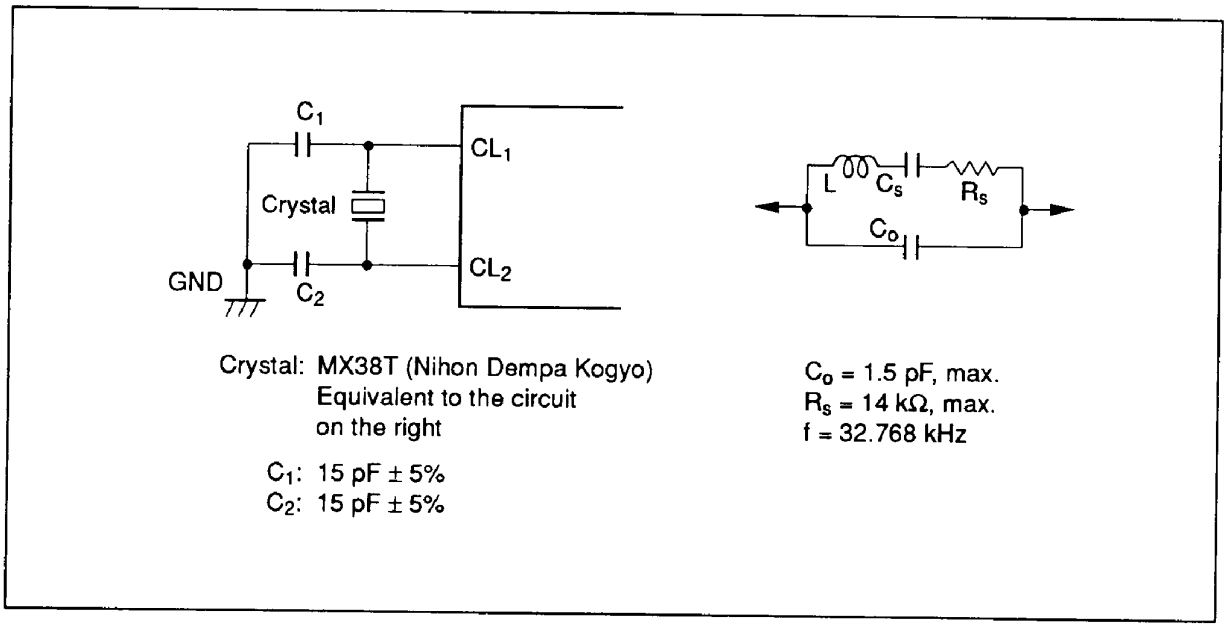


Figure 69 Oscillation Circuits (2)

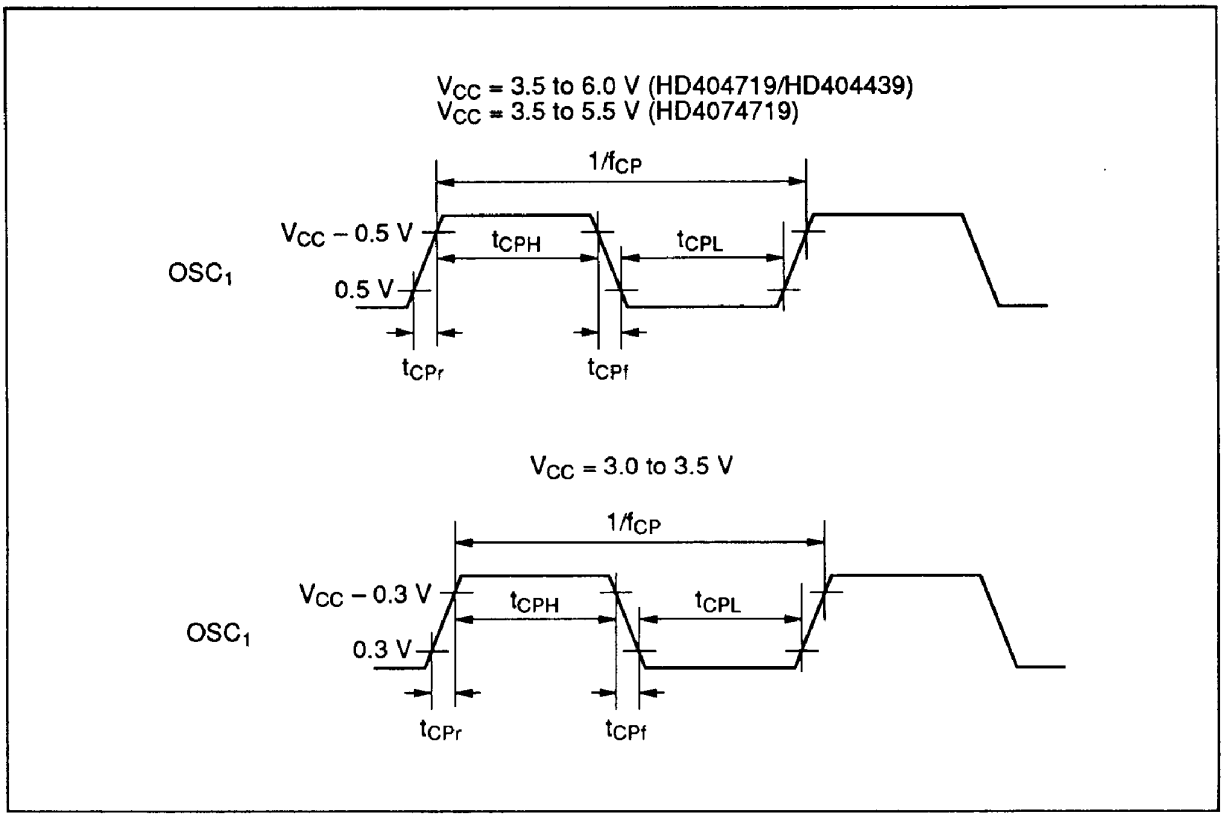


Figure 70 Oscillator Waveforms

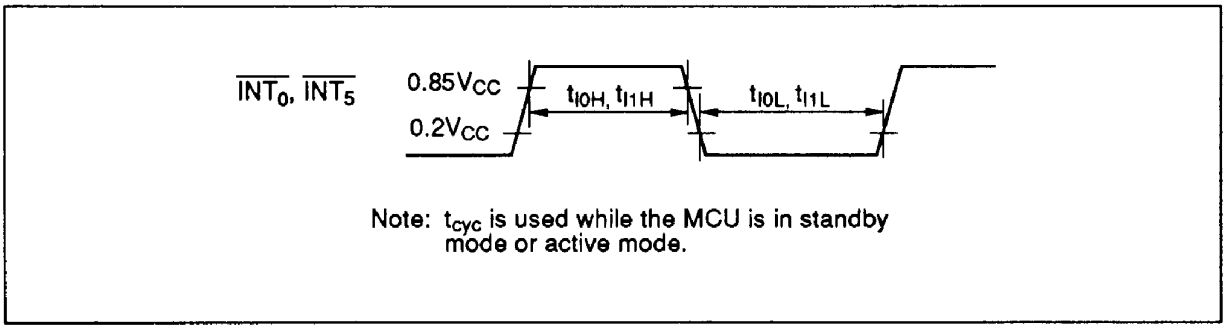


Figure 71 Interrupt Timing

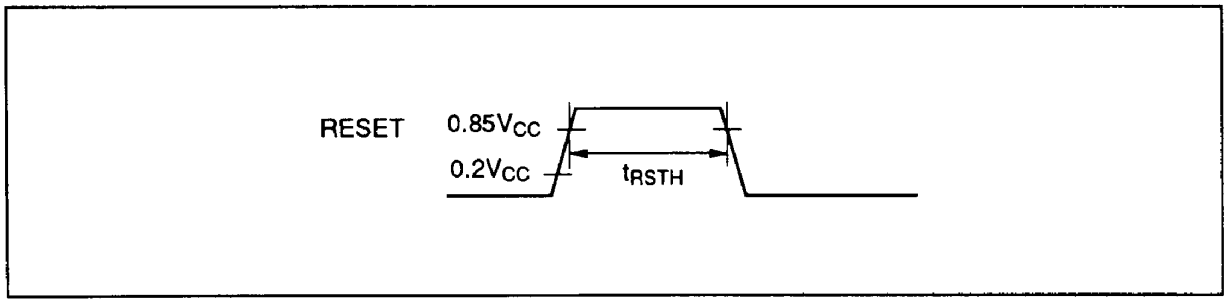
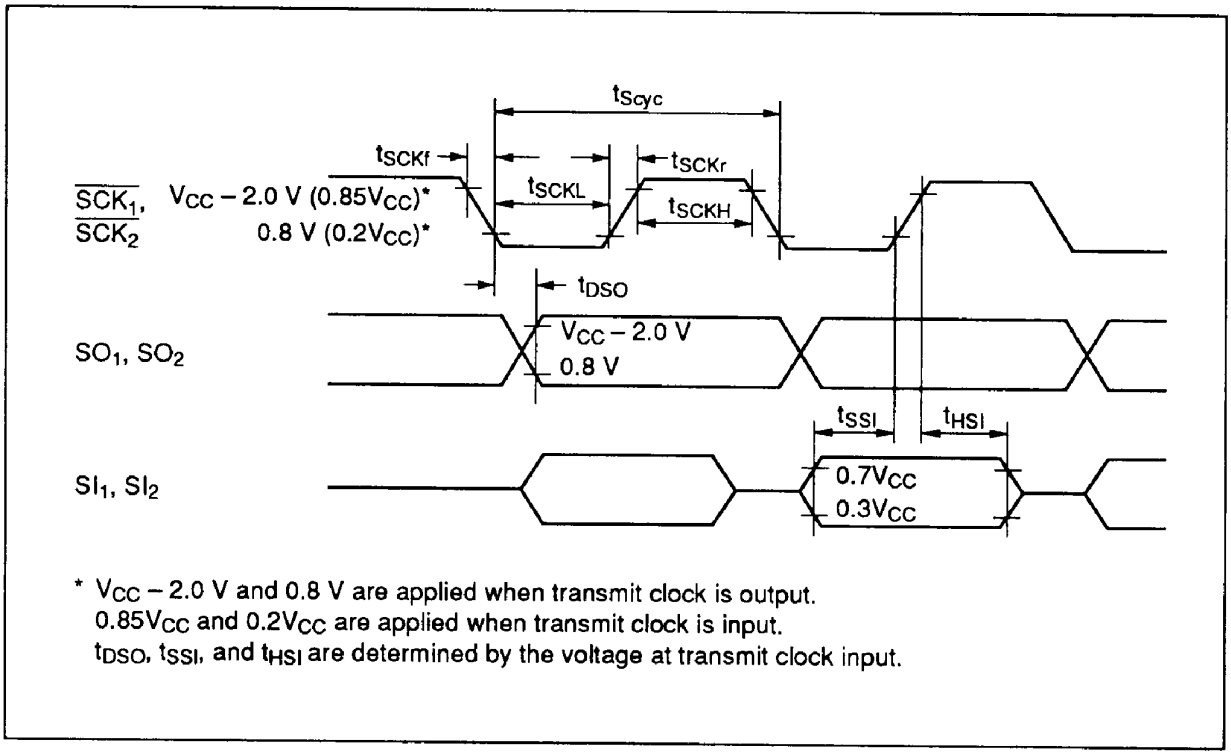


Figure 72 Reset Timing



* V_{CC} – 2.0 V and 0.8 V are applied when transmit clock is output.
0.85V_{CC} and 0.2V_{CC} are applied when transmit clock is input.
t_{DSO}, t_{SSI}, and t_{HSI} are determined by the voltage at transmit clock input.

Figure 73 Serial Interface Timing

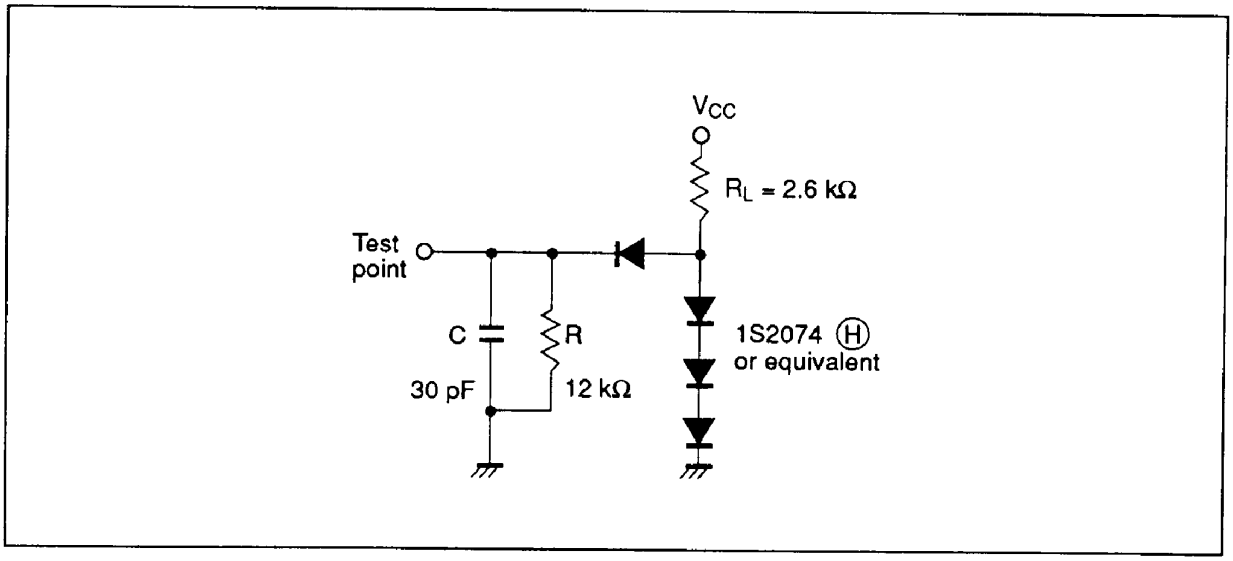


Figure 74 Load Circuit for Timing Measurement

HD404719 Option List

Order date	
Customer name	
Department	
Name	
ROM code	
LSI type	HD404719

* Please check off applicable items by ■, ×, or ✓ within ☐.

1. Package and Storage Tray Types

☐ FP-80A	☐ Hard tray
☐ FP-80B	☐ Soft tray

For other tray types, contact Hitachi's business department.

2. Optional Functions

☐ 32-kHz CPU operation
☐ No 32-kHz CPU operation with clock time-base
☐ No 32-kHz CPU operation, no clock time-base

3. ZTAT™ Compatibility

☐ I/O circuit compatibility with the HD4074719
☐ No I/O circuit compatibility with the HD4074719

Note: ZTAT™ compatibility is enabled only when all pins have C- or D-type circuits. In this case do not use checklist 5.

4. ROM Media

☐ EPROM: Emulator type
☐ HD4074719

5. I/O Options (shaded options are not available)

Pin name	I/O	I/O option B	C	D	E
D_0	I/O				
D_1	I/O				
D_2	I/O				
D_3	I/O				
D_4	I/O				
D_5	I/O				
D_6	I/O				
D_7	I/O				
D_8	I/O				
D_9	I/O				
D_{10}	I/O				
D_{11}	I/O				
D_{12}	I/O				
D_{13}	I/O				
D_{14}	I/O				
D_{15}	I/O				
R0 $R0_0$	I/O				
R0 $R0_1$	I/O				
R0 $R0_2$	I/O				
R0 $R0_3$	I/O				
R1 $R1_0$	I/O				
R1 $R1_1$	I/O				
R1 $R1_2$	I/O				
R1 $R1_3$	I/O				
R2 $R2_0$	I/O				
R2 $R2_1$	I/O				
R2 $R2_2$	I/O				
R2 $R2_3$	I/O				
R3 $R3_0$	I/O				
R3 $R3_1$	I/O				
R3 $R3_2$	I/O				
R3 $R3_3$	I/O				

(High-voltage pins)

Pin name	I/O	I/O option B	C	D	E
R4 $R4_0$	I/O				
R4 $R4_1$	I/O				
R4 $R4_2$	I/O				
R4 $R4_3$	I/O				
R5 $R5_0$	I	Checklist 6			
R5 $R5_1$	I				
R5 $R5_2$	I				
R5 $R5_3$	I				
R6 *1 $R6_0$	I/O				
R6 *1 $R6_1$	I/O				
R6 *1 $R6_2$	I/O				
R6 *1 $R6_3$	I/O				
R7 $R7_0$	I/O				
R7 $R7_1$	I/O				
R7 $R7_2$	I/O				
R7 $R7_3$	I/O				
R8 $R8_0$	I/O				
R8 $R8_1$	I/O				
R8 $R8_2$	I/O				
R8 $R8_3$	I/O				
R9 $R9_0$	I/O				
R9 $R9_1$	I/O				
R9 $R9_2$	I/O				
R9 $R9_3$	I/O				
RA RA_0	I/O				
RA RA_1	I/O				
RA RA_2	I/O				
RA RA_3	I/O				
RB RB_0	I/O				
RB RB_1	I/O				
RC *2 RC_0	I				
RC *2 RC_1	I				

(Standard pins)

Pin name	I/O	I/O option B	C	D	E
RC *2 RC_2	I				
RC *2 RC_3	I				
RD *2 RD_0	I				
RD *2 RD_1	I				
RD *2 RD_2	I				
RD *2 RD_3	I				

(Standard pins)

Check the I/O option required.
B: With pull-up MOS
C: Without pull-up MOS
D: Without pull-down MOS
E: With pull-down MOS

Notes: *1. When using the comparator, do not select B-type circuits for the $R6_0$/COMP and $R6_1/V_{ref}$ pins.
*2. When using the RC and RD pins as analog input pins, do not select B-type circuits.

6. $R5_0/V_{disp}$

☐ $R5_0$: Without pull-down MOS (D)
☐ V_{disp}

Note: $R5_0/V_{disp}$ must be selected as the V_{disp} pin, except when all high-voltage pins are option D.

7. OSC_1 and OSC_2 Oscillator

☐ Ceramic oscillator	f =	MHz
☐ Crystal	f =	MHz
☐ External clock	f =	MHz

8. CL_1 and CL_2 Oscillator

☐ Not used	—
☐ Crystal	f = 32.768 kHz

HD404439 Option List

Order date	
Customer name	
Department	
Name	
ROM code	
LSI type	HD404439

* Please check off applicable items by ■, ×, or ✓ within □.

1. Package and Storage Tray Types

□ FP-80A	□ Hard tray
□ FP-80B	□ Soft tray

For other tray types, contact Hitachi's business department.

2. Optional Functions

□ 32-kHz CPU operation
□ No 32-kHz CPU operation with clock time-base
□ No 32-kHz CPU operation, no clock time-base

3. ZTAT™ Compatibility

□ I/O circuit compatibility with the HD4074719
□ No I/O circuit compatibility with the HD4074719

Note: ZTAT™ compatibility is enabled only when all pins have C- or D-type circuits. In this case do not use checklist 5.

4. ROM Media

□ EPROM: Emulator type
□ HD4074719

5. I/O Options (shaded options are not available)

Pin name		I/O	I/O option B	C	D	E
D_0		I/O				
D_1		I/O				
D_2		I/O				
D_3		I/O				
D_4		I/O				
D_5		I/O				
D_6		I/O				
D_7		I/O				
D_8		I/O				
D_9		I/O				
D_{10}		I/O				
D_{11}		I/O				
D_{12}		I/O				
D_{13}		I/O				
D_{14}		I/O				
D_{15}		I/O				
R0	$R0_0$	I/O				
	$R0_1$	I/O				
	$R0_2$	I/O				
	$R0_3$	I/O				
R1	$R1_0$	I/O				
	$R1_1$	I/O				
	$R1_2$	I/O				
	$R1_3$	I/O				
R2	$R2_0$	I/O				
	$R2_1$	I/O				
	$R2_2$	I/O				
	$R2_3$	I/O				
R3	$R3_0$	I/O				
	$R3_1$	I/O				
	$R3_2$	I/O				
	$R3_3$	I/O				

Open-drain PMOS pins

Pin name		I/O	I/O option B	C	D	E
R4	$R4_0$	I/O				
	$R4_1$	I/O				
	$R4_2$	I/O				
	$R4_3$	I/O				
R5	$R5_0$	I				
	$R5_1$	I				
	$R5_2$	I				
	$R5_3$	I				
R6 *1	$R6_0$	I/O				
	$R6_1$	I/O				
	$R6_2$	I/O				
	$R6_3$	I/O				
R7	$R7_0$	I/O				
	$R7_1$	I/O				
	$R7_2$	I/O				
	$R7_3$	I/O				
R8	$R8_0$	I/O				
	$R8_1$	I/O				
	$R8_2$	I/O				
	$R8_3$	I/O				
R9	$R9_0$	I/O				
	$R9_1$	I/O				
	$R9_2$	I/O				
	$R9_3$	I/O				
RA	RA_0	I/O				
	RA_1	I/O				
	RA_2	I/O				
	RA_3	I/O				
RB	RB_0	I/O				
	RB_1	I/O				
RC *2	RC_0	I				
	RC_1	I				

Standard pins

Pin name		I/O	I/O option B	C	D	E
RC *2	RC_2	I				
	RC_3	I				
RD *2	RD_0	I				
	RD_1	I				
	RD_2	I				
	RD_3	I				

Check the I/O option required.
B: With pull-up MOS
C: Without pull-up MOS
D: Without pull-down MOS
E: With pull-down MOS

Notes: *1. When using the comparator, do not select B-type circuits for the $R6_0$/COMP and $R6_1/V_{ref}$ pins.
*2. When using the RC and RD pins as analog input pins, do not select B-type circuits.

6. OSC_1 and OSC_2 Oscillator

□ Ceramic oscillator	f = MHz
□ Crystal	f = MHz
□ External clock	f = MHz

7. CL_1 and CL_2 Oscillator

□ Not used	—
□ Crystal	f = 32.768 kHz