MA007A

3-in-1 8-bit serial to parallel latch

Features

- Three 8-bit serial input
- Three 8-bit parallel output
- Operation voltage: 2.0V to 5.7V
- Storage register with 3-state outputs
- Shift register with direct clear
- 5 MHz (typical) shift out frequency
- Output capability:
  - Parallel outputs; bus driver
  - Serial output; standard

Selection Information

	MA007AH	MA007AP	MA007AD	MA007AF
Package / Dice	Dice	44-PLCC	48-LQFP	44-PQFP
Parallel Output	24 pins			
Sink Current	20mA			

Application Field

Serial-to-parallel data conversion

Remote control holding register

2005/11 version A1

MEGAWIN

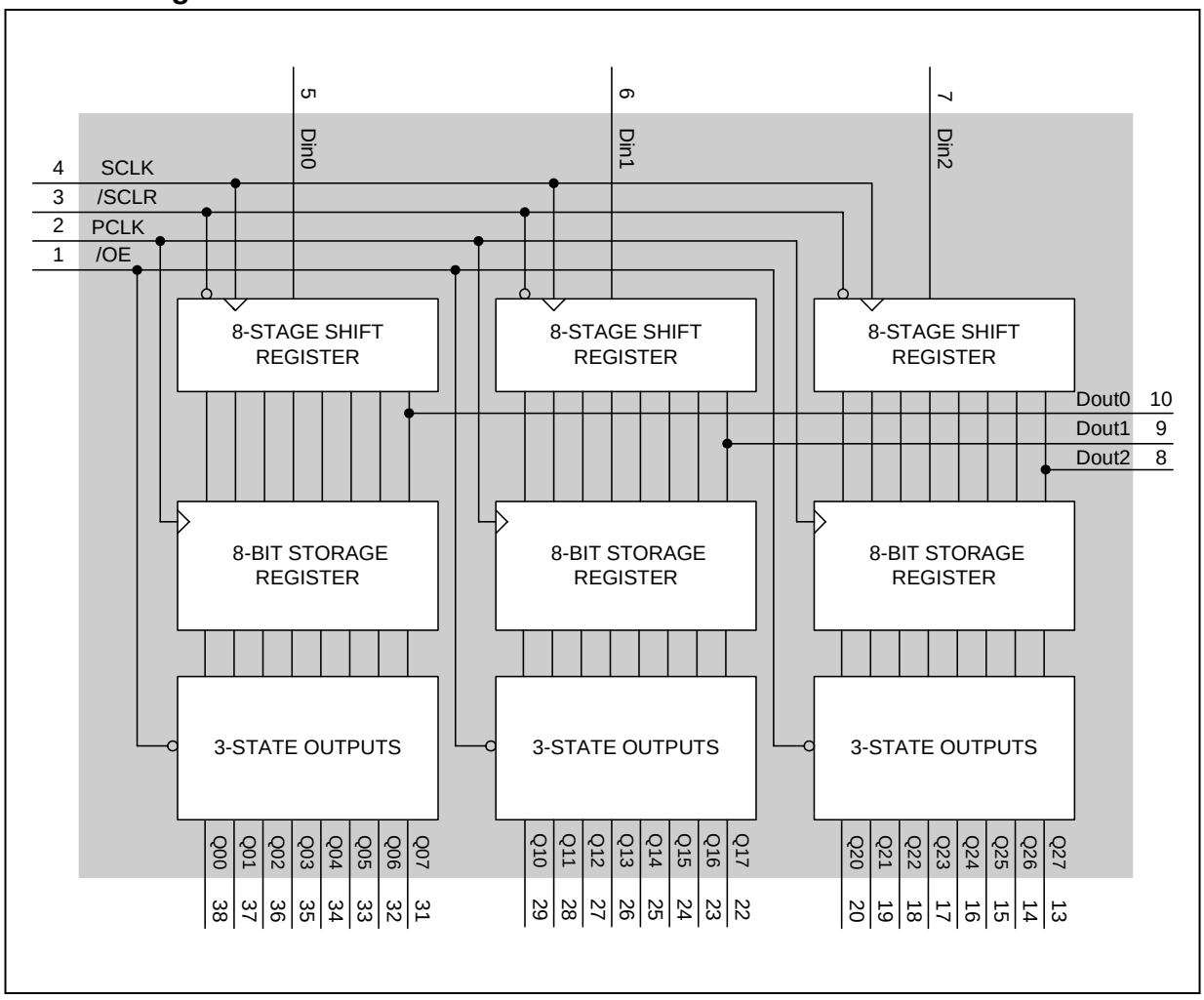
General Description

The MA007 are high-speed Si-gate CMOS devices. There are three groups 8-stage serial shift register with a storage register and 3-state outputs in MA007. The shift register and storage register have separate clocks. Data is shifted on the positive-going transitions of the SCLK input. The data in each register is transferred to the storage register on a positive-going transition of the PCLK input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register. The shift register has a serial input (D_{INx}) and a serial standard output (D_{OUTx}) for cascading. It is also provided with asynchronous reset (active LOW) for all 8 stages shift register. The storage register has 8 parallel 3-state bus driver outputs. Data in the storage register appears at the output whenever the output enable input (/OE) is LOW.

Pad Description

Pad No.	Pad Name	I/O	Description
1	/OE	I	Output enable (active LOW)
2	PCLK	I	Parallel register clock input
3	/SCLR	I	Serial register reset (active LOW)
4	SCLK	I	Shift register clock input
5, 6, 7	D_{IN0}, D_{IN1}, D_{IN2}	I	Serial data input
10, 9, 8	D_{OUT0}, D_{OUT1}, D_{OUT2}	O	Serial data output
20 to 13	Q_{20} to Q_{27}	O	Parallel data group 2 output
29 to 22	Q_{10} to Q_{17}	O	Parallel data group 1 output
38 to 31	Q_{00} to Q_{07}	O	Parallel data group 0 output
12, 30, 40	V_{CC}	P	Positive supply voltage
11, 21, 39, 41	GND	P	Power ground (0 V)

Block Diagram



Function Description

FUNCTION TABLE

INPUTS					OUTPUTS		FUNCTON
SCLK	PCLK	/OE	/SCLR	D_{INx}	D_{OUTx}	Q_{xN}	
X	X	L	L	X	L	NC	A LOW level on /SCLR only affects the shift registers
X	↑	L	L	X	L	L	Empty shift register loaded into storage register
X	X	H	L	X	L	Z	Shift register clear. Parallel outputs in high-impedance OFF-state
↑	X	L	H	H	Qx6'	NC	Logic high level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Qx6') appears on the serial output (D_{OUTx})
X	↑	L	H	X	NC	Qxn'	Contents of shift register stages (internal Qxn') are transferred to the storage register and parallel output stages
↑	↑	L	H	X	Qx6'	Qxn'	Contents of shift register shifted through. Previous contents of the shift register are transferred to the storage register and the parallel output stages.

Notes

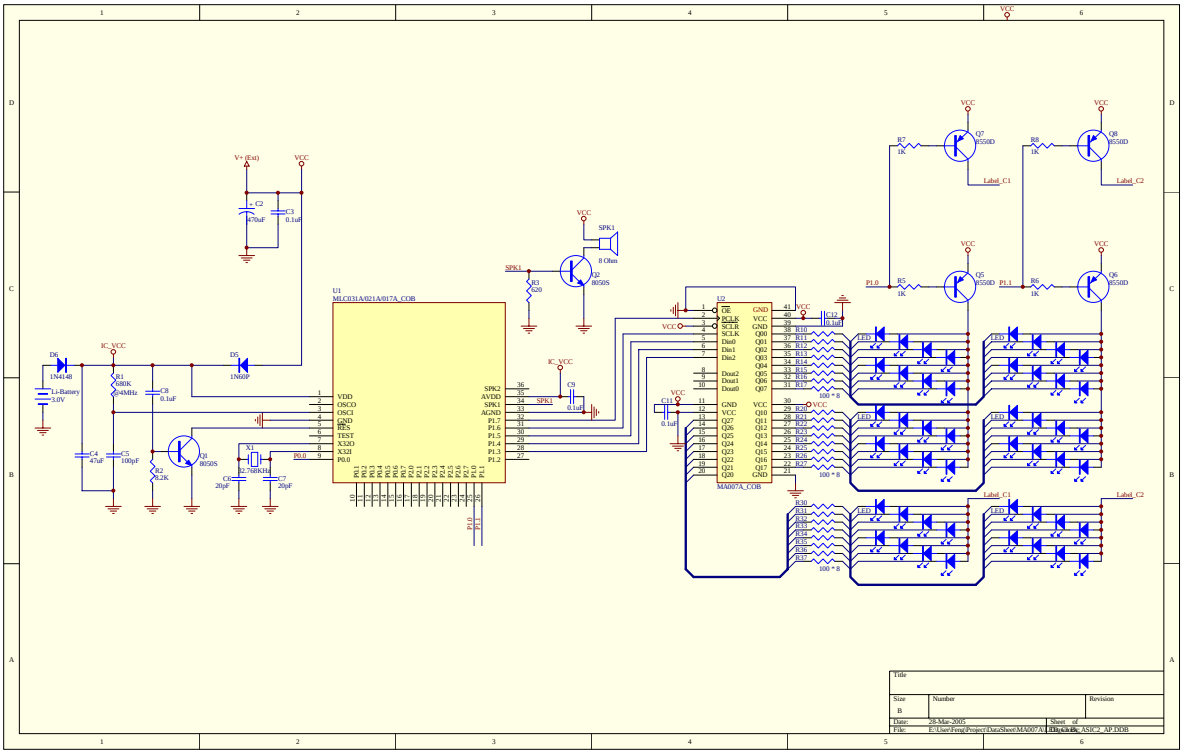
H = HIGH voltage level; L = LOW voltage level

↑ = LOW-to-HIGH transition; ↓ = HIGH-to-LOW

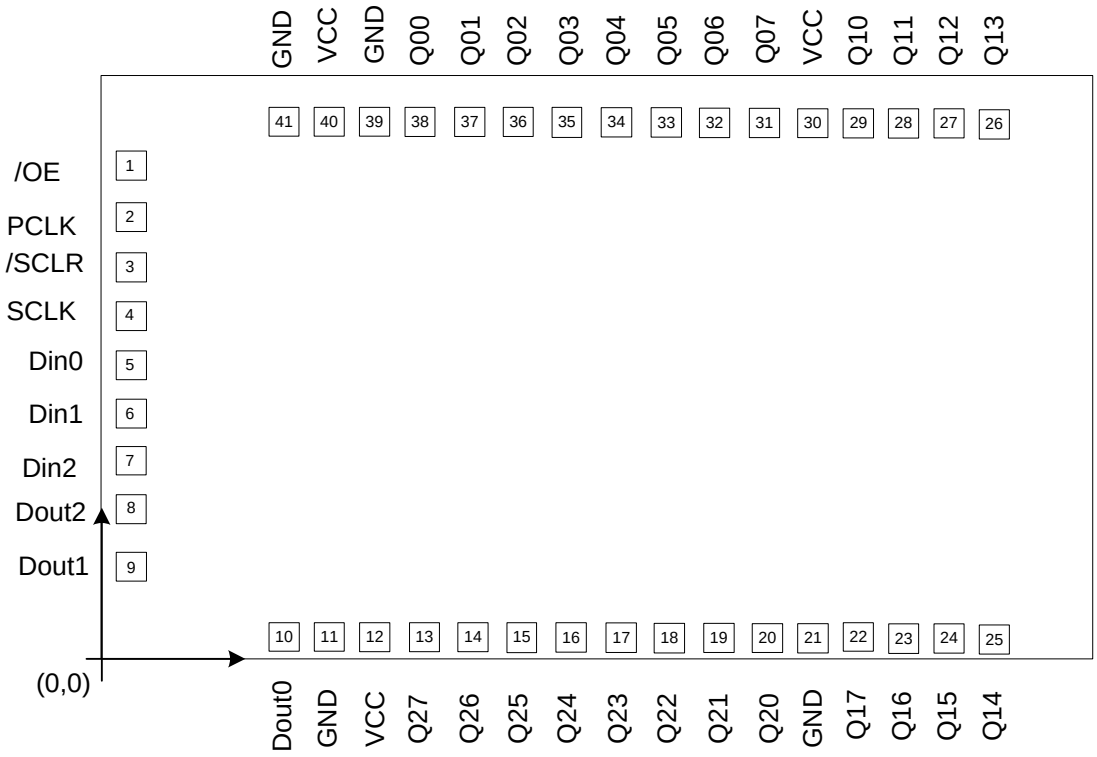
Z = high-impedance OFF-state; NC = no change

X = don't care.

Application Circuit



Pad Assignment



Absolute Maximum Rating

PARAMETER	RATING	UNIT
Supply Voltage to Ground Potential	-0.3 to +6.0	V
Applied Input / Output Voltage	-0.3 to +6.0	V
Power Dissipation	500	mW
Ambient Operating Temperature	0 to +70	°C
Storage Temperature	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC Characteristics

(V_{CC}-GND = 5.0V, Ta = 25° C; unless otherwise specified)

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Op. Voltage	V_{CC}	-	2.0	5.0	6.0	V
Op. Current	I_{OP}	No load (Ext.-V)	-	4.0	16.0	μA
Input High Voltage	V_{IH}	-	0.7 V_{DD}	-	V_{DD}	V
Input Low Voltage	V_{IL}	-	0	-	0.3V_{DD}	V
D_{OUTx} sink current	I_{OL0}	V_{OL} = 0.4V	-	3.0	4.5	mA
D_{OUTx} drive current	I_{OH0}	V_{OH} = 4.5V	-	1.5	2.5	mA
Q_{x0} to Q_{x7} sink current	I_{OL1}	V_{OL} = 0.4V	-	18	27	mA
		V_{OL} = 0.4V, V_{CC} = 6.0V	-	20	32	mA
Q_{x0} to Q_{x7} drive current	I_{OH1}	V_{OH} = 4.5V	-	2.7	3.5	mA
		V_{OH} = 5.4V, V_{CC} = 6.0V	-	3.0	5.0	mA
All output sink current	I_{OL2}	V_{OL} = 0.4V	-	16	24	mA
All output drive current	I_{OH2}	V_{OH} = 4.5V	-	8	12	mA
Total output sink current	I_{OL3}	V_{OL} = 0.4V	-	384	576	mA
Total output drive current	I_{OH3}	V_{OH} = 4.5V	-	192	288	mA

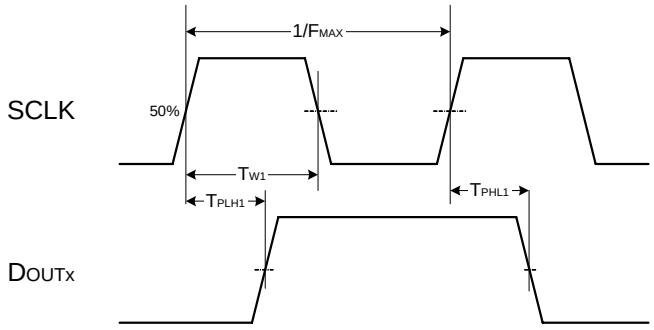
AC Characteristics

(VCC-GND = 5.0V, Ta = 25° C; unless otherwise specified)

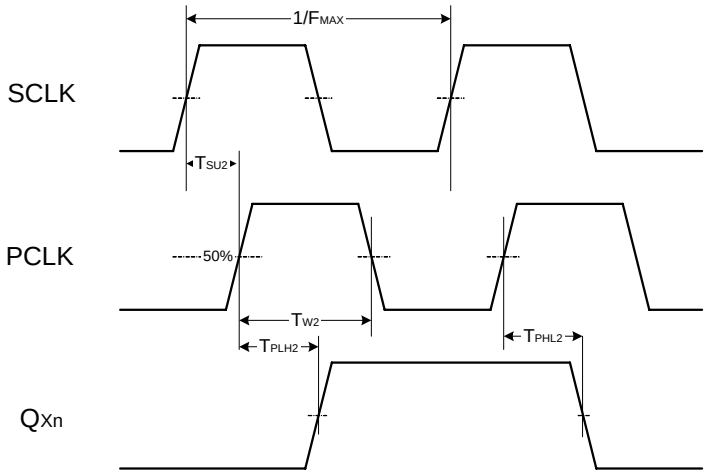
PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Maximum clock pulse frequency (SCLK, PCLK)	F_{MAX}	50 % duty cycle	-	2.5	5	MHz
Propagation delay	T_{PHL1} T_{PLH1}	SCLK to D_{OUTx}, C_L = 15 pF	-	95	195	nS
	T_{PHL2} T_{PLH2}	PCLK to Q_{Xn}, C_L = 15 pF	-	100	200	nS
	T_{PHL3}	/SCLR to D_{OUTx}, C_L = 15 pF	-	100	200	nS
Setup Time	T_{SU1}	Din to SCLK	10	-	-	nS
	T_{SU2}	SCLK to PCLK	100	-	-	nS
	T_{SU3}	SCLK to PCLK	-	5	10	nS
Pulse Width	T_{W1}	SCLK	25	-	-	nS
	T_{W2}	PCLK	25	-	-	nS
	T_{W3}	/SCLR	25	-	-	nS
Tri-state output enable time	T_{PZH} T_{PZL}	/OE to Q_{Xn}	-	100	200	nS
Tri-state output disable time	T_{PHZ} T_{PLZ}	/OE to Q_{Xn}	-	100	200	nS
Hold time	T_H	Din to SCLK	5	-	-	nS
Removal time	T_{REM}	/SCLR to SCLK	10	-	-	nS

System Timing

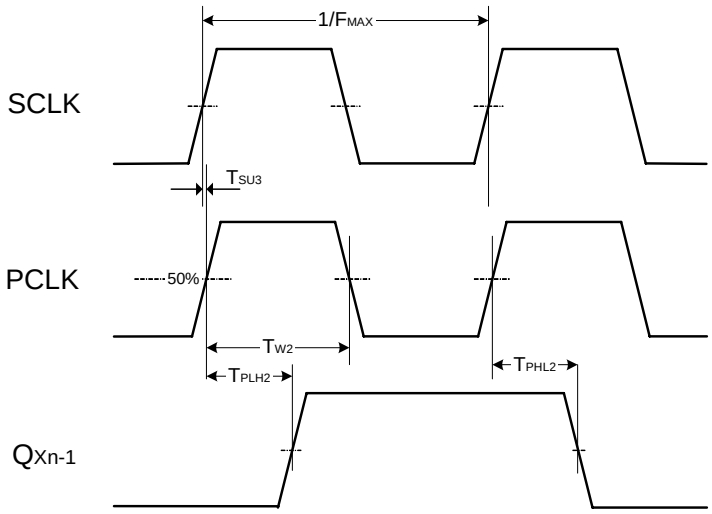
SCLK to DOUTx Propagation Delay Waveforms



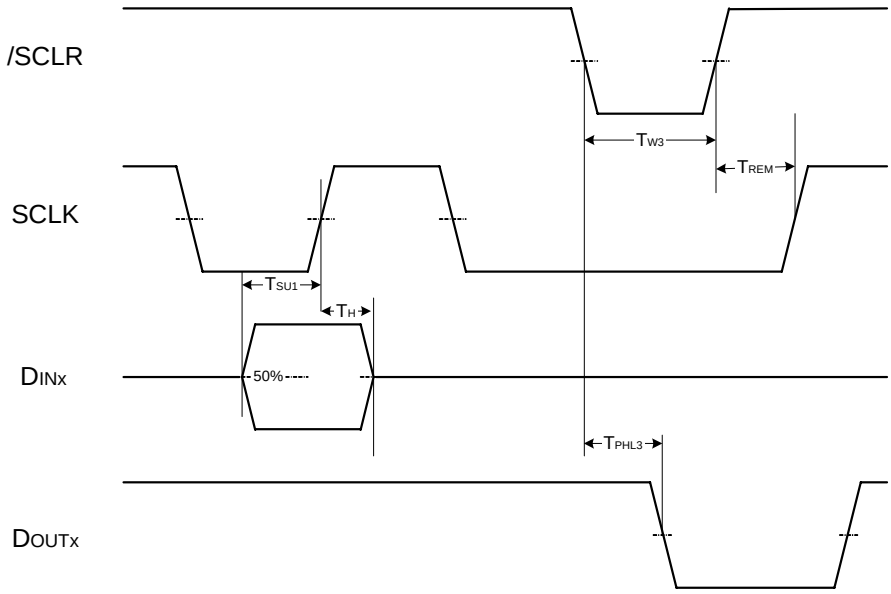
PCLK to QXn Propagation Delay and Setup Time Waveforms



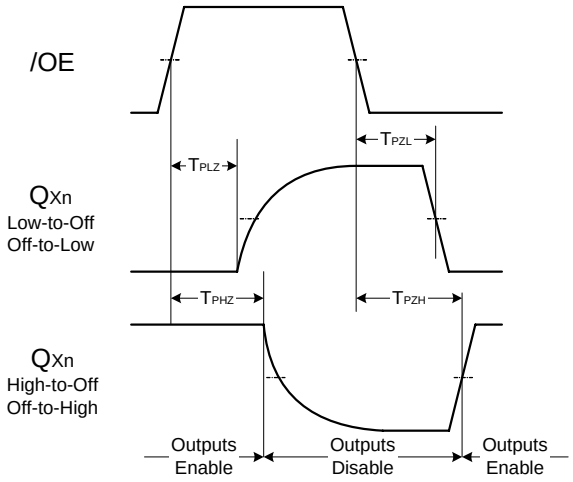
SCLK and PCLK are connected together to Q_{Xn-1} Propagation Delay and Setup Time Waveforms



PCLK to Q_{Xn} Propagation Delay and Setup Time Waveforms

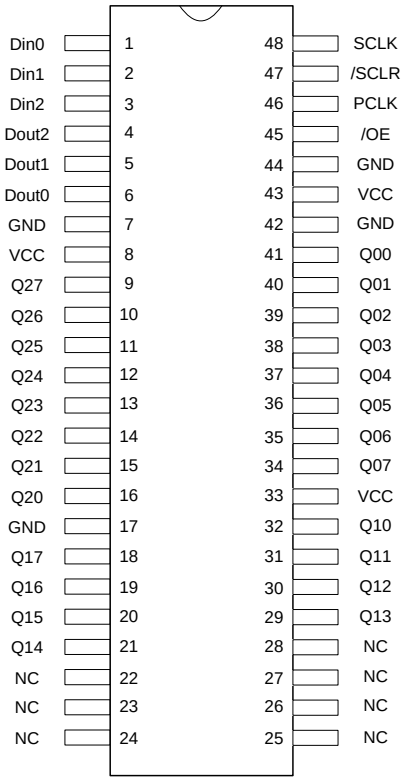


Tri-state Enable/Disable Time Waveforms



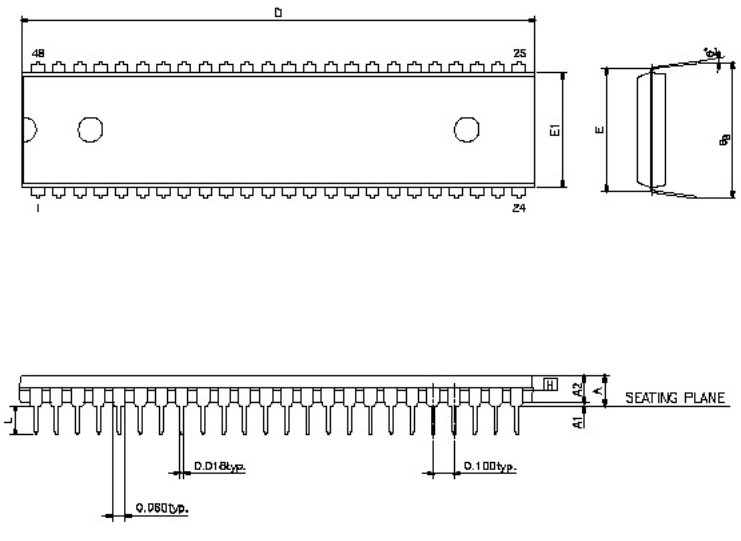
Package Information

MA007AE 48 Pin PDIP (600mil) Configuration



48-PDIP (600 mil)

48 Pin PDIP Package Dimension

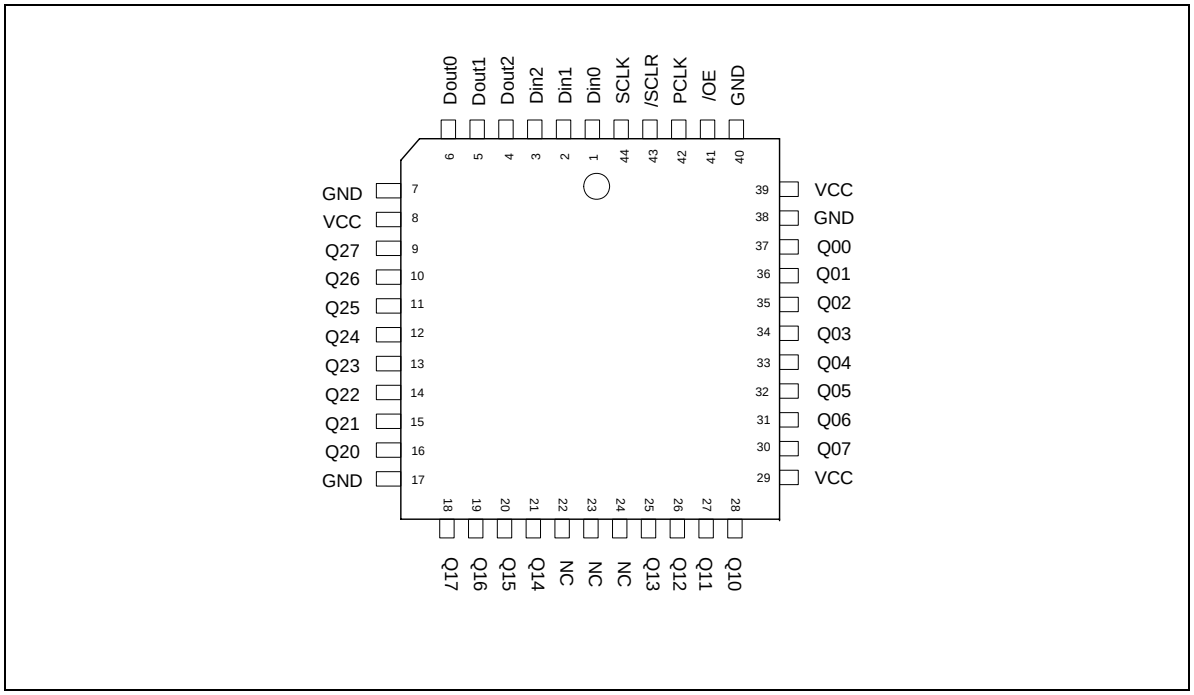


SYMBOLS	MIN.	NOR.	MAX.
A	–	–	0.220
A1	0.015	–	–
A2	0.150	0.155	0.160
D	2.400	2.450	2.550
E		0.600 BSC	
E1	0.540	0.545	0.550
L	0.115	0.130	0.150
e_B	0.630	0.650	0.670
θ°	0	7	15

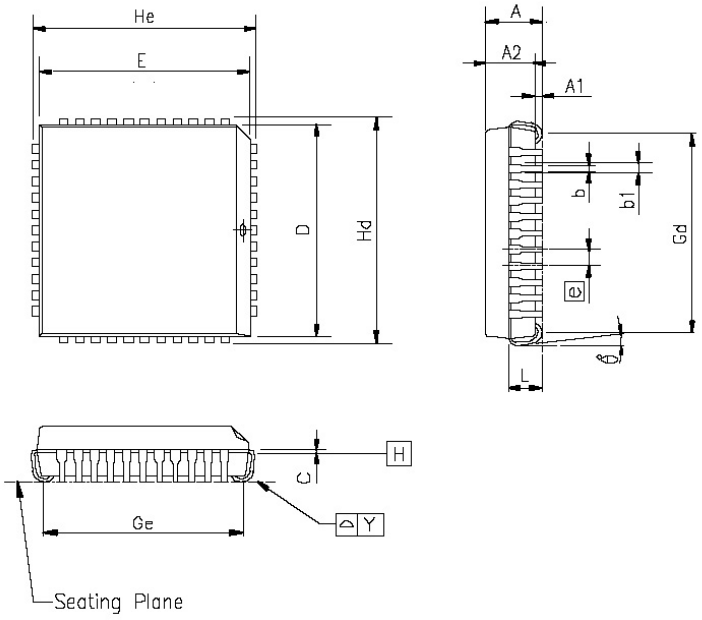
UNIT : INCH

NOTE:
1.JEDEC OUTLINE : MS-011 AD

MA007AP 44 Pin PLCC Configuration



44 Pin PLCC Package Dimension



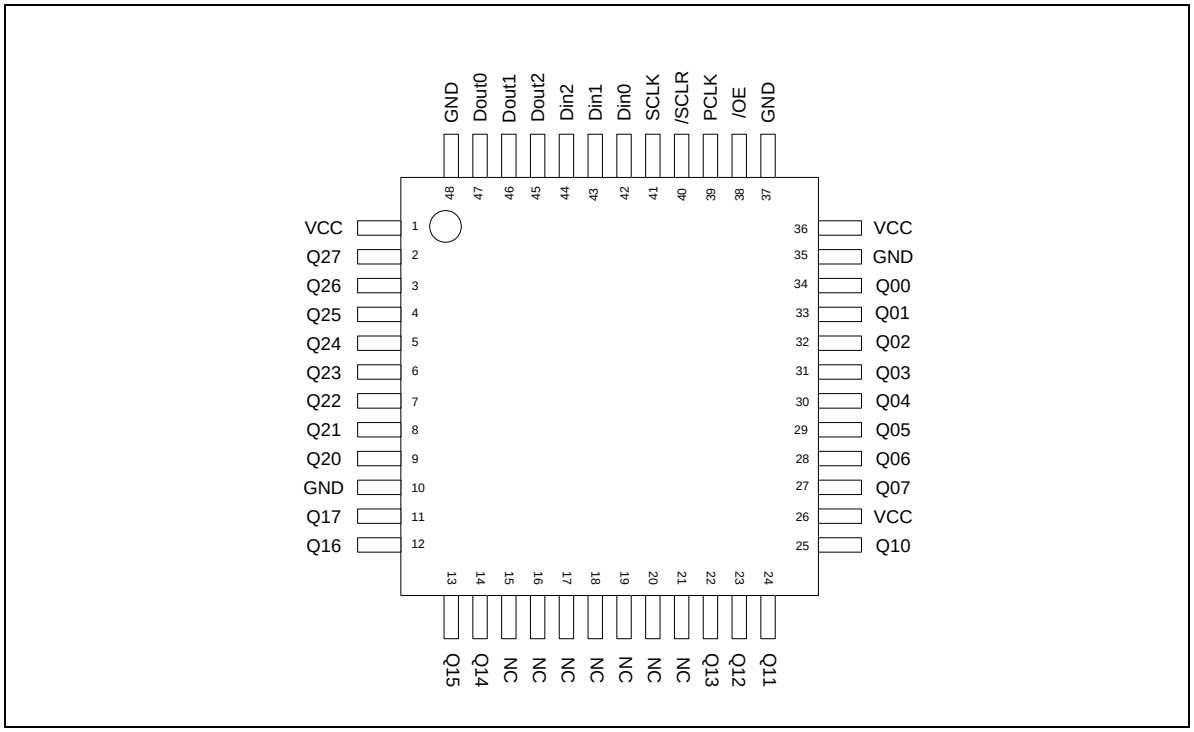
SYMBOLS	MIN.	NOM.	MAX.
A	–	–	0.185
A1	0.020	–	–
A2	0.145	0.150	0.155
b1	0.026	0.028	0.032
b	0.016	0.018	0.022
c	0.007	0.010	0.013
D	0.648	0.653	0.658
E	0.648	0.653	0.658
e		0.050 BSC	
Gd	0.590	0.610	0.630
Ge	0.590	0.610	0.630
Hd	0.680	0.690	0.700
He	0.680	0.690	0.700
L	0.090	0.100	0.110
Y	–	–	0.004

UNIT : INCH

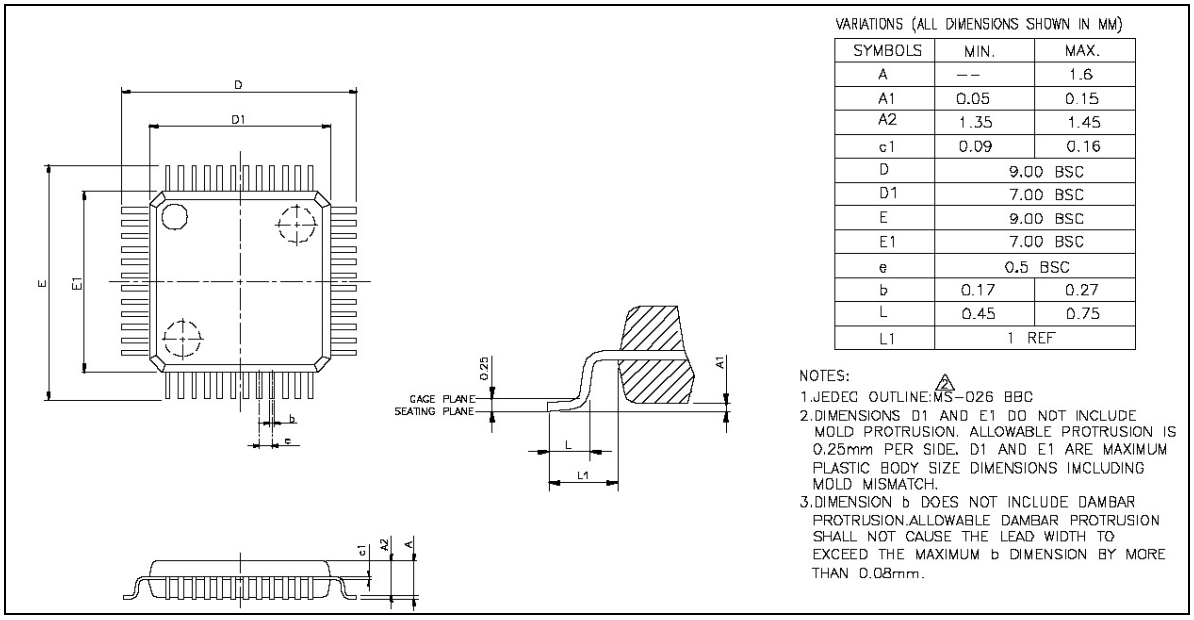
* ***NOTE:***

1. JEDEC OUTLINE : MO-047 AC
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DIMENSIONS E AND D DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 10 MIL PER SIDE. DIMENSIONS E AND D DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
4. DIMENSION b1 DOES NOT INCLUDE DAMBAR PROTRUSION .

MA007AD 48 Pin LQFP Configuration



48 Pin LQFP Package Dimension

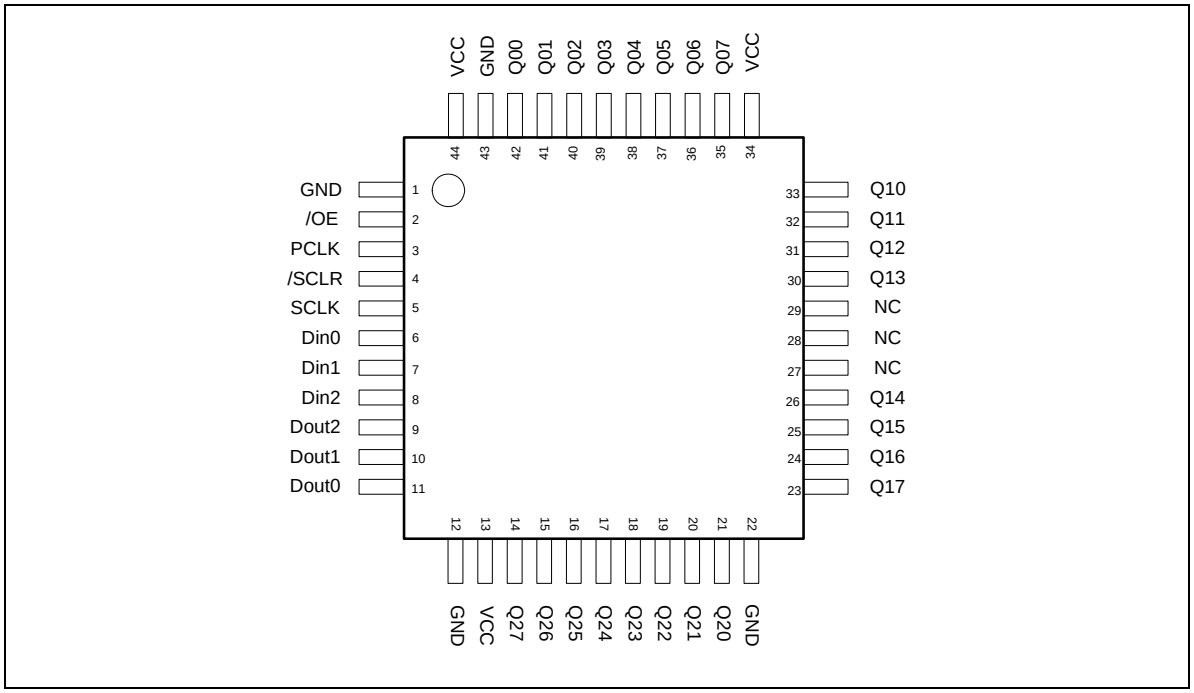


VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

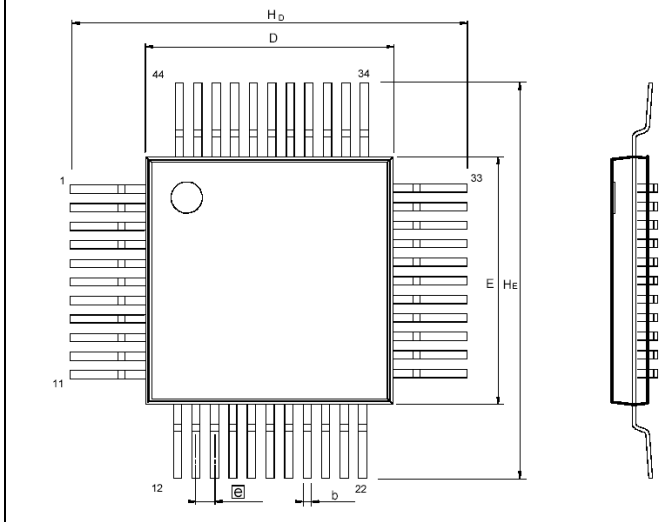
SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.5 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	

NOTES:
1. JEDEC OUTLINE: MS-026 BBC
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

MA007AF 44 Pin PQFP Configuration



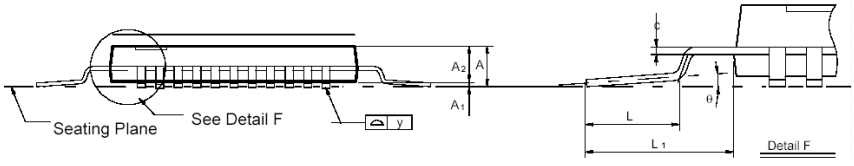
44 Pin PQFP Package Dimension



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	---	---	---	---
A_1	0.002	0.01	0.02	0.05	0.25	0.5
A_2	0.075	0.081	0.087	1.90	2.05	2.20
b	0.01	0.014	0.018	0.25	0.35	0.45
c	0.004	0.006	0.010	0.101	0.152	0.254
D	0.390	0.394	0.398	9.9	10.00	10.1
E	0.390	0.394	0.398	9.9	10.00	10.1
e	0.025	0.031	0.036	0.635	0.80	0.952
H_D	0.510	0.520	0.530	12.95	13.2	13.45
H_E	0.510	0.520	0.530	12.95	13.2	13.45
L	0.025	0.031	0.037	0.65	0.8	0.95
L_1	0.051	0.063	0.075	1.295	1.6	1.905
y	—	—	0.003	—	—	0.08
θ	0°	—	7°	0°	—	7°

Notes:

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.



Notes:

Vision History

VERSION	DATE	PAGE	DESCRIPTION
A1	Nov. 2005		Initial issue.