Contents

CMOS SERIAL E^2PROM

S-29LX94A Series

The S-29LX94A Series is low power 1K/2K/4K-bit serial E^2PROMs with a low operating voltage range. They are organized as 64-word × 16-bit, 128-word × 16-bit and 256-word × 16-bit, respectively. Each is capable of sequential read, where addresses are automatically incremented in 16-bit blocks.
The S-29LX94A Series is capable of protecting the memory, 50% of which can be protected starting from address 00.

Interface is structured so that this IC can be directly connected to the CPU with serial ports. 8-bit instructions make it easy to prepare your own software.

■ Features

- Low power consumption
  Standby : 0.8 μA Max. (V_{CC} = 5.5 V)
  Operating : 0.8 mA Max. (V_{CC} = 5.5 V)
  0.4 mA Max. (V_{CC} = 2.7 V)
- Low operating voltage range
  Write : 1.8 to 5.5 V
  Read : 1.8 to 5.5 V
- Sequential read capable
- Memory Protection
- Can be easily connected to the serial port
- CS Active "L"
- Endurance : 10^5 cycles/word
- Data retention : 10 years
- S-29L194A : 1 Kbits
- S-29L294A : 2 Kbits
- S-29L394A : 4 Kbits

■ Pin Assignment

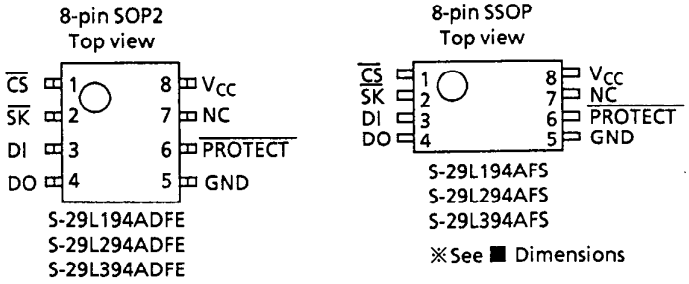


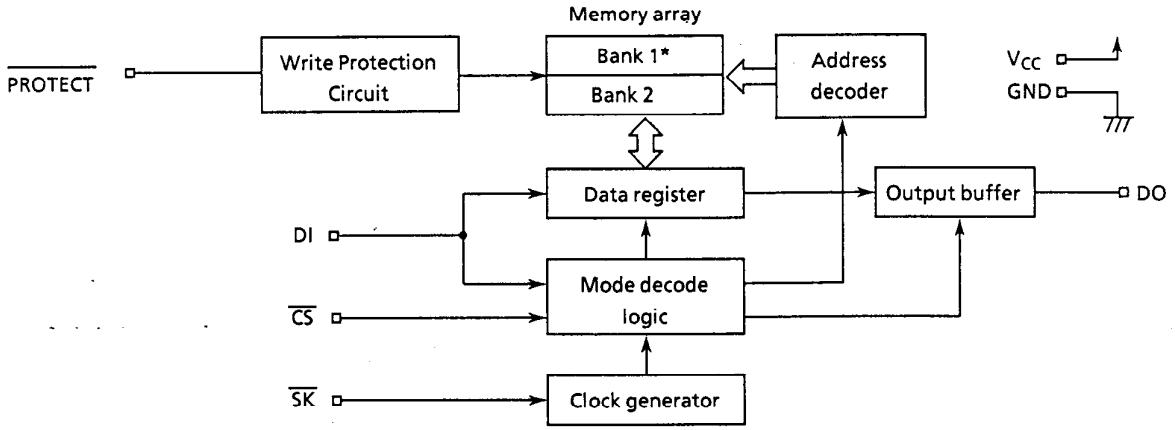
Figure 1

■ Pin Functions

Table 1

Name	Pin Number		Function
	SOP2	SSOP	
$\overline{CS}$	1	1	Chip select input
$\overline{SK}$	2	2	Serial clock input
DI	3	3	Serial data input
DO	4	4	Serial data output
GND	5	5	Ground
$\overline{PROTECT}$	6	6	Memory Protection Control Input Connected to GND or Open : Protection Valid Connected to Vcc : Protection Invalid
NC	7	7	No Connection
V_{CC}	8	8	Power supply

■ Block Diagram



* 50% of the memory can be protected starting from address 00.

Figure 2

■ Instruction Set

Table 2

Instruction	Start Bit	Ope code	– Address			Data
			S-29L194A	S-29L294A	S-29L394A	
READ (Read data)	1	1000xxx	xx A5toA0	x A6toA0	A7toA0	D_{15} to D_0 Output*
PROGRAM (Program data)	1	x100xxx	xx A5toA0	x A6toA0	A7toA0	D_{15} to D_0 Input
PEN (Program enable)	1	0011xxx	xxxxxxxx	xxxxxxxx	xxxxxxxx	—
PDS (Program disable)	1	0000xxx	xxxxxxxx	xxxxxxxx	xxxxxxxx	—

x : Doesn't matter.

* : When 16-bit data of the specified address is output, the data of the next address is output.

■ Absolute Maximum Ratings

Table 3

Parameter	Symbol	Ratings	Unit
Power supply voltage	V_{CC}	– 0.3 to + 7.0	V
Input voltage	V_{IN}	– 0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}	– 0.3 to V_{CC}	V
Storage temperature under bias	T_{bias}	– 50 to + 95	°C
Storage temperature	T_{stg}	– 65 to + 150	°C

■ Recommended Operating Conditions

Table 4

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	Read Operation Write Enable/Disable	1.8	—	5.5	V
		Write Operation	1.8	—	5.5	V
High level input voltage	V_{IH}		0.8 × V_{CC}	—	V_{CC}	V
Low level input voltage	V_{IL}		0.0	—	0.2 × V_{CC}	V
Operating temperature	T_{opr}		– 40	—	+ 85	°C

■ Pin Capacitance

Table 5

($Ta = 25°C$, $f = 1.0$ MHz, $V_{CC} = 5$ V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0$ V	—	—	8	pF
Output Capacitance	C_{OUT}	$V_{OUT} = 0$ V	—	—	10	pF

■ Endurance

Table 6

Parameter	Symbol	Min.	Typ.	Max.	Unit
Endurance	N_W	10^5	—	—	cycles/word

■ DC Characteristics

Table 7

Parameter	Smbl	Conditions	$V_{CC} = 4.5$ to 5.5 V			$V_{CC} = 2.7$ to 4.5 V			$V_{CC} = 1.8$ to 2.7 V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Current consumption (READ)	I_{CC1}	DO unloaded	—	—	0.8	—	—	0.6	—	—	0.4	mA
Current consumption (PROGRAM)	I_{CC2}	DO unloaded	—	—	2.0	—	—	1.5	—	—	1.0	mA

Table 8

Parameter	Smbl	Conditions	$V_{CC} = 4.5$ to 5.5 V			$V_{CC} = 2.7$ to 4.5 V			$V_{CC} = 1.8$ to 2.7 V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Standby current consumption	I_{SB}	$\overline{CS} = V_{CC}$ DO = Open Other input: Connected to V_{CC} or GND	—	—	0.8	—	—	0.6	—	—	0.4	μA
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	μA
Output leakage current	I_{LO}	V_{OUT} = GND to V_{CC}	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	μA
Low level output voltage	V_{OL}	$I_{OL} = 2.1$ mA	—	—	0.45							V
		$I_{OL} = 100$ μA	—	—	0.1	—	—	0.1	—	—	0.1	V
High level output voltage	V_{OH}	$I_{OH} = -400$ μA	2.4	—	—							V
		$I_{OH} = -100$ μA	$V_{CC} - 0.7$	—	—	$V_{CC} - 0.7$	—	—				V
		$I_{OH} = -10$ μA	$V_{CC} - 0.7$	—	—	$V_{CC} - 0.7$	—	—	$V_{CC} - 0.3$	—	—	V
Write enable latch data hold voltage	V_{DH}	Only when write disable mode	1.5	—	—	1.5	—	—	1.5	—	—	V
Pull-down current	I_{PD}	$\overline{PROTECT}$ Terminal = V_{CC}	15	—	80	4	—	50	1	—	15	μA

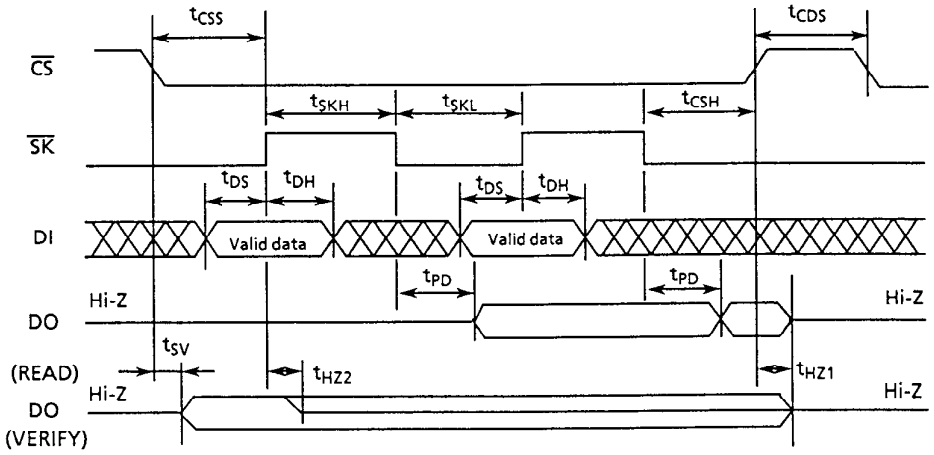
■ AC Characteristics

Table 9 Measuring conditions

Input pulse voltage	$0.1 \times V_{CC}$ to $0.9 \times V_{CC}$
Output reference voltage	$0.5 \times V_{CC}$
Output load	100pF

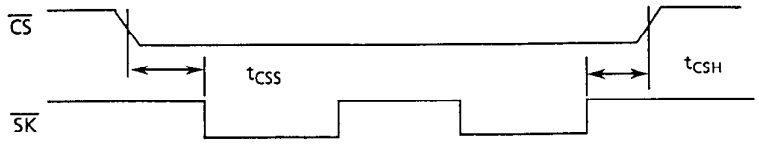
Table 10

Parameter	Smbl	V_{CC} = 4.5 to 5.5V			V_{CC} = 2.7 to 4.5 V			V_{CC} = 1.8 to 2.7V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
CS setup time	t_{CSS}	0.2	—	—	0.4	—	—	1.0	—	—	μs
CS hold time	t_{CSH}	0.2	—	—	0.4	—	—	1.0	—	—	μs
CS deselect time	t_{CDS}	0.2	—	—	0.2	—	—	0.4	—	—	μs
Data setup time	t_{DS}	0.2	—	—	0.4	—	—	0.8	—	—	μs
Data hold time	t_{DH}	0.2	—	—	0.4	—	—	0.8	—	—	μs
Output delay time	t_{PD}	—	—	0.4	—	—	1.0	—	—	2.0	μs
Clock frequency	f_{SK}	0	—	2.0	0	—	0.5	—	—	0.25	MHz
Clock pulse width	t_{SKH} t_{SKL}	0.25	—	—	1.0	—	—	2.0	—	—	μs
Output disable time	t_{HZ1} t_{HZ2}	0	—	0.15	0	—	0.5	0	—	1.0	μs
Output enable time	t_{SV}	0	—	0.15	0	—	0.5	0	—	1.0	μs
Programming time	t_{PR}	—	4.0	10.0	—	4.0	10.0	—	4.0	10.0	ms



Input data is retrieved on the rising edge of $\overline{SK}$.
Output data is triggered on the falling edge of $\overline{SK}$.

Figure3 Timing Chart



Fiure4 Timing Chart for t_{CSS} and t_{CSH} when $\overline{SK}$ is "H"

■ Operation

Instructions (in the order of start-bit, instruction, address, and data) are latched to DI in synchronization with the rising edge of $\overline{SK}$ after $\overline{CS}$ goes low. A start-bit can only be recognized when the high of DI is latched at the rising edge of $\overline{SK}$ after changing $\overline{CS}$ to low, it is impossible for it to be recognized as long as DI is low, even if there are $\overline{SK}$ pulses after $\overline{CS}$ goes low. Instruction finishes when $\overline{CS}$ goes high, where it must be high between commands during t_{CDS}.

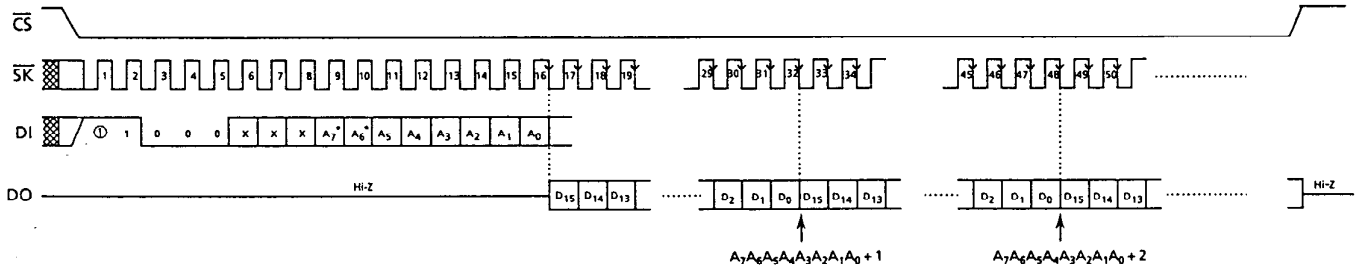
All input, including DI and $\overline{SK}$ signals, is ignored while $\overline{CS}$ is high, which is stand-by mode. The start bit + instruction, address, and data are 8-bit instructions. This makes it easy to prepare your own software using a serial interface incorporated into the CPU.

1. READ

The READ instruction reads data from a specified address. After A0 is latched at the risig edge of $\overline{SK}$, 16-bit data is continuously output in synchronization with the falling edge of $\overline{SK}$.

When all of the data (D_{15} to D_0) in the specified address has been read, data in the next address can be read with the input of another $\overline{SK}$ clock. Thus, the data over whole area of the memory can be read by continuously inputting $\overline{SK}$ clocks as long as $\overline{CS}$ is low.

The last address (An ··· A1 A0 = 1 ··· 11) rolls over to the top address (An ··· A1 A0 = 0 ··· 00).



* On the S-29L194A, A_7 and A_6 are optional.
On the S-29L294A, A_7 is optional.

Figure 5 Read Timing (S-29L394A)

2. PROGRAM

The PROGRAM instruction automatically begins writing to the non-volatile memory when $\overline{CS}$ goes high at the completion of the specified clock input.

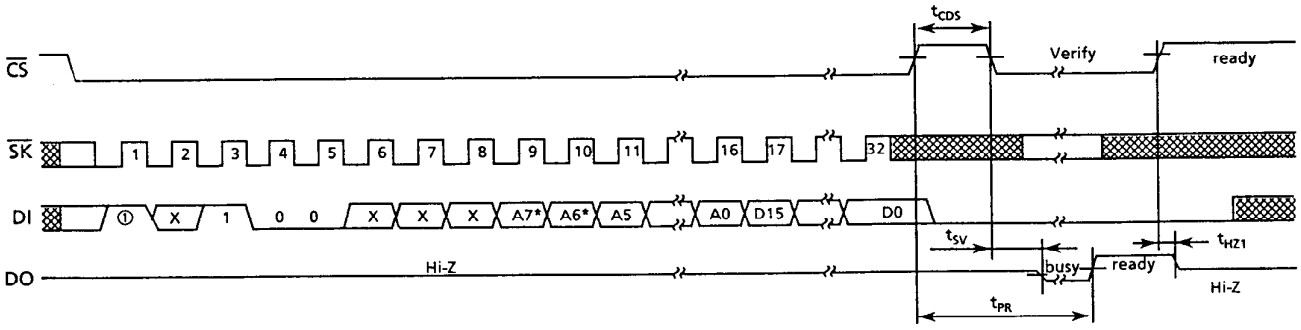
The write operation is completed in 10 ms (t_{PR} Max.), and the typical write period is less than 5 ms. In the S-29LX94A Series, it is easy to VERIFY the completion of the write operation in order to minimize the write cycle by setting $\overline{CS}$ to low and checking the DO pin, which is low during the write operation and high after its completion. This VERIFY procedure can be executed over and over again.
There are two methods to detect a change in the DO output. One is to detect a change from low to high setting $\overline{CS}$ to low, and the other is to detect a change from low to high as a result of repetitous operations of returning the $\overline{CS}$ to high after setting $\overline{CS}$ to low and checking the DO output.

Because all $\overline{SK}$ and DI inputs are ignored during the write operation, any input of instruction will also be disregarded. When DO outputs high after completion of the write operation or if it is in the high-impedence state (Hi-Z), the input of instructions is available. Even if the DO pin remains high, it will enter the high-impedence state upon the recognition of a high of DI (start-bit) attached to the rising edge of an $\overline{SK}$ pulse.

DI input should be low during the VERIFY procedure.

2.1 PROGRAM

This instruction writes 16-bit data to a specified address.
After changing $\overline{CS}$ to low, input a start-bit, op-code (PROGRAM), address, and 16-bit data. If there is a data overflow of more than 16 bits, only the last 16-bits of the data is considered valid. Changing $\overline{CS}$ to high will start the PROGRAM operation. It is not necessary to make the data "1" before initiating the PROGRAM operation.



* On the S-29L194A, A_7 and A_6 are optional.
On the S-29L294A, A_7 is optional.

Figure 6 WRITE Timing (S-29L394A)

3. Write enable (PEN) and Write disable (PDS)

The PEN instruction puts the S-29LX94A Series into write enable mode, which accepts PROGRAM instruction. The PDS instruction puts the S-29LX94A Series into write disable mode, which refuses PROGRAM instruction.
The S-29LX94A Series powers on in write disable mode, which protects data against unexpected, erroneous write operations caused by noise and/or CPU malfunctions. It should be kept in write disable mode except when performing write operations.

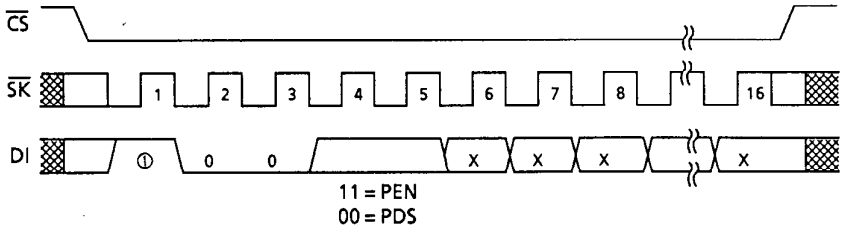


Figure 7 PEN/PDS Timing

■ Receiving a Start-Bit

A start-bit can be recognized by latching the high level of DI at the rising edge of $\overline{SK}$ after changing $\overline{CS}$ to low (Start-Bit Recognition). The write operation begins by inputting the write instruction and setting $\overline{CS}$ to high. The DO pin then outputs low during the write operation and high at its completion by setting $\overline{CS}$ to low (Verify Operation). Therefore, only after a write operation, in order to accept the next command by having $\overline{CS}$ go low, the DO pin is switched from a state of high-impedence to a state of data output; but if it recognizes a start-bit, the DO pin returns to a state of high-impedence (see Figure 3).

Make sure that data output from the CPU does not interfere with the data output from the serial memory IC when you configure a 3-wire interface by connecting DI input pin and DO output pin. Such interference may cause a start-bit fetch problem.

■ Three-wire Interface (DI-DO direct connection)

Although the normal configuration of a serial interface is a 4-wire interface to $\overline{CS}$, $\overline{SK}$, DI, and DO, a 3-wire interface is also a possibility by connecting DI and DO. However, since there is a possibility that the DO output from the serial memory IC will interfere with the data output from the CPU with a 3-wire interface, install a resistor between DI and DO in order to give preference to data output from the CPU to DI (See Figure 8).

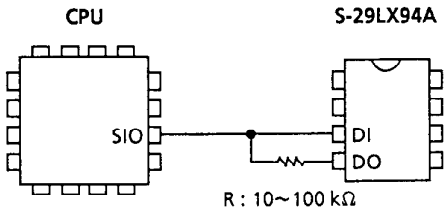


Figure 8 3-wire interface

■ Connecting to the CPU with a Serial Port

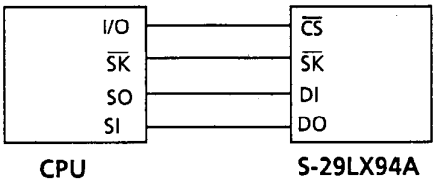


Figure 9 Connectin Example

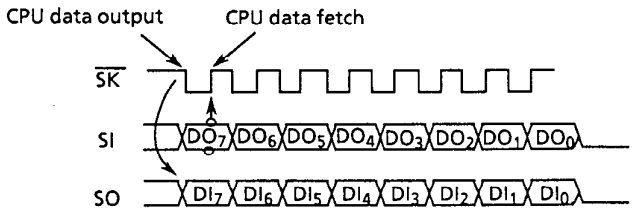


Figure 10 Serial Shift Timing

■ Memory Protection

The S-29LX94A Series is capable of protecting the memory. So, the contents of the memory will not be miswritten due to error run or malfunction of the CPU. When the $\overline{\text{PROTECT}}$ terminal is connected to GND or OPEN, write to Bank 1 in the memory array is prohibited (50% of the memory can be protected starting from address 00). Because the pull-down resistance is connected to the $\overline{\text{PROTECT}}$ terminal internally, the memory can be automatically protected when the $\overline{\text{PROTECT}}$ terminal is OPEN. When the protection is valid, the data in the memory of Bank 1 will not be rewritten. However, because the write control circuit inside the IC functions, the next instruction cannot be executed during the time period of writing (t_{PR}). While write instruction is being input and write is being executed, always connect the $\overline{\text{PROTECT}}$ terminal to "H," "L" or OPEN, and leave the input signal unchanged (see Figure 11).

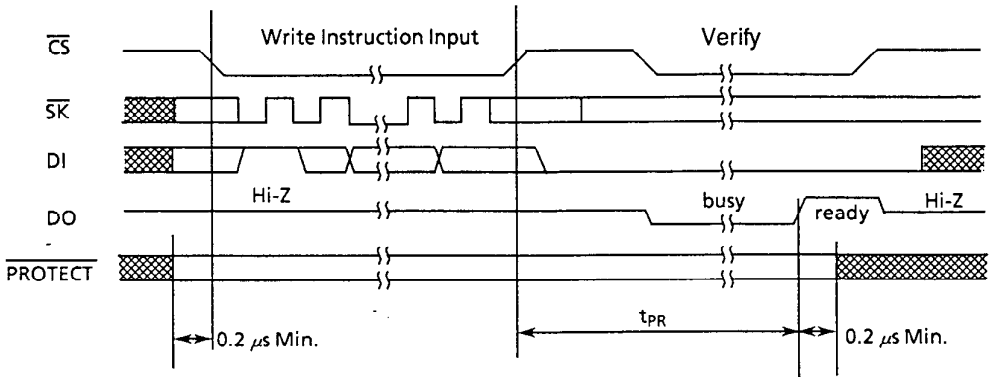


Figure 11 PROTECT Terminal Input Signal Timing

■ Dimensions (Unit : mm)

1. 8-pin SOP

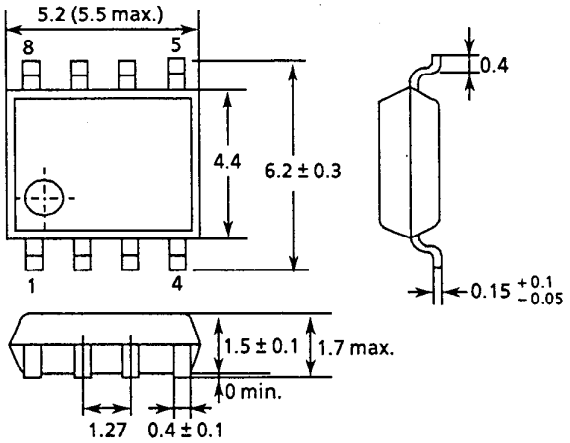


Figure 12

2. 8-pin SSOP

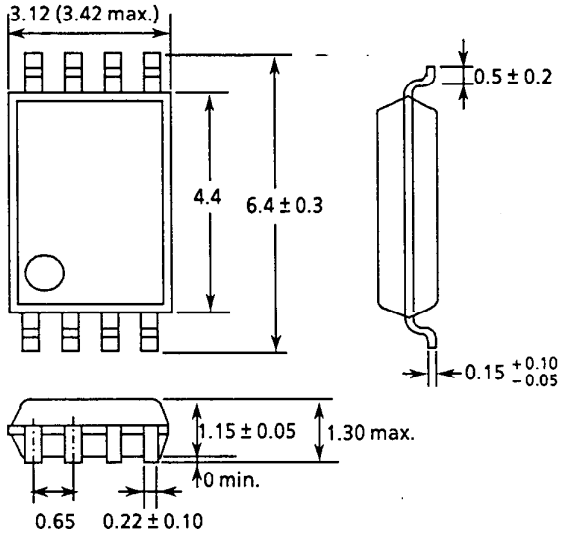


Figure 13

■ Ordering Information

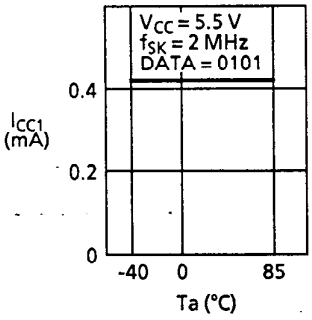
S-29LX94A XXX

- Package: DFE: SOP2, FS : SSOP
- Product name: S-29L194A : 1K-bit, S-29L294A : 2K-bit, S-29L394A : 4K-bit

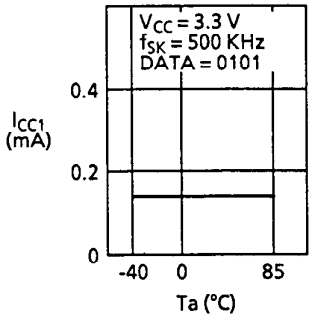
■ Characteristics

1. DC Characteristics

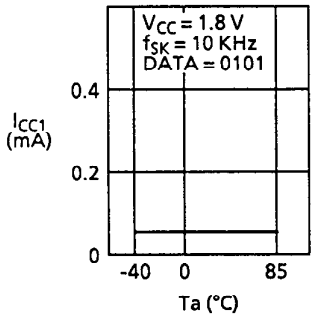
1.1 Current consumption (READ) I_{CC1} — Ambient temperature Ta



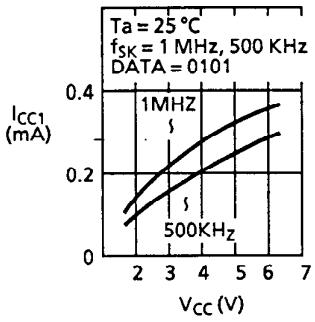
1.2 Current consumption (READ) I_{CC1} — Ambient temperature Ta



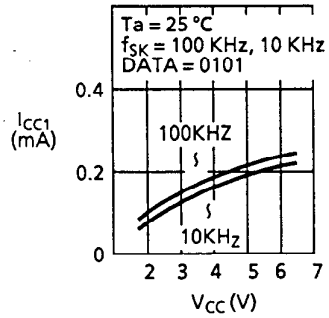
1.3 Current consumption (READ) I_{CC1} — Ambient temperature Ta



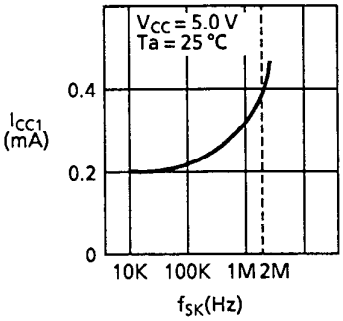
1.4 Current consumption (READ) I_{CC1} — Power supply voltage V_{CC}



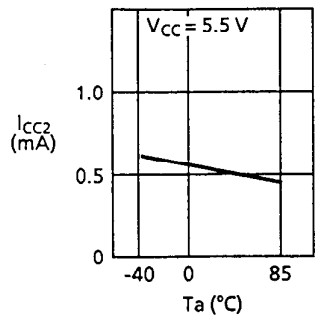
1.5 Current consumption (READ) I_{CC1} — Power supply voltage V_{CC}



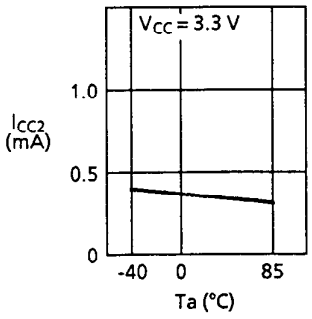
1.6 Current consumption (READ) I_{CC1} — Clock frequency f_{SK}



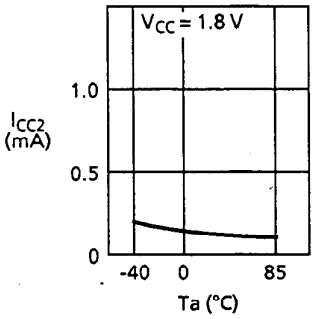
1.7 Current consumption (PROGRAM) I_{CC2} – Ambient temperature Ta



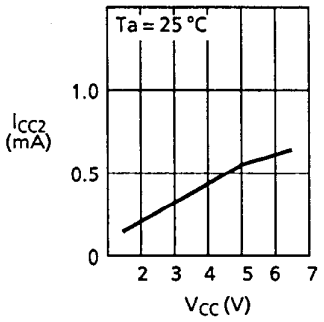
1.8 Current consumption (PROGRAM) I_{CC2} – Ambient temperature Ta



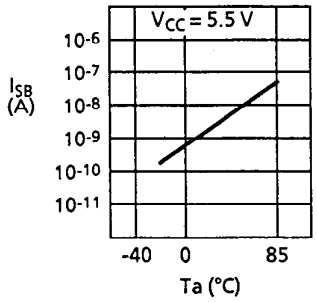
1.9 Current consumption (PROGRAM) I_{CC2} – Ambient temperature Ta



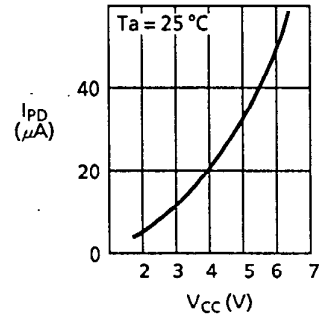
1.10 Current consumption (PROGRAM) I_{CC2} – Power supply voltage V_{CC}



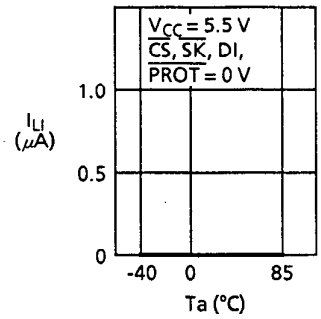
1.11 Standby current consumption I_{SB} — Ambient temperature Ta



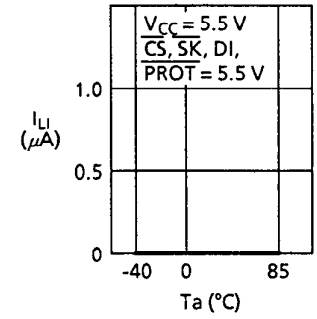
1.12 Pull-Down current I_{PD} — Power supply voltageV_{CC}



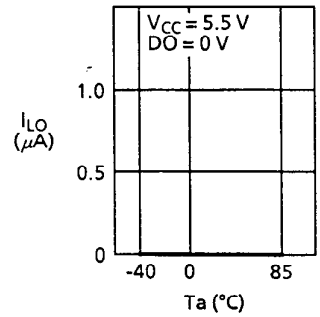
1.13 Input leakage current I_{LI} – Ambient temperature Ta



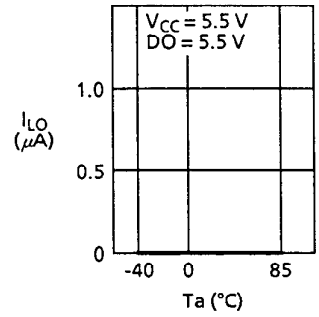
1.14 Input leakage current I_{LI} – Ambient temperature Ta



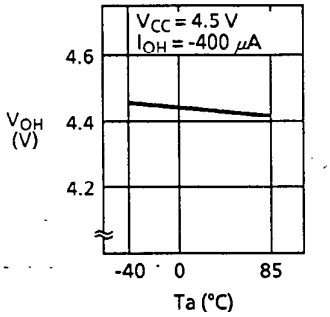
1.15 Output leakage current I_{LO} – Ambient temperature Ta



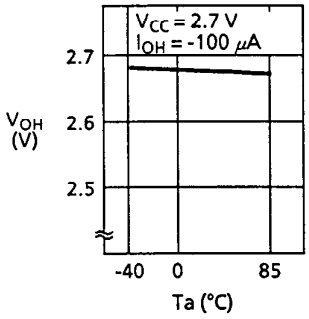
1.16 Output leakage current I_{LO} – Ambient temperature Ta



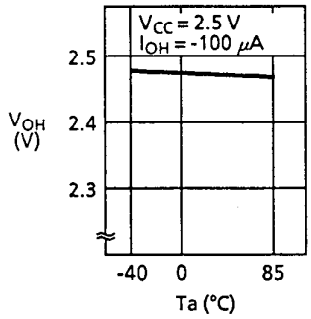
1.17 High level output voltage V_{OH} – Ambient temperature Ta



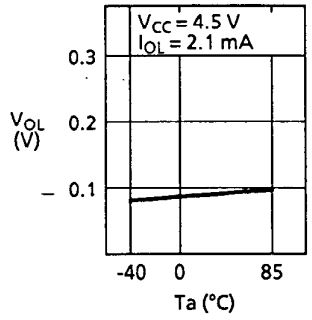
1.18 High level output voltage V_{OH} – Ambient temperature Ta



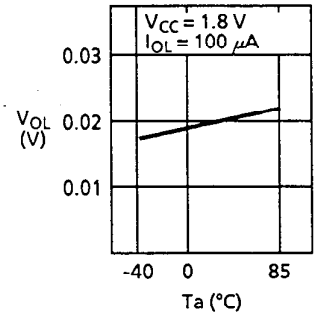
1.19 High level output voltage V_{OH} – Ambient temperature Ta



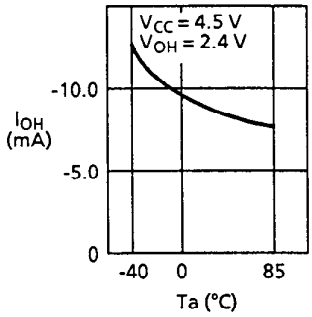
1.20 Low level output voltage V_{OL} – Ambient temperature Ta



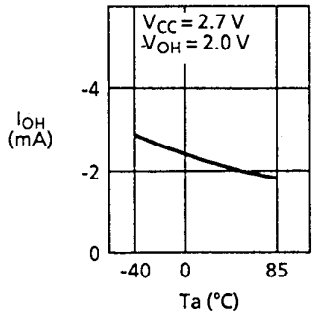
1.21 Low level output voltage V_{OL} – Ambient temperature Ta



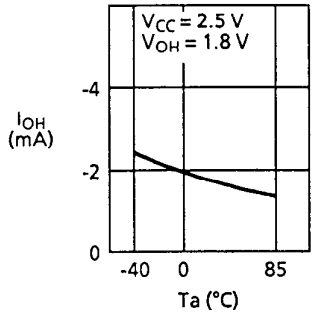
1.22 High level output current I_{OH} – Ambient temperature Ta



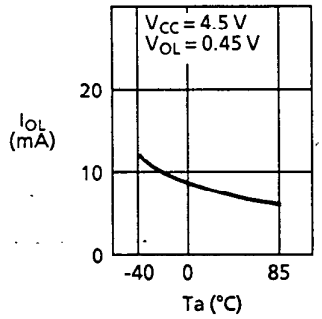
1.23 High level output current I_{OH} – Ambient temperature Ta



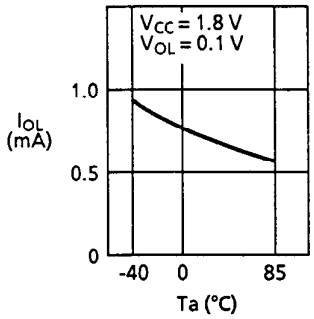
1.24 High level output current I_{OH} – Ambient temperature Ta



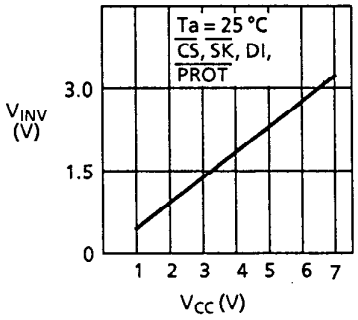
1.25 Low level output current I_{OL} – Ambient temperature Ta



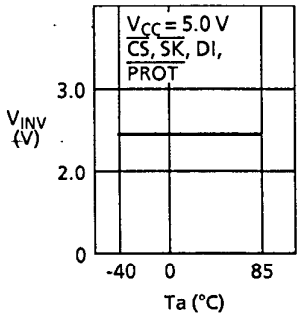
1.26 Low level output current I_{OL} – Ambient temperature Ta



1.27 Input inversion voltage V_{INV} – Power supply voltage V_{CC}

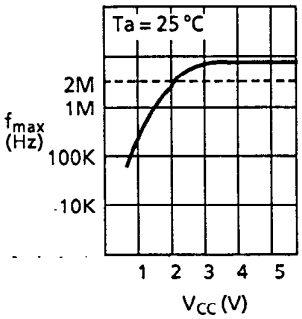


1.28 Input inversion voltage V_{INV} – Ambient temperature Ta

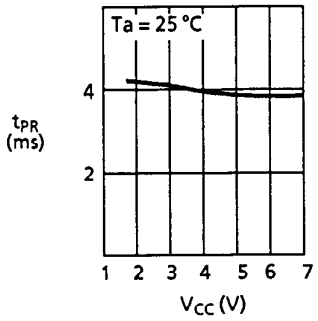


2. AC Characteristics

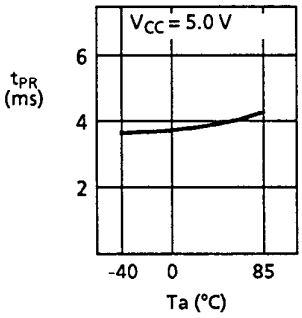
2.1 Maximum operating frequency f_{max} – Power supply voltage V_{CC}



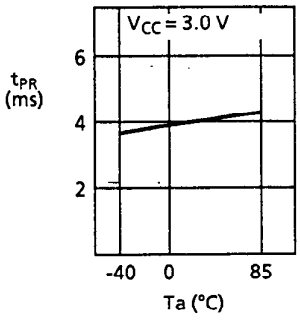
2.2 Program time t_{PR} – Power supply voltage V_{CC}



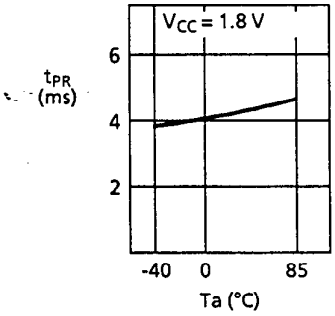
2.3 Program time t_{PR} – Ambient temperature Ta



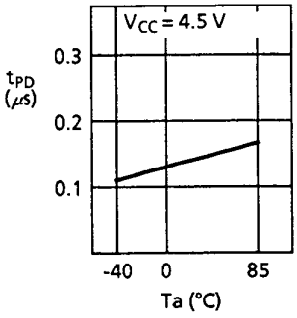
2.4 Program time t_{PR} – Ambient temperature Ta



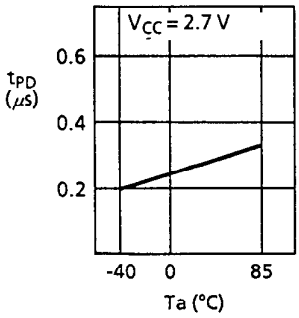
2.5 Program time t_{PR} – Ambient temperature Ta



2.6 Data output delay time t_{PD} – Ambient temperature Ta



2.7 Data output delay time t_{PD} – Ambient temperature Ta



2.8 Data output delay time t_{PD} – Ambient temperature Ta