

## **ACST2 Series**

## AC Switch family Alternating current switch

#### **Main features**

Symbol	Value	Unit
I <sub>T(RMS)</sub>	2	Α
V <sub>DRM</sub> /V <sub>RRM</sub>	800	V
I <sub>GT</sub>	10	mA

- Overvoltage crowbar technology
- High noise immunity: static dV/dt > 500 V/µs

The ACST2-8SFP in the TO-220FPAB package provides insulation voltage rated at  $1500V_{\rm BMS}$ 

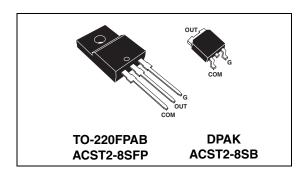
#### Main application

- AC ON/OFF static switching in appliances & industrial control systems
- Drive of low power highly resistive or inductive loads like:
  - solenoid,
  - pump, fan, micro-motor

### **Description**

The ACST2 series belongs to the AC power switch family built around the ASD technology. This high performance device is adapted to home appliances or industrial systems and drives loads up to 2 A.

This ACST2 switch embeds a Triac structure with a high voltage clamping device to absorb the inductive turn-off energy and withstand line transients such as those described in the IEC 61000-4-5 standards. The component needs a low gate current to be activated ( $I_{\rm GT} < 10$  mA) and in the mean time provides a high electrical noise immunity such as those described in the IEC 61000-4-4 standards.



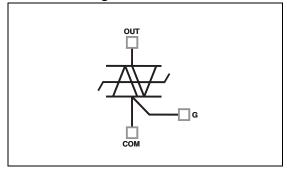
#### **Benefits**

- Enables equipment to meet IEC 61000-4-5
- High off-state reliability with planar technology
- Needs no external overvoltage protection
- Reduces component count
- Interfaces directly with the micro-controller
- High immunity against fast transients described in IEC 61000-4-4 standards

#### Order code

Part number	Marking
ACST2-8SFP	ACST28S
ACST2-8SB	ACST28S

#### **Functional diagram**



Characteristics ACST2 Series

## 1 Characteristics

Table 1. Absolute maximum ratings (limiting values)

Symbol	Paramete	r		Value	Unit
1	RMS on-state current (full sine wave)	TO-220FPAB	T <sub>c</sub> = 105° C	2	Α
I <sub>T(RMS)</sub>	Inividual current (tuli sine wave)	DPAK	T <sub>c</sub> = 110 °C	2	
l	Non repetitive surge peak on-state current	F = 60 Hz	t = 16.7 ms	8.4	Α
I <sub>TSM</sub>	(full cycle sine wave, T <sub>J</sub> initial = 25° C)	F = 50 Hz	t = 20 ms	8.0	
l <sup>2</sup> t	I <sup>2</sup> t Value for fusing	t <sub>p</sub> = 10 ms		0.5	A <sup>2</sup> s
dl/dt	Critical rate of rise of on-state current $I_G = 2 \times I_{GT}$ , $t_r = 100 \text{ ns}$	F = 120 Hz	Tj = 125° C	50	A/μs
V <sub>PP</sub> <sup>(1)</sup>	Non repetitive line peak mains voltage (1)		Tj = 25° C	2	kV
P <sub>G(AV)</sub>	Average gate power dissipation Tj		Tj = 125° C	0.1	W
P <sub>GM</sub>	Peak gate power dissipation ( $t_p = 20 \mu s$ ) $T_j = 12$		Tj = 125° C	10	W
I <sub>GM</sub>	Peak gate current ( $t_p = 20 \mu s$ ) Tj = 125° C		1.6	Α	
T <sub>stg</sub> T <sub>j</sub>	Storage junction temperature range Operating junction temperature range	-40 to +150 -40 to +125	°C		
T <sub>I</sub>	Maximum lead soldering temperature durin	g 10 s (at 3 mm	from plastic case)	260	° C

<sup>1.</sup> according to test described by IEC 61000-4-5 standard and Figure 16

Table 2. Electrical characteristics ( $T_i = 25^{\circ}$  C, unless otherwise specified)

Symbol	Test conditions Quadrar			Value	Unit
I <sub>GT</sub> <sup>(1)</sup>	$V_{OUT}$ = 12 V R <sub>L</sub> = 33 $\Omega$		MAX	10	mA
V <sub>GT</sub>	$V_{OUT}$ = 12 V R <sub>L</sub> = 33 $\Omega$	1 - 11 - 111	MAX	1.1	V
$V_{GD}$	$V_{OUT} = V_{DRM} R_L = 3.3 \text{ k}\Omega T_j = 125^{\circ} \text{ C}$ I - II - III		MIN	0.2	V
I <sub>H</sub> <sup>(2)</sup>	I <sub>OUT</sub> = 100 mA			10	mA
	I <sub>G</sub> = 1.2 x I <sub>GT</sub>	1 - 111	MAX	25	mA
ΙL	IG = 1.2 X IGT	II	MAX	35	ША
dV/dt (2)	V <sub>OUT</sub> = 67% V <sub>DRM</sub> gate open T <sub>j</sub> = 125° C			500	V/µs
(dl/dt)c (2)	$(dV/dt)c = 15 V/\mu s T_j = 125^{\circ} C$		MIN	0.5	A/ms
V <sub>CL</sub>	$I_{CL} = 0.1 \text{ mA t}_p = 1 \text{ ms T}_j = 25^{\circ} \text{ C}$		MIN	850	V

<sup>1.</sup> minimum  $\rm I_{GT}$  is guaranteed at 5% of  $\rm I_{GT}$  max

<sup>2.</sup> for both polarity of OUT pin referenced to COM pin

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Table 3. Static electrical characteristics

Symbol	Test conditions		Value	Unit	
V <sub>TM</sub> <sup>(1)</sup>	I <sub>TM</sub> = 2.8 A t <sub>p</sub> = 500 μs	T <sub>j</sub> = 25° C	MAX	2	V
V <sub>TO</sub> <sup>(1)</sup>	Threshold voltage	T <sub>j</sub> = 125° C	MAX	0.9	V
R <sub>D</sub> <sup>(1)</sup>	Dynamic resistance	T <sub>j</sub> = 125° C	MAX	250	$m\Omega$
I <sub>DRM</sub>	V -V /V	T <sub>j</sub> = 25° C	MAX	10	μΑ
I <sub>RRM</sub>	$V_{OUT} = V_{DRM} / V_{RRM}$	T <sub>j</sub> = 125° C	IVIAA	0.5	mA

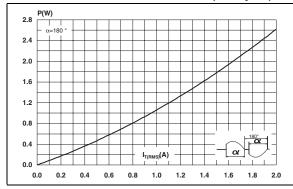
<sup>1.</sup> for both polarity of OUT pin referenced to COM pin

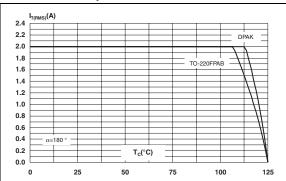
Table 4. Thermal resistances

Symbol	Parameter				Unit
В	lunction to cook (AC)		DPAK	4.5	
□ th(j-c)	R <sub>th(j-c)</sub> Junction to case (AC)		TO-220FPAB	7	° C/W
В	Junction to ambient		TO-220FPAB	60	C/VV
$R_{th(j-a)}$	Junction to ambient	$S_{CU}^{(1)} = 0.5 \text{ cm}^2$	DPAK	70	

<sup>1.</sup>  $S_{CU} = copper surface under tab$ 

Figure 1. Maximum power dissipation versus Figure 2. RMS on-state current versus case RMS on-state current (full cycle) temperature





Characteristics ACST2 Series

Figure 3. RMS on-state current versus ambient temperature

Figure 4. Relative variation of thermal impedance versus pulse duration - TO-220FPAB

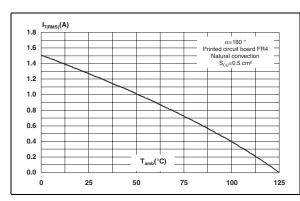
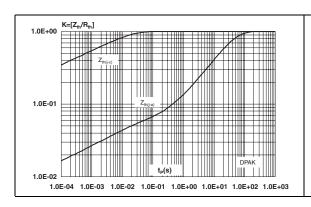


Figure 5. Relative variation of thermal impedance versus pulse duration - DPAK

Figure 6. Relative variation of gate trigger current  $I_{GT}$ , holding current  $I_{H}$  and latching current  $I_{L}$  versus junction temperature (typical values)



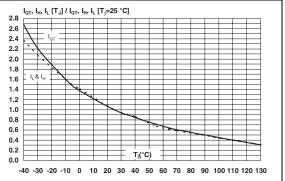
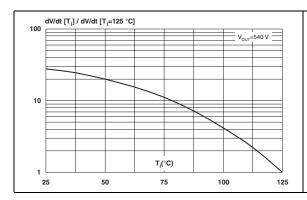
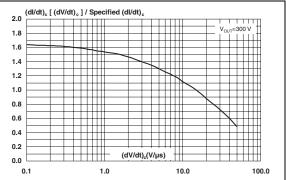


Figure 7. Relative variation of static dV/dt versus junction temperature

Figure 8. Relative variation of critical rate of decrease of main current versus reapplied dV/dt (typical values)





**ACST2 Series Characteristics** 

Relative variation of critical rate of Figure 10. Surge peak on-state current versus Figure 9. decrease of main current versus number of cycles junction temperature

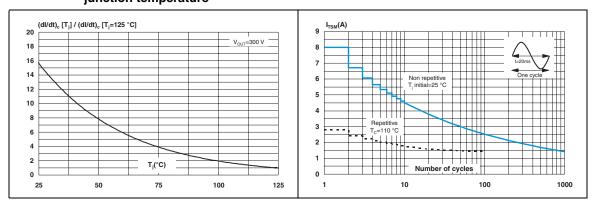


Figure 11. Non repetitive surge peak on-state Figure 12. On-state characteristics (maximum current for a sinusoidal pulse with width  $t_P < 10$  ms, and corresponding value of I<sup>2</sup>t

values)

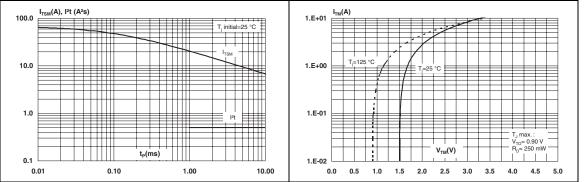
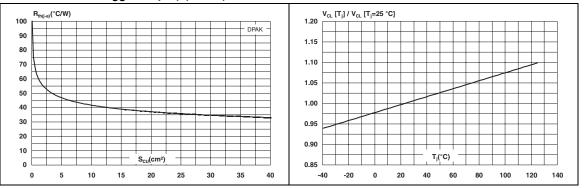


Figure 13. Thermal resistance junction to ambient versus copper surface under tab (printed circuit board FR4,  $e_{CU} = 35 \mu m$ ) (DPAK)

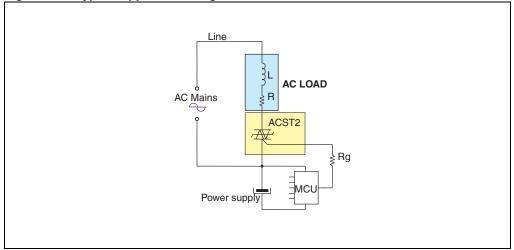
Figure 14. Relative variation of clamping voltage V<sub>CL</sub> versus junction temperature



### 2 AC line switch basic application

The ACST2 device has been designed to switch on and off highly inductive or resistive loads such as pump, valve, fan, or bulb lamp. Thanks to its high sensitivity ( $I_{GT}$  max = 10 mA), the ACST2 can be driven directly by logic level circuits through a resistor as shown on the typical application diagram. Thanks to its thermal and turn-off commutation performances, the ACST2 switch can drive, without any additional snubber, an inductive load up to 2 A.

Figure 15. Typical application diagram



## 2.1 Protection against overvoltage: the best choice is ACST

In comparison with standard triacs, which are not robust against surge voltages, the ACST2 is over-voltage self-protected, specified by the new parameter  $V_{CL}$ . In addition, ACST2 is a sensitive device ( $I_{GT} = 10 \text{mA}$ ), but provides a high noise immunity level against fast transients.

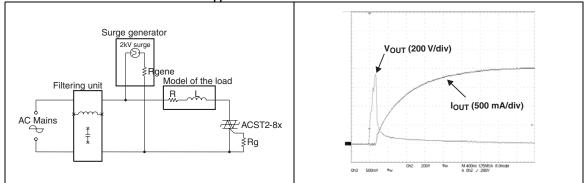
The ACST2 switch is able to sustain safely the AC line transient voltages either by clamping the low energy spikes or by breaking over under high energy shocks, even with fast turn-on current rises.

The test circuit of the *Figure 16* is representative of the final ACST2 application, and is also used to stress the ACST switch according to the IEC 61000-4-5 standard conditions. Thanks to the load limiting the current, the ACST switch sustains the voltage spikes up to 2 kV above the peak line voltage. The protection is based on an overvoltage crowbar technology. Actually, the ACST2 will break over safely as shown on *Figure 17*. The ACST is recovering its blocking voltage capability at the next zero current crossing point. Such non repetitive test can be done 10 times on each AC line voltage polarity.

Figure 16. Overvoltage ruggedness test circuit Figure 17. for resistive and inductive loads according to IEC 61000-4-5 standards:

Typical current and voltage waveforms across the ACST2 during IEC 61000-4-5 standard test

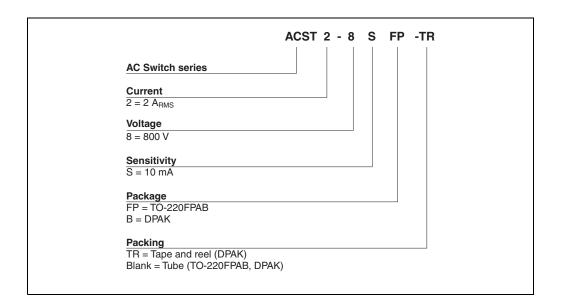
R = 200  $\Omega$ , L = 10  $\mu$ H, V<sub>pp</sub> = 2 kV



### 2.2 Electrical noise immunity

Even if the ACST2 is a sensitive device ( $I_{GT} = 10 \text{ mA}$ ) and can be controlled directly though a simple resistor by a logic level circuit, it provides a high electrical noise immunity. The intrinsic immunity of the ACST2 is shown by the specified dV/dt equal to 500 V/ $\mu$ s @ 125° C. This immunity level is 5 to 10 times higher than the immunity provided by an equivalent standard technology triac with the same sensitivity. In other word, ACST2 is sensitive, but has an immunity reaching the one provided by non-sensitive device ( $I_{GT}$  higher than 35 mA).

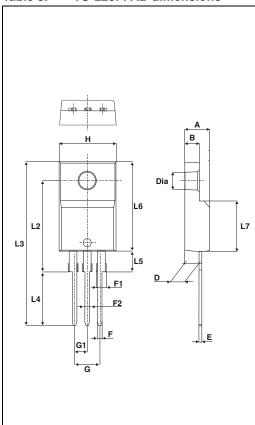
## 3 Ordering information scheme



# 4 Package information

Epoxy meets UL94, V0

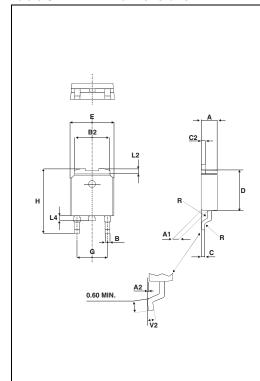
Table 5. TO-220FPAB dimensions



	Dimensions				
Ref.	Millimeters		Inc	hes	
	Min.	Max.	Min.	Max.	
Α	4.4	4.6	0.173	0.181	
В	2.5	2.7	0.098	0.106	
D	2.5	2.75	0.098	0.108	
Е	0.45	0.70	0.018	0.027	
F	0.75	1	0.030	0.039	
F1	1.15	1.70	0.045	0.067	
F2	1.15	1.70	0.045	0.067	
G	4.95	5.20	0.195	0.205	
G1	2.4	2.7	0.094	0.106	
Н	10	10.4	0.393	0.409	
L2	16	Тур.	0.63	Тур.	
L3	28.6	30.6	1.126	1.205	
L4	9.8	10.6	0.386	0.417	
L5	2.9	3.6	0.114	0.142	
L6	15.9	16.4	0.626	0.646	
L7	9.00	9.30	0.354	0.366	
Dia.	3.00	3.20	0.118	0.126	

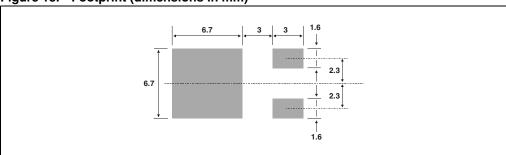
ACST2 Series Package information

Table 6. DPAK dimensions



	Dimensions				
Ref.	Millimeters		Inc	hes	
	Min.	Max.	Min.	Max.	
Α	2.20	2.40	0.086	0.094	
A1	0.90	1.10	0.035	0.043	
A2	0.03	0.23	0.001	0.009	
В	0.64	0.90	0.025	0.035	
B2	5.20	5.40	0.204	0.212	
С	0.45	0.60	0.017	0.023	
C2	0.48	0.60	0.018	0.023	
D	6.00	6.20	0.236	0.244	
Е	6.40	6.60	0.251	0.259	
G	4.40	4.60	0.173	0.181	
Н	9.35	10.10	0.368	0.397	
L2	0.80 typ.		0.03	1 typ.	
L4	0.60	1.00	0.023	0.039	
V2	0°	8°	0°	8°	

Figure 18. Footprint (dimensions in mm)



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Ordering information ACST2 Series

# 5 Ordering information

Part number	Marking	Package	Weight	Base Qty	Packing mode
ACST2-8SFP	ACST28S	TO-220FPAB	2.4g	50	Tube
ACST2-8SB	ACST28S	DPAK	0.3g	50	Tube
ACST2-8SB-TR	ACST28S	DPAK	0.3g	2500	Tape and Reel

# 6 Revision history

Date	Revision	Changes
01-Mar-2007	1	Initial release.

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