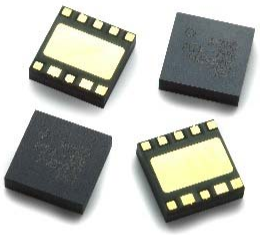
ACPM-7886
TD-SCDMA Power Amplifier

Data Sheet



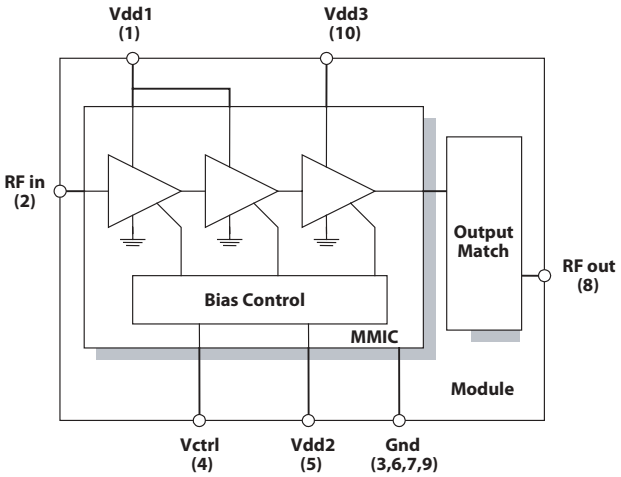
General Description

The ACPM-7886 is an amplifier module designed for TD-SCDMA applications in the 2010-2025MHz band. Designed around Avago Technologies' GaAs Enhancement Mode pHEMT process, the ACPM-7886 offers premium performance in a very small form factor. It is matched to 50 Ohms on the input and output.

The amplifier has excellent ACLR and efficiency performance at max Pout and low quiescent current (50mA) with a single bias control voltage, Vctrl = 2.0V.

Designed in a surface mount RF package, the ACPM-7886 is very cost and size competitive.

Functional Block Diagram



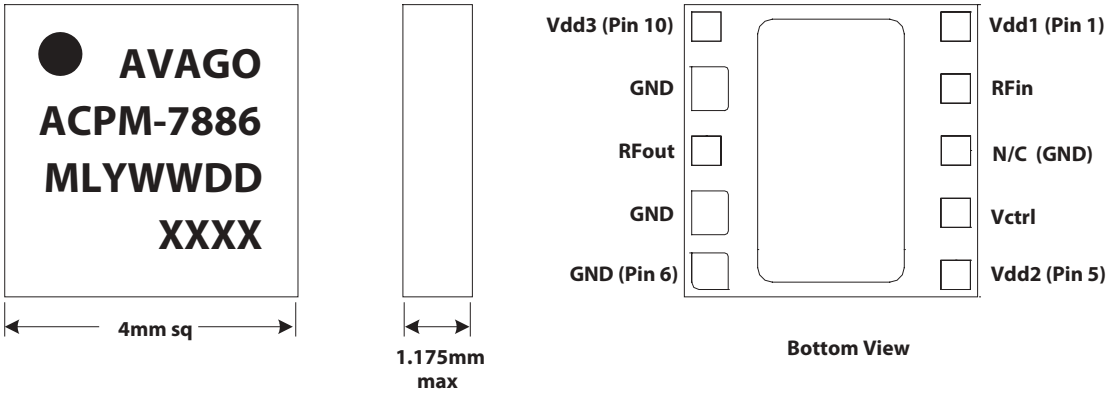
Features

- Operating frequency: 2010 - 2025 MHz
- 28 dBm Linear Output Power @ 3.5V
- High Efficiency 41% PAE
- Single bias, low quiescent current (50mA)
- Internal 50 ohm matching networks for both RF input & output
- 3.2 - 4.2 V linear operation
- 4.0 x 4.0mm SMT Package
- Low package profile, 1.1mm

Applications

- TD-SCDMA Handsets
- TD-SCDMA Data Cards
- TD-SCDMA PDAs

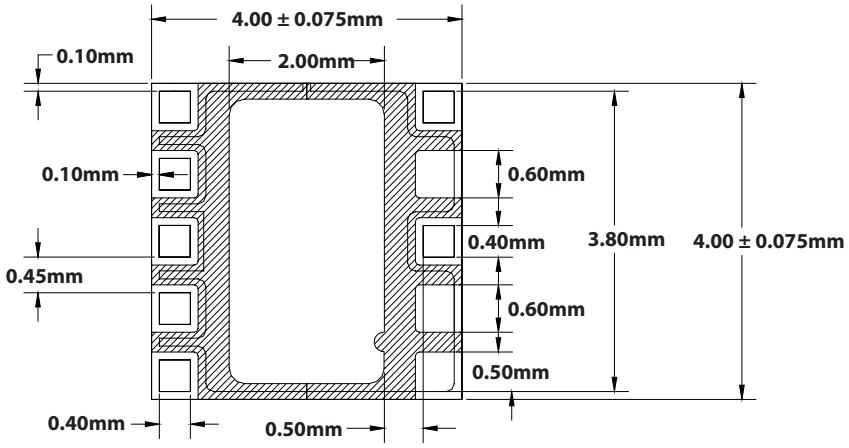
Package Diagram



Pin Description Table

Pin Number	Pin Label	Description	Function
1	Vdd1	Supply bias	1st and 2nd stages drain bias, nominally 3.5V
2	RFin	RF input	Signal input, internally grounded through inductor. External DC block needed if DC voltage present on input trace.
3	N/C	No internal connection	Recommend ground connection on PCB
4	Vctrl	Control voltage	Output level control, nominally 2V
5	Vdd2	Supply bias	Bias circuit supply, > 2.5V; nominally 2.85V. Does not require a regulated input and can be connected directly to the battery, if desired.
6	Gnd	Ground	
7	Gnd	Ground	
8	RFout	RF output	Signal output, requires external DC block
9	Gnd	Ground	
10	Vdd3	Supply bias	3rd stage drain bias, nominally 3.5V

Package Dimensions



Viewed down through top of package

Marking Notes :

Row 3:
- ML = Manufacturing Location
- Y = Year
- WW = Work Week
- DD = Date Code

Row 4:
- XXXX = Trace Code (Avago Technologies internal reference)

Maximum Ratings Table

Parameter	Min.	Max.
Supply voltage, Vdd1 and Vdd3		5.0 V
Supply voltage, Vdd2	-1 V	5.0 V
Analog control voltage	-1 V	3.0 V
RF input power		+5 dBm
Operating case temperature		+90 °C
Load VSWR		12:1
Storage temperature (case temperature)	-30 °C	+100 °C

Notes:
1. Operation of this device in excess of any of these limits may cause permanent damage.
2. Avoid electrostatic discharge on I/O pins

Recommended Operating Conditions

Parameter	Min.	Typ.	Max.
Supply voltage, Vdd1 and Vdd3	1.0 V	3.5 V	4.5 V
Supply voltage, Vdd2	2.6 V	2.85 V	4.5 V
Control voltage	1.9 V	2.0 V	2.1 V
Case temperature	-20 °C		+85 °C

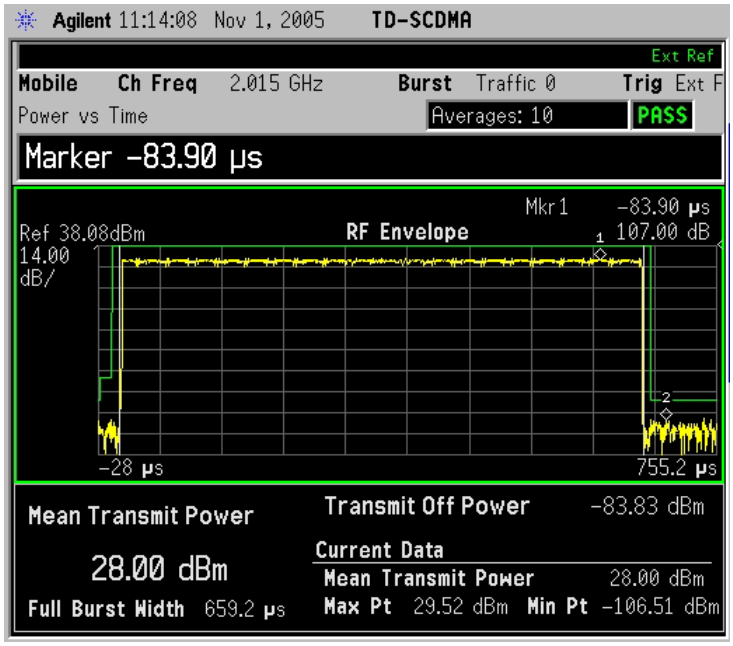
Electrical Characteristics of TD-SCDMA PA

Unless Otherwise Specified: f=2010-2025MHz, Vdd1=Vdd3=3.5V, Vdd2=2.85V, Vctrl=2.0V, Pout=28.0dBm, Ta=25°C, Zin/Zout = 50Ω

Parameter	min	typ	Max	Units
Leakage Current, Idd1,2,3; Vctrl=0 V, RF Off		20	80	uA
Control Current, Ictrl; Vctrl=2.0 V	75	110	145	uA
Bias Current, Idd2; Vctrl=2 V, Vdd2=2.85 V		6	10	mA
Quiescent Current, Idd1,3; RF Off Vctrl=2.0 V		50	80	mA
At Pout=28.0dBm				
Supply current Idd1+Idd3		435	480	mA
PAE including Vdd1,2,3	36	41		%
Gain	25.5	28.5	32	dB
Input VSWR		1.1	2.0:1	-
ACLR				
1.6MHz offset		-40	-35	dBc/1.28MHz
3.2MHz offset		-54	-48	dBc/1.28MHz
2nd Harmonic		-50	-40	dBc/1MHz
3rd Harmonic		-60	-45	dBc/1MHz
Noise Figure		3.1	4.1	dB
Stability, no spurious under conditions: VSWR=4:1, all phases 3<Vdd<4.5, -50 dBm to 28.0 dBm			-60	dBc
At Pout=16dBm				
Supply current Idd1+Idd3		120	145	mA
PAE including Vdd1,2,3		9.0		%
Gain		28		dB
Input VSWR		1.1		-
ACLR				
1.6MHz offset		-42	-35	dBc/1.28MHz
3.2MHz offset		-55	-49	dBc/1.28MHz

PA Operation/Shutdown Logic: DC signals

	Vctrl	Vdd2
Operational Mode	2.0V typ	2.6 ~ 3.5V (2.85V typ)
Shutdown	< 0.2V	0 ~ 4.5 V



Transmitter Off Power Dynamic Range: 107dB
Transmitt Off Power: -83dBm

Figure 1. Transmit off power.

Signal Studio Configuration

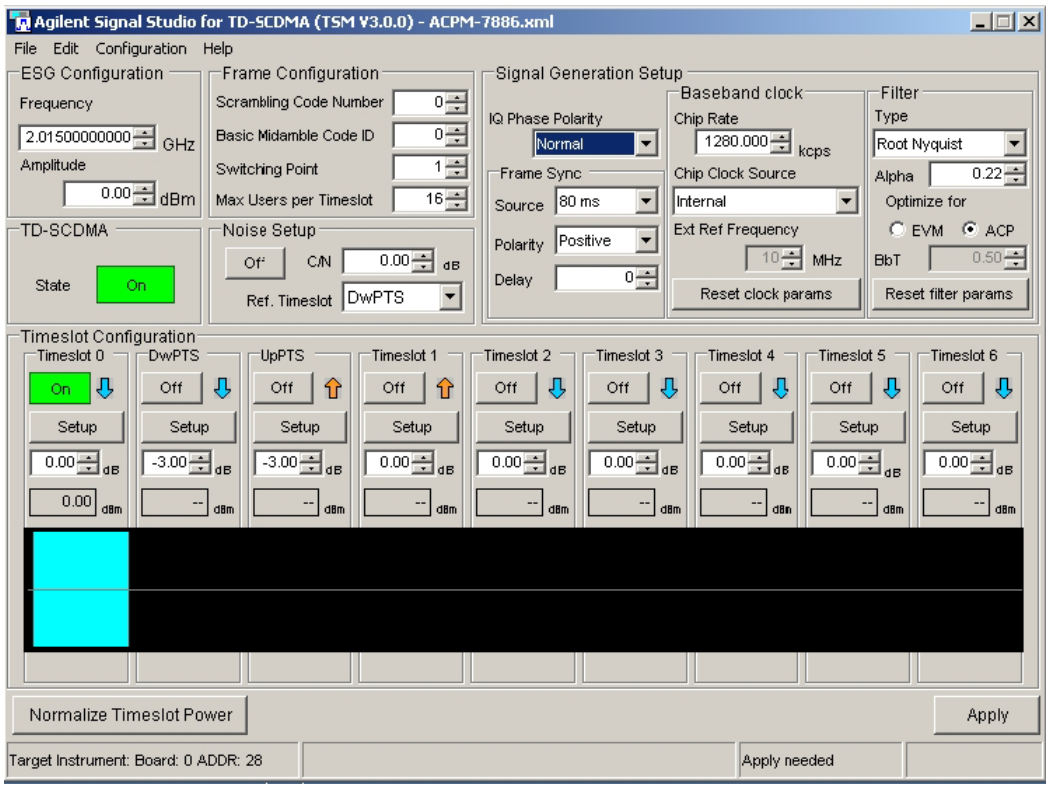


Figure 2 TD-SCDMA signal configuration.

ESD Sensitivity Level

Human Body Model (EIA/JESD22-A114B):
Class 1A (250Vmin, less than 500V)

Machine Model (EIA/JESD22-A115A):
Class A (50Vmin, less than 200V)

Notes:
ESD Sensitivity level for Human Body Model and Machine Model necessitate the following handling precautions:

1. Ensure Faraday cage or conductive shield bag is used during transportation processes.
2. If the static charge at SMT assemble station is above the device sensitivity level, place an ionizer near to the device for charge neutralization purposes.
3. Personal grounding must be worn at all times when handling the devices.

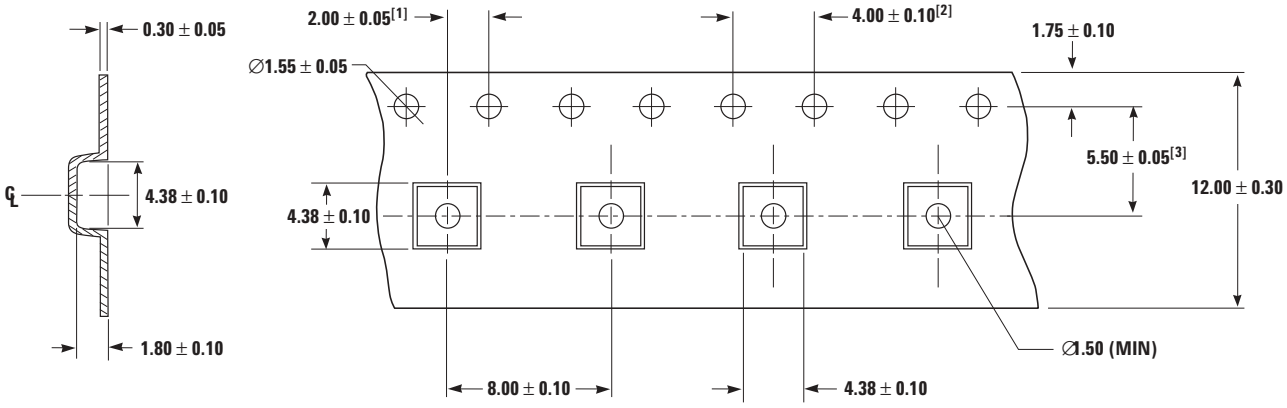
Moisture Sensitivity Classification: Class 3

Preconditioning per JESD22-A113-D Class 3 was performed on all devices prior to reliability testing.

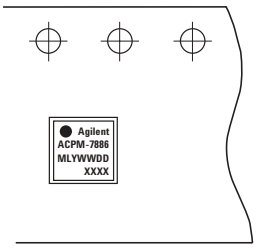
ACPM-7886 is a moisture sensitive component. It's important that the parts are handled under precaution and a proper manner. The handling, baking and out-of-pack storage conditions of the moisture sensitive components are described in IPC/JEDC S-STD-033A. Avago Technologies recommends utilizing the standard precautions listed below.

1. Calculated Shelf Life in Sealed Bag: 12 months at < 40°C and < 90% Relative Humidity (RH)
2. Peak Package Body Temperature: 250°C
3. After bag is opened, devices that will be subjected to reflow solder of other high temperature process must be:
   a. Mounted within 168 hours of factory condition ≤ 30°C / 60% RH
   b. Stored at <10% RH if not used
4. Devices require baking, before mounting if:
   a. Humidity indicator card is > 10% when read at 23 ± 5°C immediately after moisture barrier bag is opened.
   b. Items 3a or 3b is not met
5. If baking is required, please refer to J-STD-033 standard for low temperature (40°C) baking requirement in Tape/Reel form.

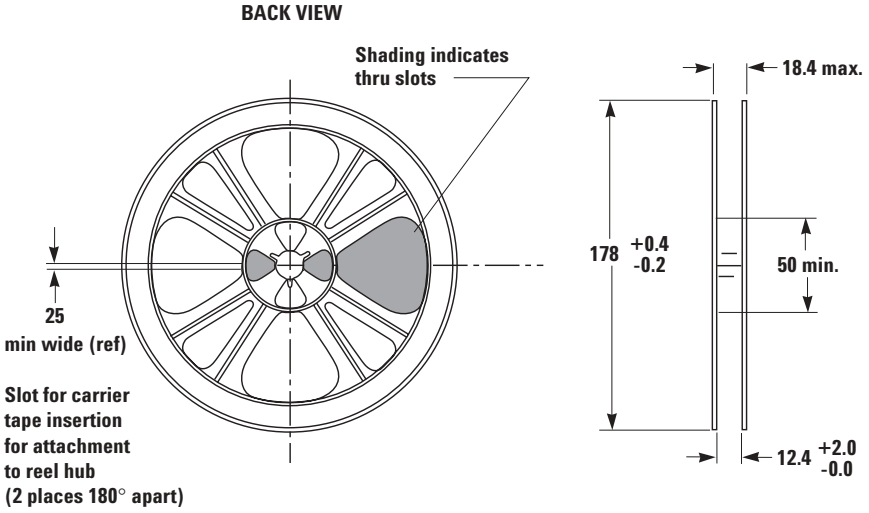
Tape Dimensions and Orientation

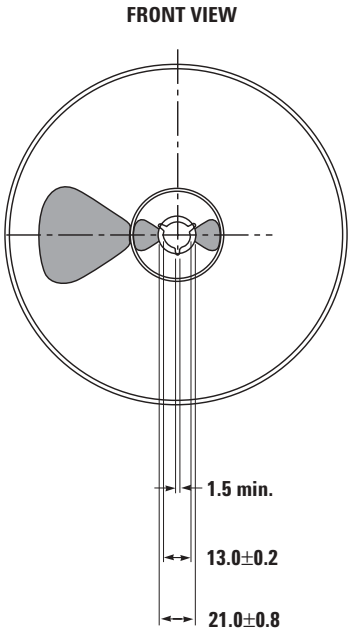


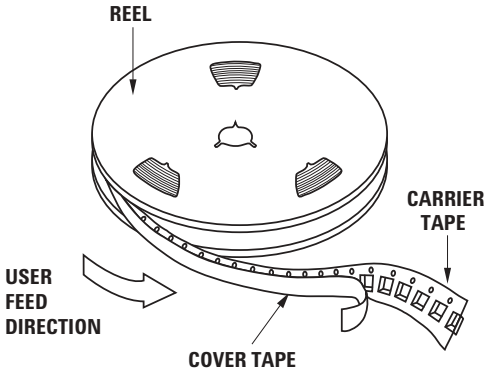
Notes:
1. Measured from centerline of sprocket hole to centerline of pocket
2. Cumulative tolerance of 10 sprocket holes is ± 0.2 mm
3. All dimensions in millimeters unless otherwise stated.



Reel Dimensions and Orientation







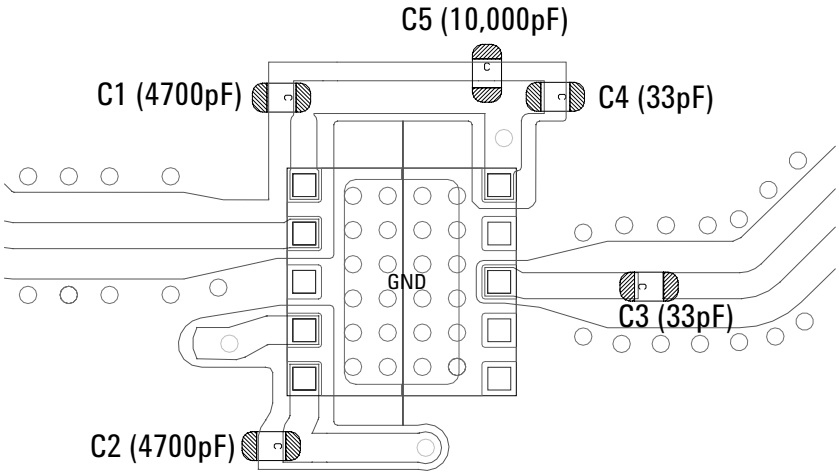
Notes:

1. Reel shall be labeled with the following information (as a minimum).
   a. manufacturers name or symbol
   b. Avago Technologies part number
   c. purchase order number
   d. date code
   e. quantity of units
2. A certificate of compliance shall be issued and accompany each shipment of product.
3. Reel must not be made with or contain ozone depleting materials.
4. All dimensions in millimeters (mm).

Order Information

Part Number	No. of Devices	Container
ACPM-7886-BLK	100	Bulk
ACPM-7886-TR1	1000	7" Tape and Reel

Suggested Board Implementation



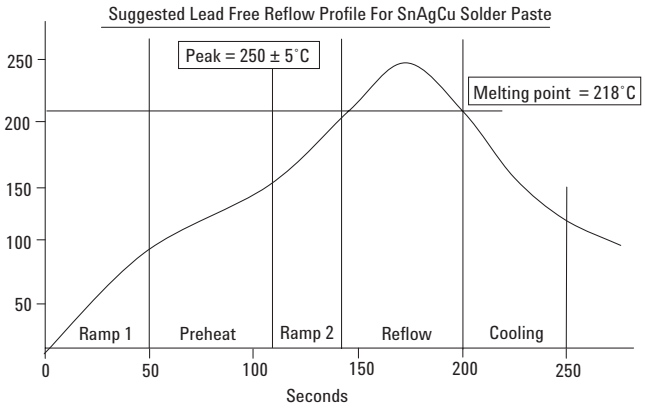
Notes:

1. All decoupling capacitors should be placed as close to the power module as possible.
2. RFin (Pin 2) has a grounded inductor inside package as a matching element. An external series capacitor is needed if a DC voltage is present.
3. An additional battery bypass capacitor should be placed on bias line before the battery terminal, but does not need to be immediately adjacent to the PA module. The bypass capacitor should be a large value, nominally between 2.2uF and 4.7uF.
4. Trace impedance on RF lines should be 50Ω.

Solder Reflow Profile

The most commonly used solder reflow method is accomplished in a belt furnace using convection heat transfer. This profile is designed to ensure reliable finished joints. However, the profile indicated will vary among different solder pastes from different manufacturers and is shown here for reference only.

Other factors that can affect the profile include the density and types of components on the board, type of solder used and type of board or substrate material being used. The profile shows the actual temperature that should occur on the surface of a test board at or near the central of the solder joint. For this type of reflow soldering, the circuit board and solder joints are first to get heated up. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs thermal energy efficiently and distributes this heat to the components.



Reflow temperature profiles designed for tin/lead alloys will need to be revised accordingly to cater for the melting point of the lead free solder being 34°C (54°F) higher than that of tin/lead eutectic or near-eutectic alloys. In addition, the surface tension of molten lead free solder alloys is significantly higher than the surface tension for tin/lead alloys and this can reduce the spread of lead free solder during reflow.

Lead Free Reflow Profile General Guidelines

i. Ramp 1

Ramp to 100°C. Maximum slope for this zone is limited to 2°C/sec. Faster heating with ramp higher than 2°C may result in excessive solder balling and slump.

ii. Preheat

Preheat setting should range from 100 to 150°C over a period of 60 to 120 seconds depending on the characteristics of the PCB components and the thermal characteristics of the oven. If possible, do not prolong preheat as it will cause excessive oxidation to occur to the solder powder surface.

iii. Ramp 2

The time in this zone should be kept below 35 seconds to reduce the risk of flux exhaustion. The ramp up rate should be 2°C/sec from 150°C to re-flow at 217°C. It is important that the flux medium retains its activity during this phase to ensure the complete coalescence of the solder particles during re-flow.

iv. Reflow

The peak reflow temperature is calculated by adding ~32°C to the melting point of the alloy. Lead free solder paste melts at 218°C and peak reflow temperature is 218°C + 32°C = 250°C (±5°C). Note that total time over 218°C is critical and should typically be 60 – 150 seconds. This period determines the appearance of the solder joints. Excessive time above reflow may cause a dull finish and charred of flux residues. Insufficient time above reflow may lead to poor wetting and improperly fused (cloudy) flux residues.

v. Cooling

Maximum slope for cooling is limited to 3°C/sec. More rapid cooling may cause solder joints crack while cooling at a slower rate will increase the likelihood of a crystalline appearance on the solder joints (dull finish).

PCB Design Guidelines

The recommended ACPM-7886 PCB land pattern is shown in Figure 3. The substrate is coated with solder mask between the I/O and conductive paddle to protect the gold pads from short circuit that is caused by solder bleeding / bridging.

Stencil Design Guidelines

A properly designed solder screen or stencil is required to ensure optimum amount of solder paste is deposited onto the PCB pads. The recommended stencil layout is shown in Figure 4. The stencil has a solder paste deposition opening that is approximately 80% of the PCB pad. Reducing the stencil opening can potentially generate more voids. On the other hand, stencil openings larger than 100% will lead to excessive solder paste smear or bridging across the I/O pads or conductive paddle to adjacent I/O pads. Considering the fact that solder paste thickness will directly affect the quality of the solder joint, a good choice is to use laser cut stencil composed of 0.100mm (4 mils) or 0.127mm (5 mils) thick stainless steel which is capable of producing the required fine stencil outline. The combined PCB and stencil layout is shown in Figure 5.

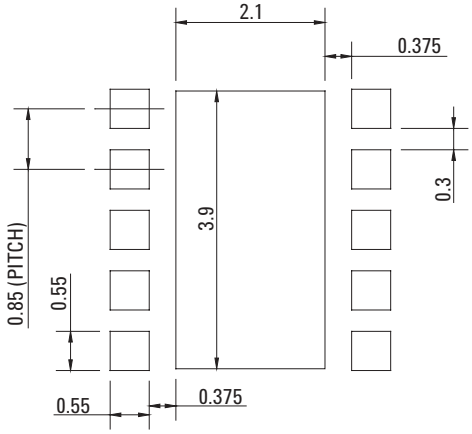


Figure 3. PCB land pattern (dimensions in mm)

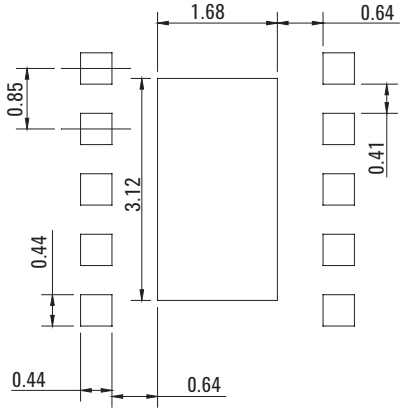


Figure 4. Stencil outline drawing (dimensions in mm)

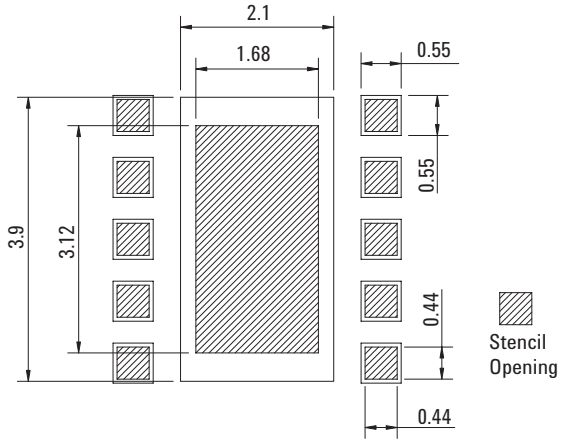


Figure 5. Combined PCB and stencil layouts (dimensions in mm)

Solder Paste Recommendation

The ACPM-7886 package is a lead free package that was proven to pass MSL3 when reflowed under lead free solder reflow profile. The recommended lead free solder for SMT reflow is Sn-Ag-Cu (95.5% Tin, 3.8% Silver, 0.7% Copper) or other similar Sn-Ag-Cu solders. This lead free solder paste has a melting point of 218°C (423°F), the ternary eutectic of Sn-Ag-Cu system, giving it the advantage of being the lowest melting lead free alternative. This temperature is still low enough to protect from damaging the internal circuitry during solder reflow operations provided the exposure time at peak reflow temperatures is not too excessive.

In certain situations, the designer may use leaded solder paste for reflow. The recommended solder for mounting ACPM-7886 package is Sn63 (63% Sn, 37% Pb). It is a eutectic compound with a typical melting point of 183°C.

Application Information

Introduction

The ACPM-7886 amplifier module is designed for TD-SCDMA applications in the 2010-2025MHz band. This power amplifier is able to produce excellent results for the emerging Chinese standard, TD-SCDMA. Typical ACLR performance at Vdd is 41dBc with Pout of 28dBm and 41% efficiency.

Background

In 1999 the China Academy of Telecommunications Technology (CATT) and Siemens proposed a new 3G standard that would rival WCDMA and CDMA2000 data rates. Time Domain Synchronous Code Domain Access (TD-SCDMA) combines both CDMA and TDMA technologies. It benefits from CDMA capacity as well as being compatible with current GSM networks. But unlike existing WCDMA, CDMA2000 and GSM networks, this new standard transmits and receives on the same frequency thus greatly increasing spectrum efficiency. Figure 6 simplifies this explanation by showing one TD-SCDMA frame with 7 slots and 16 channelization codes in each slot.

ACPM-7886 Test Setup

The test setup for measuring a TD-SCDMA power module resembles a GSM test. Specifically, it is very important to properly configure the timing for the test instruments and the device under test. In GSM, in order to turn ON and OFF each time slot, a controlled pin on the PA is triggered with a pulse period of 4.615ms and a 12% duty cycle (577uS). This pin is usually labeled as Vapc on most GSM PAs.

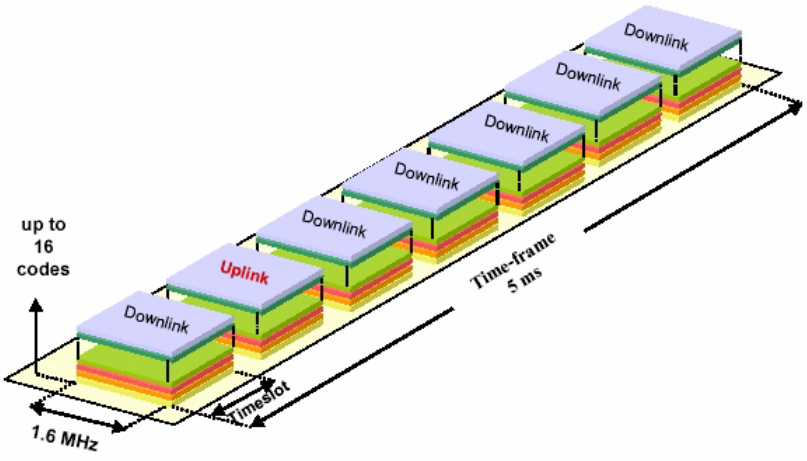


Figure 6. TD-SCDMA frame.[1]

TD-SCDMA uses the same control technique except that each frame is 5ms with only 7 timeslots and an additional 75us downlink pilot and a 125us uplink pilot. Each of the 7 slots is 675uS. For the ACPM-7886, the Vctrl pin is used instead of Vapc. As in GSM, there is a time mask specification that must be met, but conformance to this spec is dictated by the Vapc ramp.

In addition to time domain specs, TD-SCDMA must meet linearity requirement. GSM/GMSK is referred to as constant amplitude or constant envelope modulation, and thus the PAM is allowed to operate in saturation. As shown in Figure 6, each time slot supports 16 different CDMA codes with QPSK modulation; as a result this PA must meet similar ACLR specifications as CDMA or WCDMA.

Signaling Setup

To properly test a TD-SCDMA PA module as specified in the TS25.102 standard, one must generate the RF signal shown in Figure 6 along with the timing described in the previous section.

While at the time of publication of this Application note, Agilent Technologies did not have a TD-SCDMA transceiver or a baseband reference module capable of this signal generation, but it does have the E4438C capable of generating a TD-SCDMA waveform. If used in conjunction with Agilent Technologies E4440A spectrum analyzer and TSM Signal Studio, all performance tests become much simpler although, ACLR, Gain, PAE, Idd and Spurious emission, etc. can be measured with any spectrum analyzer.

Figure 7 shows the basic setup used to test ACPM-7886 for TD-SCDMA. This includes DC power supply, timing and RF signaling. In brief, the signal generator triggers the pulse generator which in turn triggers the spectrum analyzer and the ACPM-7886 and any other multimeters used. The RF signal is created using Signal Studio on a PC and downloaded to the signal generator via GPIB.

Signal Studio [2] facilitates the construction of the complex RF waveform shown in Figure 8. Using this software, one can generate uplink and downlink Dedicated Physical Channel (DPCH) signals along with the uplink and downlink pilot signals. All 7 traffic timeslots are supported, with up to 16 individually configurable code channels per timeslot, for a total of 112 resource units(RU).

Signal Studio for TSM and other standards can be found at: www.agilent.com/find/signalstudio

Figure 8 displays the main configuration window with only 1 downlink timeslot turned on.

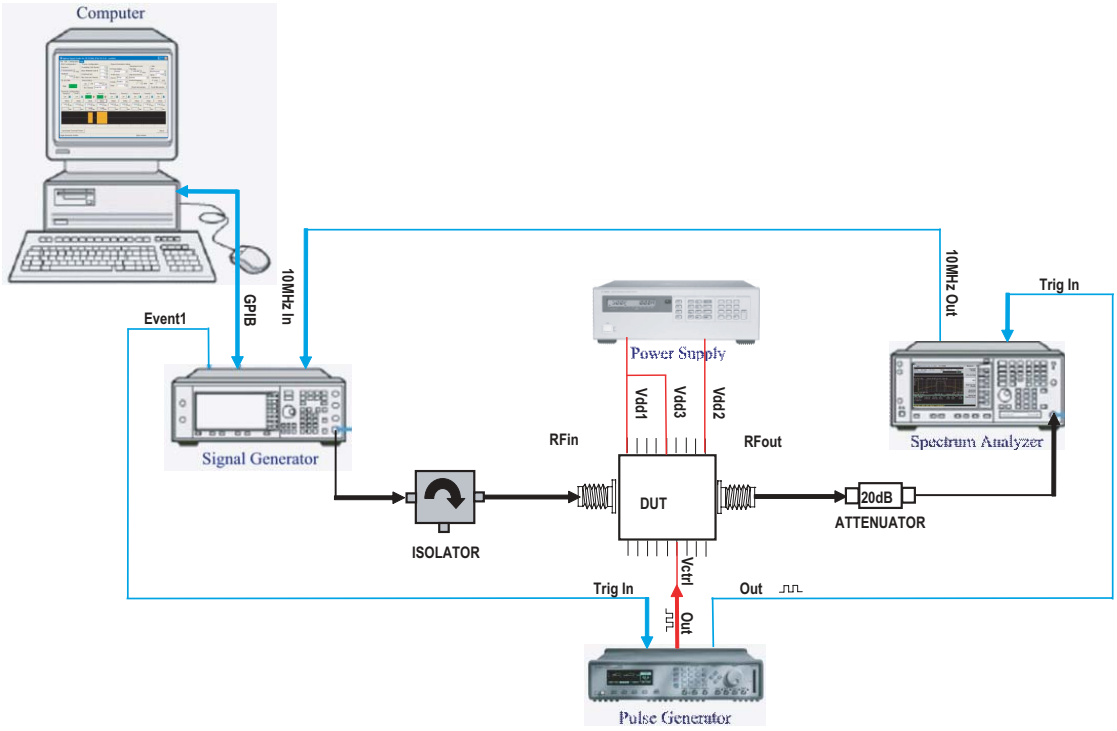


Figure 7. TD-SCDMA test setup.

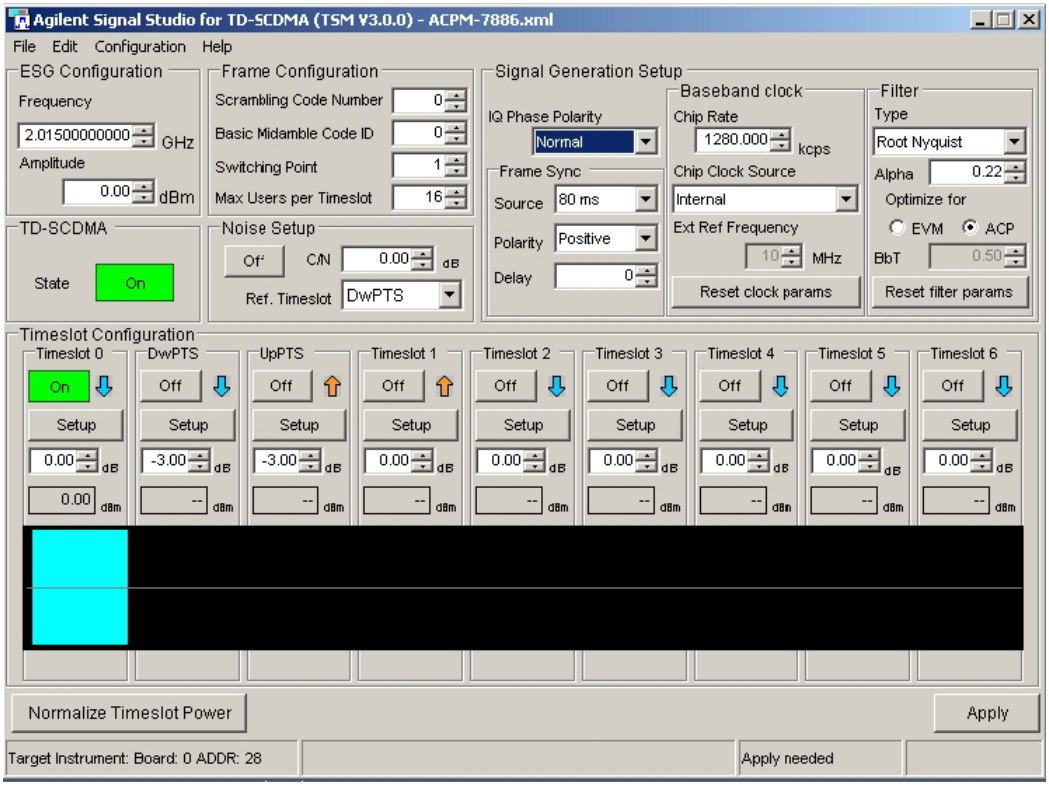


Figure 8. Signal Studio configuration.

Technically the mobile will transmit on the uplink, but the main point is to display the configurability for each slot. In fact, the test for ACPM-7886 does not require the full 16 code channels.

Signal Studio is most beneficial for a base station uplink or downlink test where multiple users will be transmitting on the same time slot. For this test only one time slot is used with a single code.

Results

ACPM-7886 delivers good performance for TD-SCDMA in the 2010 – 2025MHz frequency band see figures 10, 11, and 12. At Vdd of 3.5V, Vdd2 of 2.85 and Vcntl of 2V and Pout of 28dBm this device produces efficiency of 40% and ACLR1/ACLR2 of 41dBc and 56 dBc respectively.

In normal CDMA or WCDMA systems, receiver sensitivity is greatly affected by the TX power leakage, thus the transmit off power is of great importance. Figure 9 shows transmit off power of -83dBm which results in 107dBc of dynamic range.

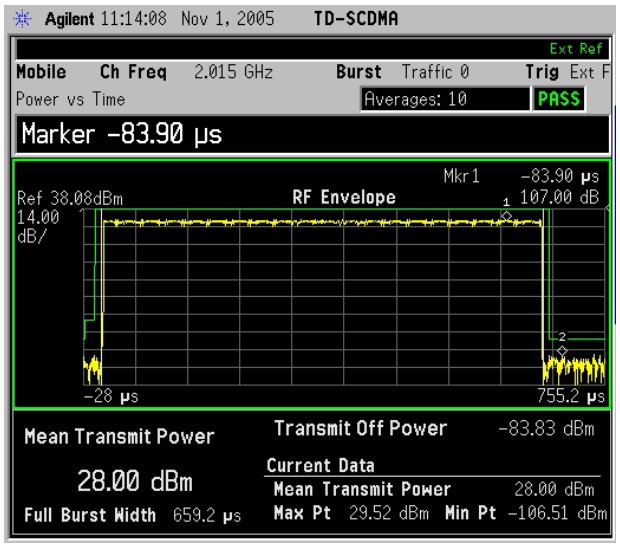


Figure 9. Transmit Off Power.

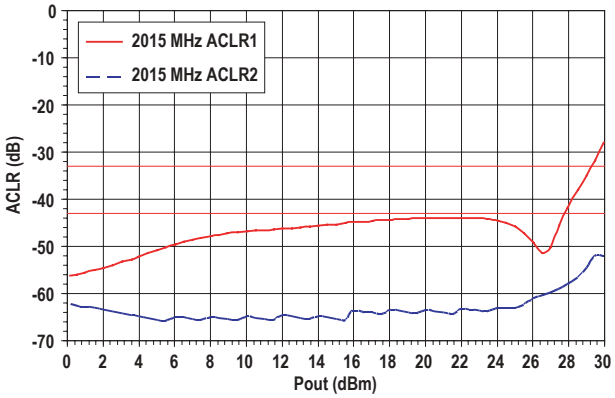


Figure 10. ACLR vs. Pout at 2015 MHz.

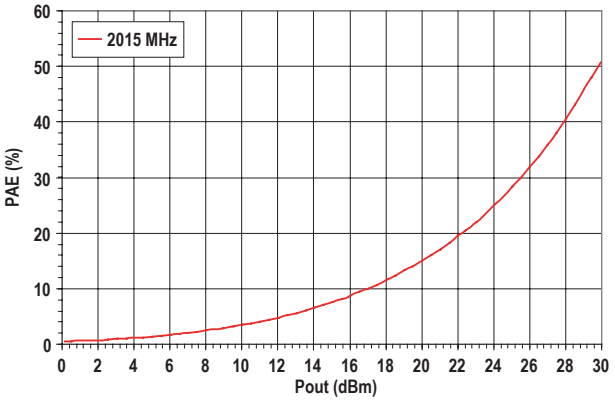


Figure 11. PAE vs. Pout at 2015 MHz.

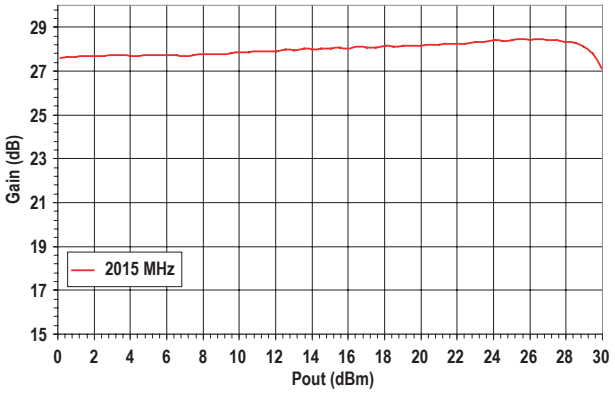


Figure 12. Gain vs. Pout at 2015 MHz.

Summary

Avago Technologies ACPM-7886 has demonstrated excellent performance in the emerging Chinese TD-SCDMA standard. In addition, ACPM-7886 has a proven track record for great results in the UMTS2100 under WCDMA modulation with or without HSDPA. This makes ACPM-7886 ideal for a dual mode/dual band system for the Chinese market.

References

[1] TD-SCDMA: The Solution for TDD Band, Di-Giuseppe, Principato, Fodor, Siemens White Paper 2002

[2] 29 Oct.-Nov. 2005 http://www.agilent.com/find/signalstudio.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

AV01-0319EN - September 1, 2006