

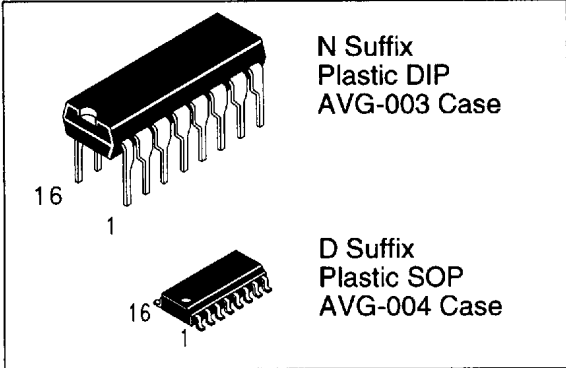
Available Q3, 1995

# Hex D Flip-Flop with Master Reset

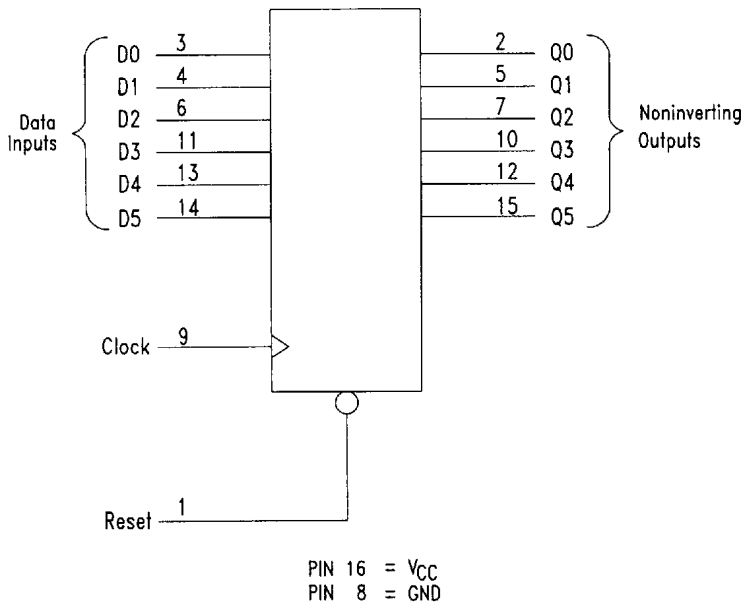
This device is a high speed hex D flip-flop. It is primarily used as a 6-bit edge triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH transition. The device has a Master Reset to simultaneously clear all flip-flops.

- Advanced very high speed CMOS
- Outputs source/sink 24 mA
- Transmission line driving 50 ohms
- ACT has TTL compatible inputs
- Operation from 2 to 6 volts guaranteed
- DC & AC Parameters guaranteed over -40 to +85°C

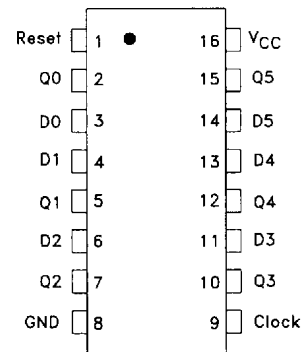
## DV74AC174 DV74ACT174



### LOGIC DIAGRAM



### PIN ASSIGNMENT



### TRUTH TABLE

Inputs			Output
Reset	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q

H=HIGH Voltage Level  
L=LOW Voltage Level  
X=Either Low or High Logic Level  
↑=LOW to HIGH transition of Clock

### ABSOLUTE MAXIMUM RATINGS

Maximum ratings are those values beyond which damage to the device may occur.

Symbol	Parameter	AC174, ACT174	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	- 0.5 to +7.0	V
V <sub>IN</sub>	DC Input Voltage (Referenced to GND)	- 0.5 to V <sub>CC</sub> +0.5	V
V <sub>OUT</sub>	DC Output Voltage (Referenced to GND)	- 0.5 to V <sub>CC</sub> +0.5	V
I <sub>IN</sub>	DC Input Current, per Pin	± 20	mA
I <sub>OUT</sub>	DC Output Sink/Source Current, per Pin	± 50	mA
I <sub>CC</sub>	DC V <sub>CC</sub> or GND Current per Output Pin	± 50	mA
T <sub>STG</sub>	Storage Temperature	- 65 to +150	°C

## GUARANTEED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	
V <sub>CC</sub>	Supply Voltage	'AC	2.0	5.0	6.0	V
		'ACT	4.5	5.0	5.5	
V <sub>IN</sub> , V <sub>OUT</sub>	DC Input Voltage, Output Voltage, (Ref. to GND)	0		V <sub>CC</sub>	V	
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V <sub>CC</sub> @ 3.0 V			150	ns/V
		V <sub>CC</sub> @ 4.5 V			40	ns/V
		V <sub>CC</sub> @ 5.5 V			25	ns/V
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V <sub>CC</sub> @ 4.5 V			10	ns/V
		V <sub>CC</sub> @ 5.5 V			8.0	ns/V
T <sub>A</sub>	Operating Ambient Temperature Range	-40		85	°C	
C <sub>PD</sub>	Power Dissipation Capacitance	V <sub>CC</sub> = 5.0 V		85	pF	
C <sub>IN</sub>	Input Capacitance V <sub>CC</sub> = 5.0 V	V <sub>CC</sub> = 5.0 V		4.5	pF	

1. V<sub>IN</sub> from 30% to 70% V<sub>CC</sub>

2. V<sub>IN</sub> from 0.8 to 2.0 V

## AC — 174

### DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	74AC			Unit		
				T <sub>A</sub> = +25°C		T <sub>A</sub> = -40 to +85°C			
				Typ	Guaranteed Limits				
V <sub>IH</sub>	Minimum High Level Input Voltage	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1 V	3.0	1.5	2.1	2.1	V		
			4.5	2.25	3.15	3.15			
			5.5	2.75	3.85	3.85			
V <sub>IL</sub>	Maximum Low Level Input Voltage	V <sub>OUT</sub> = 0.1V or V <sub>CC</sub> - 0.1 V	3.0	1.5	0.9	0.9	V		
			4.5	2.25	1.35	1.35			
			5.5	2.75	1.65	1.65			
V <sub>OH</sub>	Minimum High Level Output Voltage	I <sub>OUT</sub> = -50 μA	3.0	2.99	2.9	2.9	V		
			4.5	4.49	4.4	4.4			
			5.5	5.49	5.4	5.4			
		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OH</sub>	-12mA	3.0		2.56	2.46	V
				-24mA	4.5		3.86	3.76	
		-24 mA	5.5		4.86	4.76			
V <sub>OL</sub>	Maximum Low Level Output Voltage	I <sub>OUT</sub> = 50 μA	3.0	0.002	0.1	0.1	V		
			4.5	0.001	0.1	0.1			
			5.5	0.001	0.1	0.1			
		V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OH</sub>	12mA	3.0		0.36	0.44	V
				24mA	4.5		0.36	0.44	
		24 mA	5.5		0.36	0.44			
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>I</sub> = V <sub>CC</sub> , GND	5.5		±0.1	±1.0	μA		
I <sub>CC</sub>	Maximum Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5		8.0	80	μA		

174

## AC CHARACTERISTICS

Symbol	Parameter ( $C_L = 50 \text{ pF}$ )	$V_{CC}$ $\pm 10\%$ (V)	AC174					Unit
			$T_A = +25^\circ\text{C}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		
			Min	Typ	Max	Min	Max	
$f_{max}$	Maximum Clock Frequency	3.3 5.0	90 100	100 125		70 100	MHz	
$t_{PLH}$	Propagation Delay Clock to $Q_n$	3.3 5.0	2.0 1.5	9.0 6.0	11.5 8.5	1.5 1.0	12.5 9.5	ns
$t_{PHL}$		3.3 5.0	2.0 1.5	8.5 6.0	11 8.0	1.5 1.0	12.5 9.0	
$t_{PLH}$	Propagation Delay Master Reset to $Q_n$	3.3 5.0	2.5 1.5	9.0 7.0	11.5 9.0	2.0 1.5	12.5 10.5	ns

## AC OPERATING REQUIREMENTS

Symbol	Parameter ( $C_L = 50 \text{ pF}$ )	$V_{CC}$ $\pm 10\%$ (V)	AC174		Unit
			$T_A = +25^\circ\text{C}$	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	
			Guaranteed Minimum		
$t_s$	Setup Time, HIGH or LOW, Dn to Clock	3.3 5.0	6.5 5.0	7.0 5.5	ns
$t_h$	Hold Time, HIGH or LOW, Dn to Clock	3.3 5.0	3.0 3.0	3.0 3.0	ns
$t_w$	Master Reset Pulse Width, LOW	3.3 5.0	5.5 5.0	7.0 5.0	ns
$t_w$	Clock Pulse Width	3.3 5.0	5.5 5.0	7.0 5.0	ns
$t_{rec}$	Recovery Time, Master Reset to Clock	3.3 5.0	2.5 2.0	2.5 2.0	ns

# ACT — 174

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	$V_{CC}$ (V)	ACT174			Unit
				$T_A = +25^\circ\text{C}$		$T_A = -40$ to $+85^\circ\text{C}$	
				Typ	Guaranteed Limits		
$V_{IH}$	Minimum High Level Input Voltage	$V_{OUT} = 0.1\text{V}$ or $V_{CC} - 0.1\text{V}$	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V
$V_{IL}$	Maximum Low Level Input Voltage	$V_{OUT} = 0.1\text{V}$ or $V_{CC} - 0.1\text{V}$	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V
$V_{OH}$	Minimum High Level Output Voltage	$I_{OUT} = -50 \mu\text{A}$	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V
		$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -24\text{mA}$ $-24\text{mA}$	4.5 5.5		3.86 4.86	3.76 4.76	V
$V_{OL}$	Maximum Low Level Output Voltage	$I_{OUT} = 50 \mu\text{A}$	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V
		$V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = 24\text{mA}$ $24\text{mA}$	4.5 5.5		0.36 0.36	0.44 0.44	V
$I_{IN}$	Maximum Input Leakage Current	$V_I = V_{CC}, \text{GND}$	5.5		$\pm 0.1$	$\pm 1.0$	$\mu\text{A}$
$\Delta I_{CCT}$	Additional Max $I_{CC}$ /Input	$V_I = V_{CC} - 2.1\text{V}$	5.5	0.6		1.5	$\text{mA}$
$I_{CC}$	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or $\text{GND}$	5.5		8.0	80	$\mu\text{A}$

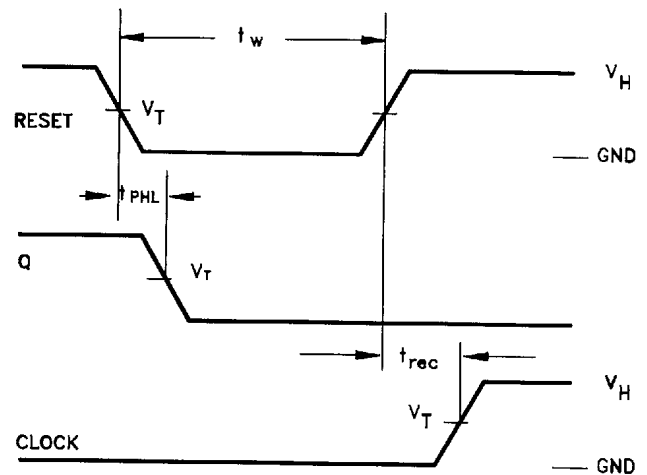
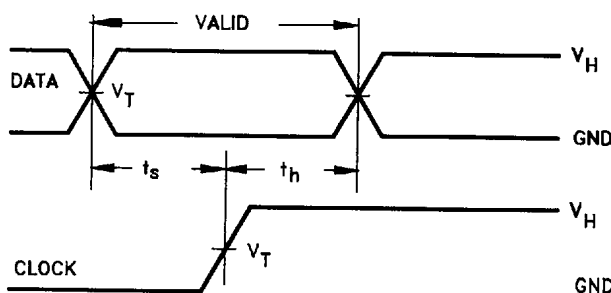
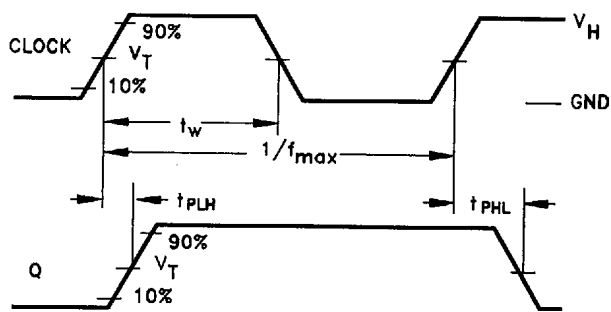
174

## AC CHARACTERISTICS

Symbol	Parameter ( $C_L = 50 \text{ pF}$ )	$V_{CC}$ $\pm 10\%$ (V)	ACT174				Unit
			$T_A = +25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		
			Min	Max	Min	Max	
$f_{max}$	Maximum Clock Frequency	5.0	165		140		MHz
$t_{PLH}$	Propagation Delay, Clock to $Q_n$	5.0	1.5	10.5	1.5	11.5	ns
$t_{PHL}$	Propagation Delay, Clock to $Q_n$	5.0	1.5	10.5	1.5	11.5	ns
$t_{PHL}$	Propagation Delay, Master Reset to $Q_n$	5.0	1.5	9.5	1.5	11.0	ns

Symbol	Parameter ( $C_L = 50 \text{ pF}$ )	$V_{CC}$ $\pm 10\%$ (V)	ACT174		Unit
			$T_A = +25^\circ\text{C}$	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	
			Guaranteed Minimum		
$t_s$	Setup Time, HIGH or LOW, Dn to Clock	5.0	1.5	1.5	ns
$t_h$	Hold Time, HIGH or LOW, Dn to Clock	5.0	2.0	2.0	ns
$t_w$	Master Reset Pulse Width, LOW	5.0	3.0	3.5	ns
$t_w$	Clock Pulse Width	5.0	3.0	3.5	ns
$t_{rec}$	Recovery Time, Master Reset to Clock	5.0	0.5	0.5	ns

## SWITCHING WAVEFORMS



Input and output threshold voltage:  
 $V_T = 50\% V_{CC}$  for AC; 1.5V for ACT  
 $V_H = V_{CC}$  for AC, 3V for ACT

174