L5510

HIGHLY INTEGRATED, AUTOMATED SINGLE-CHIP DRIVE MANAGER AND DISK DRIVE CONTROLLER

DATA BRIEF

1 ATA Host Interface Block

- Synchronous DMA (modes 0-4)
- Fast IDE PIO modes 0-4
- ATA Multiword DMA modes 0-2; supports 60 ns cycle time
- Basic level of ATAPI support
- IORDY for PIO flow control
- Automatic ATA R/W command execution
- Automatic ATA task file updates
- 128-byte host FIFO to/from buffer
- LBA or CHS TASK File Modes
- Read/write cache support with interrupt suppression
- Programmable IRQ automation for different BIOS implementations
- Provides logic for daisy chaining two embedded disk drive controllers
- Full BIOS compatibility
- On-chip selectable 4/8/12 mA host drivers

2 DSP Core

- 60 MIPS operation
- 16-bit, fixed-point DSP
- 16x16-bit, 2's complement parallel multiplier with 32-bit product
- Single-cycle multiply and accumulate
- 36-bit ALU with two 36-bit accumulators
- Bit manipulation unit with 2 additional accumulators
- 6 K words on-chip RAM

3 Buffer Controller Block

- 16-bit wide buffer data bus
- 16 Mbit x 16 SDRAM support; up to 150 Mbyte/s buffer bandwidth
- Automated Data Flow Management (ADFM) automates disk/host transfers
- Dynamic segment size switching
- Auto-Write cache support
- Automatic servo split address adjustment
- Disk LBA counter

4 EDAC Block

- Optimized ECC with up to six burst on-the-fly (OTF) correction
- Programmable 480-bit Reed-Solomon code

Figure 1. Package

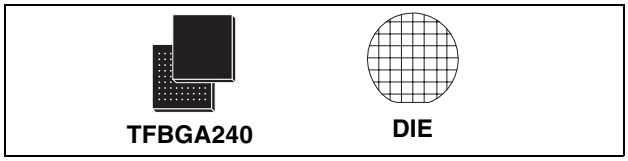

Table 1. Order Codes

Part Number	Package
L5510	TFBGA240
AIC-5465-DIE	DIE

- Programmable 3-, 4-, or 5-way interleaving with 6 to 12 8-bit symbols per interleave
- Optional 3 or 5 byte CRC support
- Guarantee up to 233-bit single burst or six 33-bit bursts OTF correction in <3 sector time
- ECC seeding validating servo and head track position
- AIC-8381 polynomial support for backward compatibility

5 Disk Controller Block

- Enhanced Headerless Architecture (EDSA)
- Up to 450 Mbits/s data rate, byte-wide NRZ
- 31 x 3 byte flexible high-speed RAM- based sequencer
- Defect skipping and/or embedded servo capabilities with Constant Density Recording (CDR)
- 128-byte disk FIFO to/from buffer
- Disk error condition summary bit added to reduce error detection time
- Three-index timer
- MR and PRML channel support

6 Servo Block

- Automatic internal sector mark generation
- Programmable servo burst sequencer
- Programmable servo timing mark sequencer
- Flexible gating and control generation
- User programmable control output pins
- Allows servo format flexibility
- Synchronous servo support

7 Other Features

- 208-pin QFP package
- Automatic and programmed power-down modes
- 3.3 V I/Os with 5 V tolerance, 2.5 V logic core
- Programmable read channel and preamp VCM serial interfaces
- Dual on-chip frequency synthesizers optimize DSP, servo, Ultra-DMA and buffer performance
- General purpose I/O and PWM pins
- Programmable baud-rate RS232 interface

8 DESCRIPTION

The Device is a highly integrated, automated single-chip Drive Manager and Disk Drive Controller IC designed for high-performance, headerless ATA drive applications. Figure 2 shows the chip's main functional blocks.

Figure 2. Functional Block Diagram

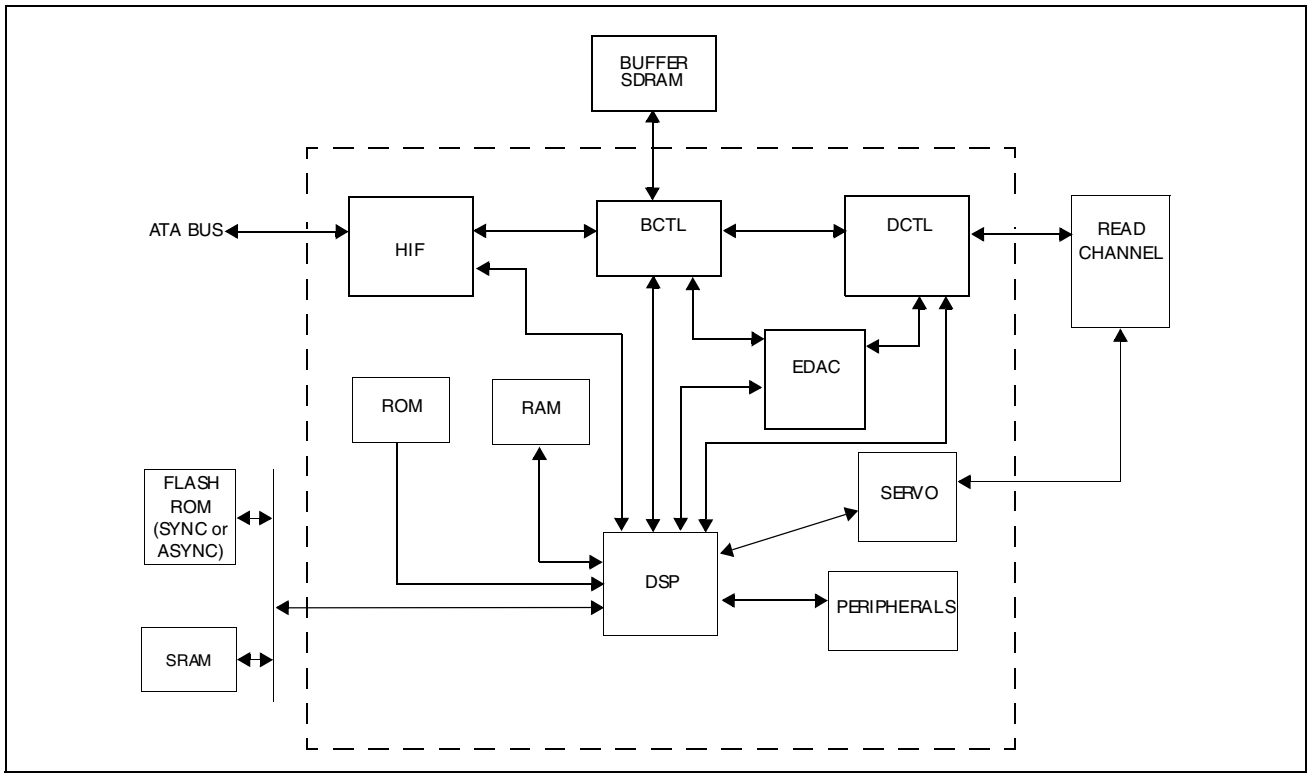

Table 2. Revision History

Date	Revision	Description of Changes
December 2004	1	First Issue