

High-Frequency SPDT Antenna Switch

Description

The CXG1022TM is an antenna switch MMIC. This IC is designed using the Sony's GaAs J-FET process and operates at a single positive power supply with an ultra-small package.

Features

- Single positive power supply operation
- Insertion loss 0.4 dB (Typ.) at 2.0 GHz
- Medium power switching

P1dB (Typ.)	29 dBm	at 2.0 GHz	
			$V_{CTL}(H)=3.0\text{ V}$
	33 dBm	at 2.0 GHz	
			$V_{CTL}(H)=4.0\text{ V}$
- Ultra-small TSSOP package

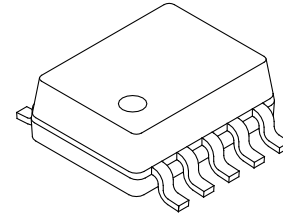
Applications

Antenna switch for digital cordless telephones

Structure

GaAs J-FET MMIC

10 pin TSSOP (Plastic)



Absolute Maximum Ratings (Ta=25 °C)

- | | | | |
|-------------------------|-----------|-------------|----|
| • Control voltage | V_{ctl} | 6 | V |
| • Operating temperature | T_{opr} | -35 to +85 | °C |
| • Storage temperature | T_{stg} | -65 to +150 | °C |

Operating Condition

- | | | | |
|-----------------|--|-----|---|
| Control voltage | | 0/3 | V |
|-----------------|--|-----|---|

Electrical Characteristics

VCTL (L) =0 V, VCTL (H) =3 V, P_{IN}=21.5 dBm

(Ta=25 °C)

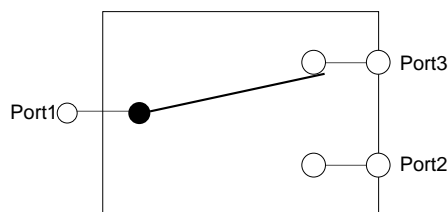
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	
Insertion loss	IL1	f=1.0 GHz		0.3	0.6	dB	
Isolation	ISO1		28	31		dB	
Insertion loss	IL2	f=2.0 GHz		0.4	0.8	dB	
Isolation	ISO2		23	26		dB	
Input VSWR	VSWRIN			1.3	1.5		
Output VSWR	VSWROUT			1.3	1.5		
Switching time	TSW			50		ns	
Control pin current	I _{CTL}				50	100	μA

VCTL (L) =0 V, f =2.0 GHz, R_{RF}=200 kΩ

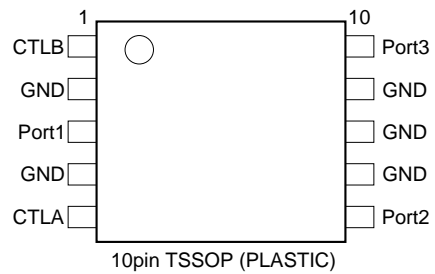
(Ta=25 °C)

1 dB gain compression point output	P1dB (3)	VCTL (H) =3 V	26	29		dBm
1 dB gain compression point output	P1dB (4)	VCTL (H) =4 V	30	33		dBm

Block Diagram

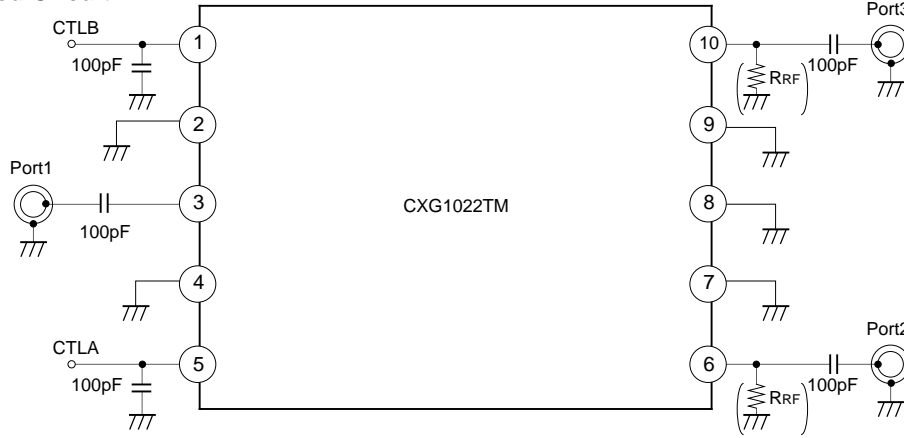


Pin Configuration



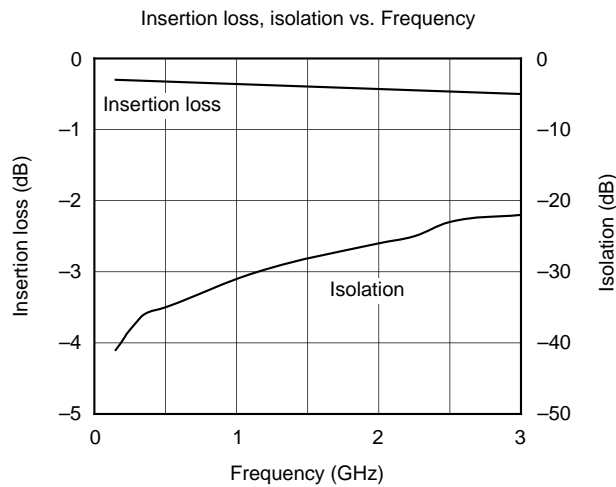
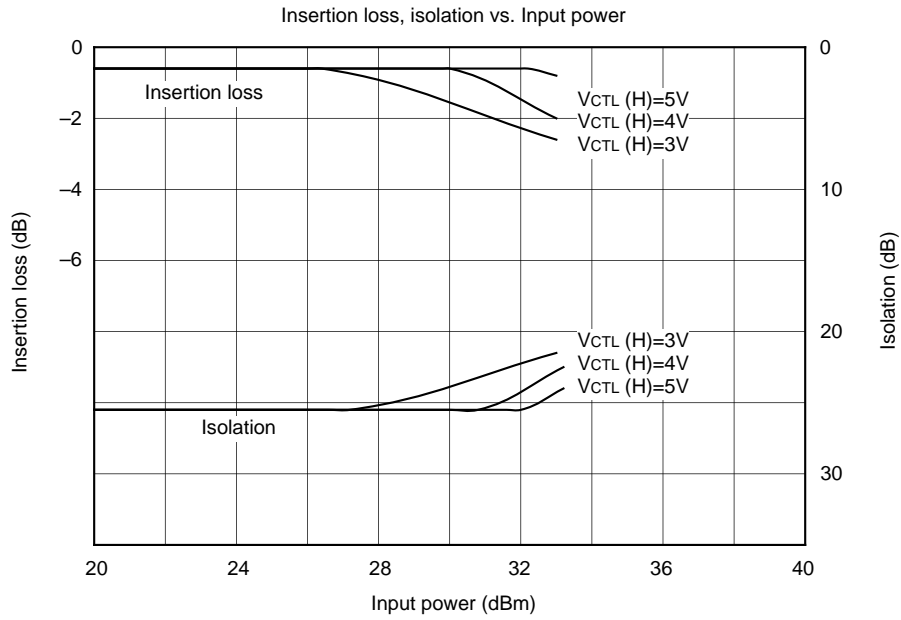
V _{CTLA}	V _{CTLB}	
High	Low	Port1-Port2 ON Port1-Port3 OFF
Low	High	Port1-Port2 OFF Port1-Port3 ON

Recommended Circuit



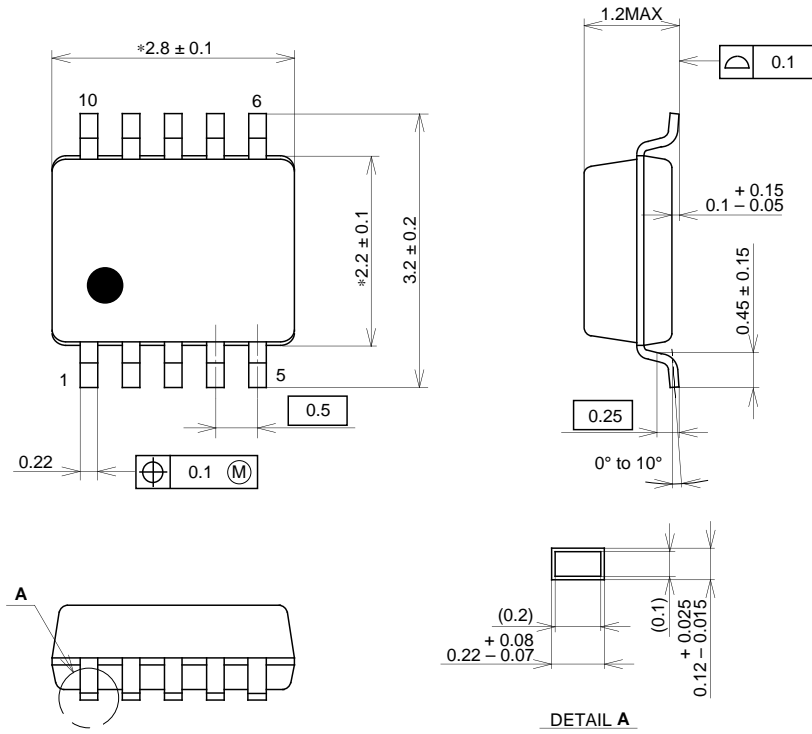
* RRF (200kΩ) is used to stabilized the electrical characteristics at high power signal input

Example of Representative Characteristics (Ta=25 °C)



Package Outline Unit : mm

10PIN TSSOP(PLASTIC)



NOTE: "*" Dimensions do not include mold protrusion.

PACKAGE STRUCTURE

SONY CODE	TSSOP-10P-L01
EIAJ CODE	_____
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.02g