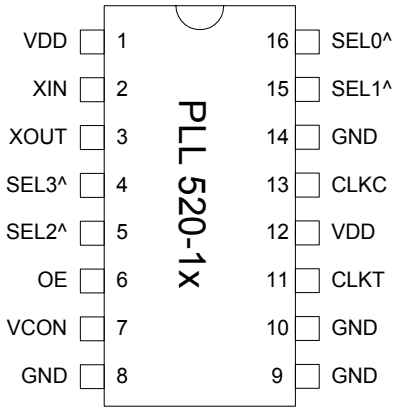
PLL520-17/-18/-19

Low Phase Noise VCXO with multipliers (for 65-130MHz Fund Xtal)

FEATURES

- 65MHz to 130MHz Fundamental Mode Crystal.
- Output range: 65MHz – 800MHz (selectable 1x, 2x, 4x and 8x multipliers).
- Low Injection Power for crystal 50uW.
- Available outputs: PECL, LVDS, or CMOS.
- Integrated variable capacitors.
- Supports 3.3V-Power Supply.
- Available in 16 pin (TSSOP or SOIC)

PIN CONFIGURATION



^: Internal pull-up

DESCRIPTION

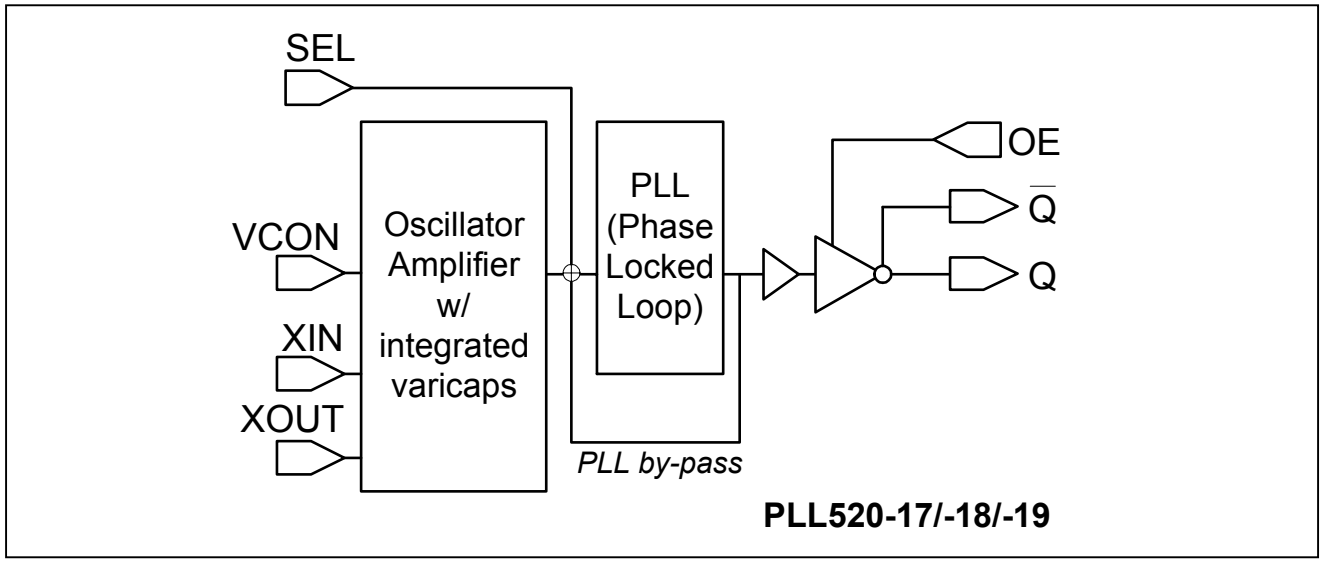
The PLL520-17/-18/-19 family of VCXO IC's is specifically designed to pull high frequency fundamental crystals. They achieve very low current into the crystal resulting in better overall stability. Their internal varicaps allow an on chip frequency pulling, controlled by the VCON input.

OUTPUT ENABLE LOGICAL LEVELS

Part #	OE	State
PLL520-18	0 (Default)	Output enabled
	1	Tri-state
PLL520-17 PLL520-19	0	Tri-state
	1 (Default)	Output enabled

OE input: Logical states defined by PECL levels for PLL520-18
Logical states defined by CMOS levels for PLL520-17/-19

BLOCK DIAGRAM



Low Phase Noise VCXO with multipliers (for 65-130MHz Fund Xtal)

PIN DESCRIPTIONS

Name	Number	Type	Description
XIN	2	I	Crystal input. See Crystal Specification on page 3.
XOUT	3	I	Crystal output. See Crystal Specification on page 3.
OE	6	I	Output enable. See Output Enable Logic Levels on page 1.
VCON	7	I	Voltage control input.
GND	8,9, 10, 14	P	Ground.
CLKT	11	O	True output PECL (PLL520-18) or LVDS (PLL520-19). No Connect for CMOS (PLL520-17).
CLKC	13	O	Complementary output PECL (PLL520-18) or LVDS (PLL520-19). CMOS output for (PLL520-17).
SEL	4,5,15,16	I	Multiplier selector pins. These pins have an internal pull-up that will default SEL to '1' when not connected to GND.
VDD	1, 12	P	+3.3V power supply.

FREQUENCY SELECTION TABLE

Pin #4 SEL3	Pin #5 SEL2	Pin #15 SEL1	Pin #16 SEL0	Selected Multiplier
0	0	1	1	Fin x 8
1	0	1	1	Fin x 4
1	1	1	0	Fin x 2
1	1	1	1	No multiplication

All pins have internal pull-ups (default value is 1). Connect to GND to set to 0.

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* **Note**: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

2. Crystal Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
Built-in Capacitance	CX+	65MHz to 130MHz (VDD=3.3V)		2	pF
	CX-			2	
Inter-electrode capacitance	C_0			2	
C0/C1 ratio (gamma)	γ			300	-
Oscillation Frequency	OF	Fund.	120	200	MHz

3. Voltage Control Crystal Oscillator

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VCXO Stabilization Time *	$T_{VCXOSTB}$	From power valid			10	ms
VCXO Tuning Range		F_{XIN} = 100 – 200MHz; XTAL C_0/C_1 < 250 0V ≤ VCON ≤ 3.3V		200*		ppm
CLK output pullability		VCON=1.65V, ±1.65V	±100*			ppm
On-chip Varicaps control range		VCON = 0 to 3.3V		4 – 18*		pF
Linearity					10*	%
VCXO Tuning Characteristic				65		ppm/V
VCON input impedance				60		kΩ
VCON modulation BW		0V ≤ VCON ≤ 3.3V, -3dB	25			kHz

Note: Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits.

4. General Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current (Loaded Outputs)	I_{DD}	PECL/LVDS/CMOS			100/80/40	mA
Operating Voltage	V_{DD}		2.97		3.63	V
Output Clock Duty Cycle		@ 1.4V (CMOS) @ 1.25V (LVDS) @ Vdd – 1.3V (PECL)	45 45 45	50 50 50	55 55 55	%
Short Circuit Current				±50		mA

5. Jitter Specifications

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Period jitter RMS	77.76MHz		2.5		ps
	155.52MHz		4		
	622.08MHz		5		
Period jitter peak-to-peak	77.76MHz		24		ps
	155.52MHz		29		
	622.08MHz		32		
Integrated jitter RMS	Integrated 12 kHz to 20 MHz at 77.76MHz		0.5		ps
	Integrated 12 kHz to 20 MHz at 155.52MHz		1.5		
	Integrated 12 kHz to 20 MHz at 622.08MHz		1.5		

6. Phase Noise Specifications

PARAMETERS	FREQUENCY	@10Hz	@100Hz	@1kHz	@10kHz	@100kHz	UNITS
Phase Noise relative to carrier	77.76MHz	-75	-95	-125	-145	-155	dBc/Hz
	155.52MHz	-75	-95	-120	-125	-123	
	622.08MHz	-75	-95	-115	-118	-115	

Note: Phase Noise measured at VCON = 0V

7. CMOS Output Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output drive current (High Drive)	I_{OH}	V_{OH}= V_{DD}-0.4V, V_{DD}=3.3V	30			mA
	I_{OL}	V_{OL} = 0.4V, V_{DD} = 3.3V	30			mA
Output drive current (Standard Drive)	I_{OH}	V_{OH}= V_{DD}-0.4V, V_{DD}=3.3V	10			mA
	I_{OL}	V_{OL} = 0.4V, V_{DD} = 3.3V	10			mA
Output Clock Rise/Fall Time (Standard Drive)		0.3V ~ 3.0V with 15 pF load		2.4		ns
Output Clock Rise/Fall Time (High Drive)		0.3V ~ 3.0V with 15 pF load		1.2		

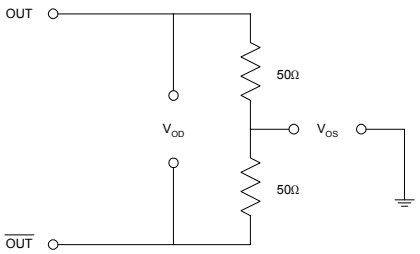
8. LVDS Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Differential Voltage	V_{OD}	R_L = 100 Ω (see figure)	247	355	454	mV
V_{DD} Magnitude Change	ΔV_{OD}		-50		50	mV
Output High Voltage	V_{OH}			1.4	1.6	V
Output Low Voltage	V_{OL}		0.9	1.1		V
Offset Voltage	V_{OS}		1.125	1.2	1.375	V
Offset Magnitude Change	ΔV_{OS}		0	3	25	mV
Power-off Leakage	I_{OXD}	V_{out} = V_{DD} or GND, V_{DD} = 0V		±1	±10	uA
Output Short Circuit Current	I_{OSD}			-5.7	-8	mA

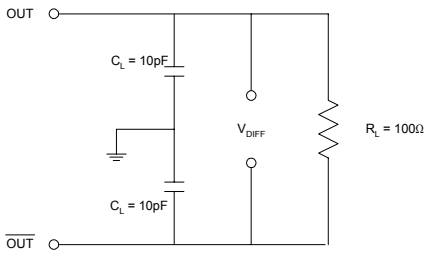
9. LVDS Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Clock Rise Time	t_r	R_L = 100 Ω, C_L = 10 pF (see figure)	0.2	0.7	1.0	ns
Differential Clock Fall Time	t_f		0.2	0.7	1.0	ns

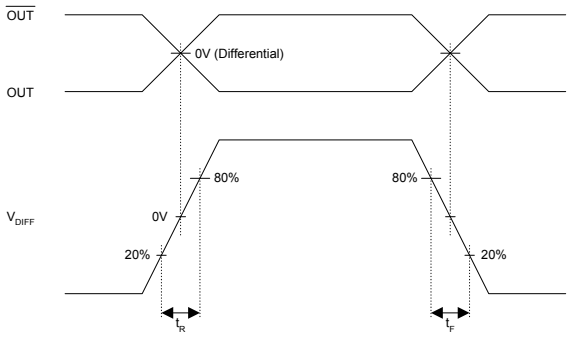
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transistion Time Waveform



Low Phase Noise VCXO with multipliers (for 65-130MHz Fund Xtal)

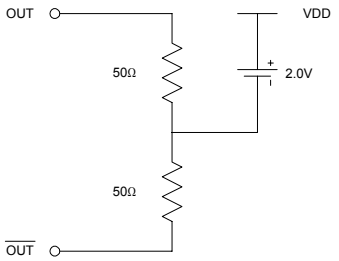
10. PECL Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
Output High Voltage	V_{OH}	R_L = 50 Ω to (V_{DD} – 2V) (see figure)	V_{DD} – 1.025		V
Output Low Voltage	V_{OL}			V_{DD} – 1.620	V

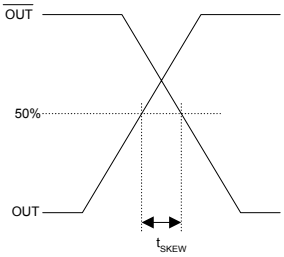
11. PECL Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Clock Rise Time	t_r	@20/80% - PECL		0.6	1.5	ns
Clock Fall Time	t_f	@80/20% - PECL		0.5	1.5	ns

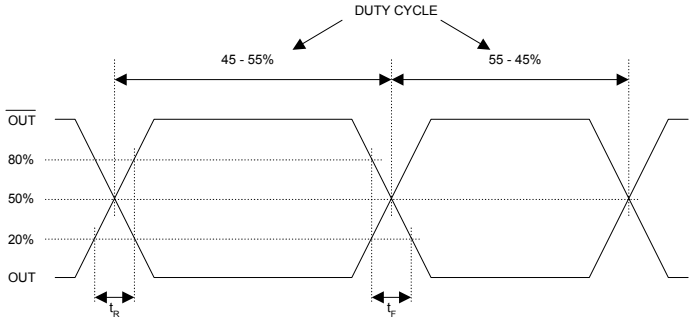
PECL Levels Test Circuit



PECL Output Skew



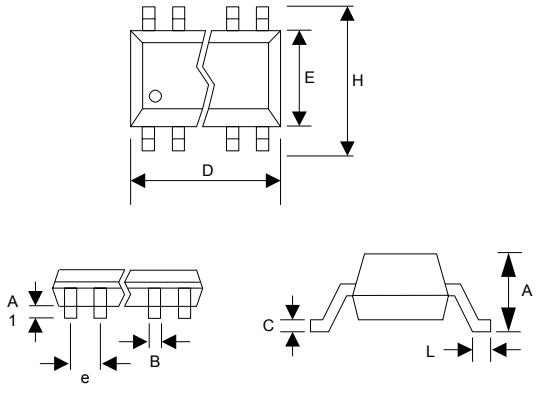
PECL Transistion Time Waveform



PACKAGE INFORMATION

16 PIN Narrow SOIC, TSSOP (mm)

	SOIC		TSSOP	
Symbol	Min.	Max.	Min.	Max.
A	1.35	1.75	-	1.20
A1	0.10	0.25	0.05	0.15
B	0.33	0.51	0.19	0.30
C	0.19	0.25	0.09	0.20
D	9.80	10.00	4.90	5.10
E	3.80	4.00	4.30	4.50
H	5.80	6.20	6.40 BSC	
L	0.40	1.27	0.45	0.75
e	1.27 BSC		0.65 BSC	



Low Phase Noise VCXO with multipliers (for 65-130MHz Fund Xtal)

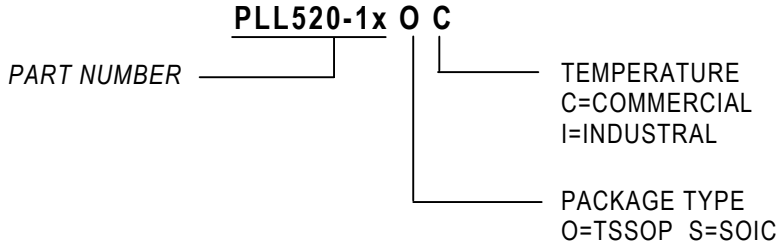
ORDERING INFORMATION

For part ordering, please contact our Sales Department:

47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range



Order Number	Marking	Package Option
PLL520-17OC	P520-17OC	TSSOP – Tube
PLL520-17OC-R	P520-17OC	TSSOP – Tape & Reel
PLL520-17SC	P520-17SC	SOIC – Tube
PLL520-17SC-R	P520-17SC	SOIC – Tape & Reel
PLL520-18OC	P520-18OC	TSSOP – Tube
PLL520-18OC-R	P520-18OC	TSSOP – Tape & Reel
PLL520-18SC	P520-18SC	SOIC – Tube
PLL520-18SC-R	P520-18SC	SOIC – Tape & Reel
PLL520-19OC	P520-19OC	TSSOP – Tube
PLL520-19OC-R	P520-19OC	TSSOP – Tape & Reel
PLL520-19SC	P520-19SC	SOIC – Tube
PLL520-19SC-R	P520-19SC	SOIC – Tape & Reel