CONSUMER MICROCIRCUITS LTD

PRODUCT INFORMATION

Obsolete Product
- For Information Only -

MULTI-PURPOSE FREQUENCY SENSITIVE SWITCH

FX-101L

GENERAL DESCRIPTION

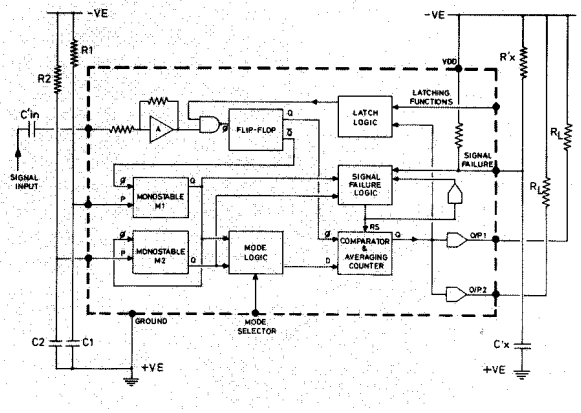
The FX-101L is a high performance frequency sensitive switch constructed in monolithic form using MOS/MSI techniques. It is a pin and function compatible equivalent of the standard CML FX-101, but offers improved accuracy and operates from lower voltage supplies. The FX-101L is the preferred version for new equipment and systems in the course of planning, and in many cases can be employed as a direct plug-in replacement for the FX-101 in existing applications.

The FX-101L accepts sinewave or pulse input signals and operates an integral semiconductor switch when the input frequency reaches an accurately predetermined value. By simply grounding or 'floating' a control input pin the FX-101L may be arranged to switch 'ON' when the input frequency lies anywhere above a single datum value (Datum Mode) or, alternatively, within a preset band of values (Band Mode). The switch set points may be varied over a wide range of frequencies according to the values of two external resistors and two capacitors. Set point stability is of a high order and is maintained over the entire specified range of supply voltages and operating temperatures. Set point thresholds are extremely sharp and yield an effective 'Q' factor exceeding 1,000; the FX-101L also exhibits a fast response time combined with exceptional immunity to turn-on by random signal noise.

In addition to the Datum/Band functions the FX-101L has control inputs which allow a choice of 'Latch or Unlatched' switch operation, which includes 'Latch to on' or 'Latch to off' in the latch mode. Further facilities include, direct switch reset, and selection of Fail Safe (switch OFF), delayed Fail Safe or Ignore (hold state) switching options in the event of signal interruption. Function control inputs are high impedance and may be operated by external logic levels.

The FX-101L is housed in a 10 lead TO-100 style package and operates from a single wide tolerance D.C. supply of − 8V to − 15V, over the extended temperature range.

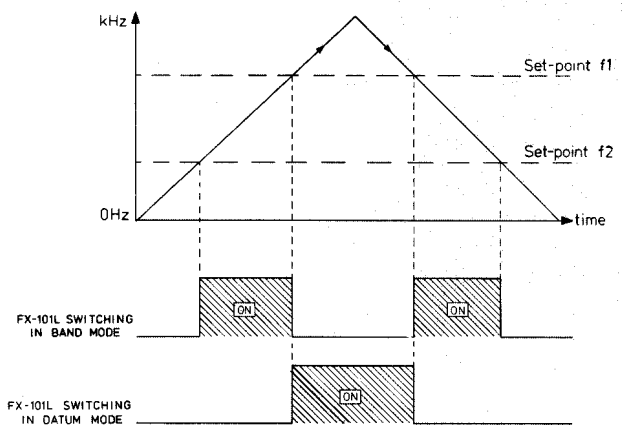
FIG.1 SIMPLIFIED BLOCK DIAGRAM FX-101L



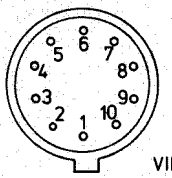
OUTSTANDING FEATURES

- DATUM OR BAND SWITCHING
- ADJUSTABLE SWITCH FREQUENCIES
- HIGH STABILITY SET POINTS
- NARROW BAND/WIDE BAND SWITCHING
- SINE OR PULSE SIGNAL INPUT
- SWITCH LATCHING OPTIONS

FIG.2 FX-101L SWITCH STATE vs INPUT FREQUENCY



TO-100 STYLE PACKAGE FIG.3



10 Leads 0·038" dia.
by 0·515" long.
Equispaced on 0·23" PCD

VIEW ON PINS

PIN DATA

1. SIGNAL INPUT	6. +VE SUPPLY
2. SIGNAL FAILURE RECOGNITION	7. -VE SUPPLY
3. LATCH FUNCTIONS	8. SET f1
4. SWITCH OUTPUT No.1	9. MODE SELECTOR
5. SWITCH OUTPUT No.2	10. SET f2

Note: Pin 6 is internally connected to the case.

OPERATING PRINCIPLE

The tone recognition system employed by the FX-101L is based on a period sampling technique. Input signals are amplified and shaped to provide clock signals to the bistable flip-flop, the output of which is a square wave having a period equal to the interval between successive input waveform 'zero-crossings'.

The flip-flop output triggers a monostable (M1) which generates a reference period corresponding to $\frac{1}{f1}$, where f1 (Hz) represents the Datum mode set-point, or the upper edge of the Band mode tone accept channel. At the expiry of M1 period, monostable M2 is triggered; the *summed* periods M1 + M2 corresponding to $\frac{1}{f2}$, the lower edge of the tone accept channel.

The reference periods are compared against the signal input period in a comparator, the output of which controls a special counter/storage system. This counting system discriminates against random spurious information and delivers an output only when a number of sampled periods have a true average value falling within the 'tone accept' limits. The output of the counter system, which is continuously monitoring the input information, is applied to the output buffer switches. Gating circuits are incorporated which prevent false operation when harmonics of the tone frequency are applied.

This unique and patented tone recognition system yields extremely sharp tone channel definition, coupled with a fast response time and high immunity to false turn-on due to outband noise, regardless of the noise frequency and amplitude. The period sampling system requires, however, a 'regular' input waveform for correct operation. Input noise can, if mixed with the required inband tone, prevent the circuit from recognising that the tone is present. This effect is produced because the noise 'jitters' the interval between successive signal zero-crossings and the comparator/counter rejects the information as not being consistent with an input signal having a frequency actively within the tone channel limits.

If the noise is *random* in nature, e.g. spurious noise spikes or short term interference (short in relation to the device recognition time, or inband tone duration) it will have little or no effect other than possibly to increase the overall tone recognition time by a few cycles. If the noise is *continuous,* e.g. parallel inband and outband tones are on the signal line simultaneously, the device will not recognise the inband tone. If the noise is semi-continuous, e.g. speech signals, increasing the inband tone duration will allow the tone to be recognised during a momentary 'noise' pause.

The device is therefore ideal for use when inband tones are transmitted individually, or sequentially, but operation in parallel-tone signalling schemes is not recommended, unless adequate pre-filtering is used.

GENERAL CIRCUIT OPERATION

Fig. 2 illustrates the switching functions performed by the FX-101L. The relationship between the signal input frequency and the output switch state is shown for Band and Datum operating modes. Two in-phase switches are provided. The logic level applied to pin 9, the mode selector input, determines which operating mode is obtained, the logic truth table is shown in fig. 4.

When Band mode is selected, signal frequencies lying within the limits f1 to f2 will turn the output switches ON; signals lying 'outband', either above f1 or below f2, will turn the switches OFF.

If Datum mode is used, signal frequencies higher than set-point f1 turn the switches ON and signals below f1 turn the switches OFF. Note that set-point f2 is inactive when Datum mode is in use, but components R2/C2 must still be fitted to ensure correct operation of the circuit. A convenient rule in these circumstances is to make f2 a 'ghost' value at a nominal 10% *below* f1 (see also the notes on Response Time).

Set-point 'definition', i.e. hysterisis, is extremely sharp; values of 0.1% of set-point frequency are typical.

A 'Signal Failure' recognition facility is incorporated in the circuit which allows a choice of switch actions in the event that the input signals are cut-off instantaneously. (See notes on Signal Failure Recognition).

Fig. 4 shows the latching options available by applying logic levels to pin 3.

Grounding pin 3 enables the switch to work in the 'unlatched' mode; in this mode the switch turns ON & OFF according to the input frequencies applied, and the switch therefore reflects the current relationship between the signal frequency and the set-point frequencies.

Latch to OFF mode is obtained by open-circuiting pin 3 whilst the switch is in the ON condition. Open-circuiting the pin has no direct effect on the switch state, but if the switch is subsequently turned OFF by the signal frequency it will latch in the OFF state, e.g. it will not turn ON again when the signal frequency reverts to an ON value.

To reset the switch, the frequency must be returned to an ON value *and* pin 3 momentarily grounded. It is only necessary to ground the pin for a period equal to the device response time, it may then be open-circuited again ready for a further latch action.

To obtain the Latch to ON function, pin 3 must be grounded (logic 'O') and a diode connected between pins 4 and 8 as shown in Fig.4. If a load is also connected to pin 4, the load current should be such that the maximum 'O' level (switch ON) at pin 4 is -2v. To reset the Latch, the signal must first be returned to an OFF value, or zero, and the diode link momentarily broken. As an alternative to breaking the link, the diode may be reverse biased by momentarily connecting pin 4 to VDD (-ve) via a 470 Ω limiting resistor.

FIG.4 TRUTH TABLES FX-101L

MODE SELECTOR PIN 9	OUTPUT SWITCHING MODE
1	BAND SWITCHING BETWEEN f1 & f2
0	DATUM SWITCHING AT SET-POINT f1

CONTROL INPUT PIN 3	OUTPUT LATCH FUNCTIONS
0	UNLATCHED
1	LATCH TO OFF
0 & link as shown (4)–▷–(8)	LATCH TO ON

LOGIC '1' = OPEN CIRCUIT LOGIC '0' = +VE SUPPLY (GROUND)

OUTPUT SWITCH CHARACTERISTICS

The standard output switches used in the FX-101L are MOS driver transistors connected between each output pin and the ground pin (+ve). No internal load is provided, therefore the only potentials present any output pin are those provided by the external load. Low current loads may be directly connected between the output pin and -ve supply, high current loads should be operated through a buffer transistor.

When the switch is turned ON, it becomes a low resistance path (value = R'on) connecting the output pin to ground, (see Fig.5). When the switch is turned OFF, it exhibits a high resistance (10MΩ minimum), effectively open-circuiting the output pin. The switch has a 'jitter-free' snap action; typical OFF-ON transition times are in the order of 2 micro-seconds.

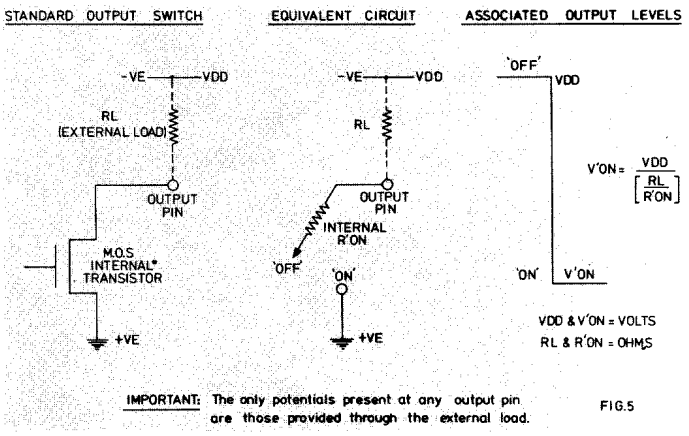


FIG.5

SUPPLY NOTES

References to ground, logic 'O' and logic 'I' in this data sheet are based on the use of a grounded positive supply, i.e. HT (VDD) is negative. A logic 'I' level is therefore near VDD (-ve) and a logic 'O' level near ground (+ve). There is, however, no objection to operation with the -ve supply grounded, but reference to logic *polarities* remain unchanged, i.e. a logic 'I' is *always* -ve with respect to a logic 'O'.

Example: a) V_{DD} = -12 +ve = ground
logic 'I' = -12V and logic 'O' = ground.

b) V_{DD} = OV +ve = + 12V
logic 'I' = OV and logic 'O' = + 12V

Note also that the case is internally connected to the +ve pin and will therefore be above ground potential if VDD = OV. It is also important to ensure that no pin receives a potential which is positive with respect to the +ve supply pin. Failure to observe this rule may result in damage to the device.

SIGNAL INPUT NOTES

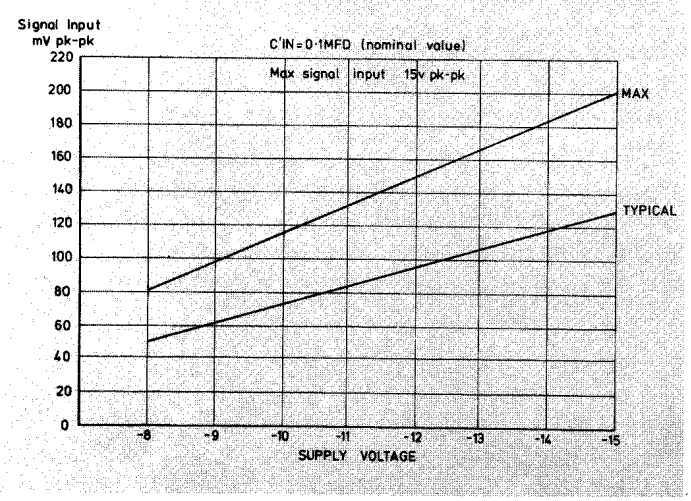
The FX-101L incorporates a signal input amplifier offering a high input impedance. The amplifier is designed using negative feedback principles and therefore the input is D.C. self-biased. Signals to the input pin should normally be A.C. coupled to avoid disturbing this bias point. High level pulse signals ($\geqslant$ -6V) may be directly coupled. The actual shape of the signal waveform is not important and may be sine, square or pulse in form.

Input impedance is typically 50kΩ at mid-range supply voltages. This value varies with supply voltage and production tolerances, and a total spread of 25kΩ to 200kΩ should be assumed. The minimum value of the input coupling capacitor (C'in) depends on the frequency of set-point f'2 and must be large enough to yield a time constant product:

$$C'in \times Z in\ (MFD \times M\Omega) \geqslant \frac{1}{f2\ (Hz)}$$

Fig. 6 shows the production spread of input signal sensitivity versus supply voltage. If overvoltages and transients are likely to occur on the signal line, a protective diode clamp should be used to limit input voltages to the maximum permitted levels.

FIG.6 SIGNAL SENSITIVITY versus SUPPLY VOLTAGE



SWITCH RESPONSE TIME (T_S)

The response time (T_S) of the FX-101L is defined as the interval between the input frequency crossing a set-point threshold and the output switches changing state. This interval is normally equal to approximately 10 cycles of the input frequency $\left(\frac{10}{f'in}\right)$, but this will be increased if the frequency difference between set-points f1 and f2 exceed 2:1, e.g. Bandwidth (BW) $\geqslant$ 50%.

Response time may also be increased if random noise impulses are superimposed on the input signals.

Excluding input noise effects, response time is expressed:

$$T_S\ (min) \approx \frac{10}{f1\ (Hz)}\ Seconds,\ where\ f1 < 2f2$$

$$T_S\ (max) \approx \frac{10}{f2\ (Hz)}\ Seconds,\ where\ f1 \geqslant 2f2$$

The frequency of set-point f2 should be taken into account regardless of whether it is an operating set-point, as in Band Mode, or a 'ghost' set-point, as in Datum Mode.

Fig. 7 shows the effect of response time T_S when the input signal changes from outband to inband and vice-versa, as in FSK signalling. The same characteristics apply when signals change from Low to High using Datum Mode. From this it is seen that T_S is a constant factor for frequency shifts in either direction, provided not less than 10 cycles of input signal are received after the frequency crosses a set-point threshold.

If the input signal changes instantly from inband to OHz, e.g. 10 cycles of outband signals are not received, a modified response time T_{FS} will elapse before the outputs switch to the OFF state.

SIGNAL FAILURE RECOGNITION (T_{FS})

As the FX-101L is essentially a digital device the internal circuits come to rest when no input signals are present. If an instantaneous signal cut-off occurs while the switch is in the ON state it will remain ON until a signal which turns it OFF is received. In applications where the signal is a continuously variable value, any absence of signals is usually preceded by a frequency run-down through a set-point and the switch is therefore OFF when signals cease. In some applications, however, an OFF value signal may not always be available and the input to pin 2 provides facilities for automatic 'no signal/no OFF signal' turn-off.

With pin 2 connected to ground (+ve), the switch ignores signal interruptions and will turn ON or OFF only in response to defined input signal frequencies.

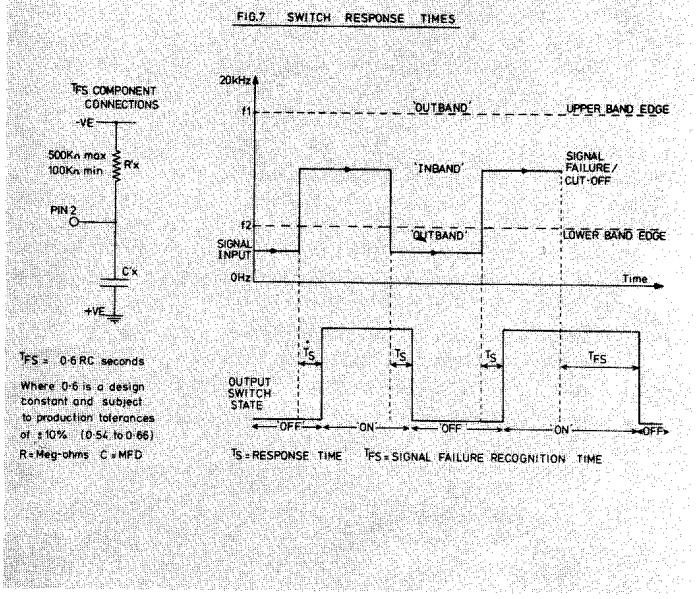
To obtain automatic switch to OFF, should input signals fail, pin 2 should be connected to a CR network (C'x, R'x) as shown in Fig. 7. If the output switches are ON and input signals are cut-off, the capacitor charges to a preset level which forces the output switches to OFF. The capacitor is then automatically discharged. The Signal Failure Recognition time T_{FS} (Fig.7) can be adjusted to allow planned signal breaks to be ignored, but ensures that the switch adopts the OFF state if a true signal failure occurs.

For general purpose applications a convenient value for T_{FS} is $\frac{10}{f2\ (Hz)}$ seconds, which yields a period T_{FS} approximately equal to the normal response time T_S. Whilst T_{FS} can be set to almost any required longer delay time, it should never be made less than $\frac{2}{f2\ (Hz)}$ seconds: if it is too short, the interval between successive input signal samples may be mistaken for 'LO Signal' and the output switches will be held permanently OFF.

To maintain T_{FS} accuracy, R'x is limited to the range 100kΩ to 500kΩ. This is due to an internal pull-up resistor on pin 2, which shunts R'x and modifies its effective value. This internal resistor has a nominal value of 4MΩ, but this is subject to production tolerances and also varies with supply voltage.

Pin 2 may also be used as a Direct Reset which switches the outputs to the OFF state, over-riding the input signal. If pin 2 is open-circuited, the internal pull-up resistor applies a reset voltage to the output switch stages. This resets the switches to an OFF state in a maximum time $\frac{1}{f2\ (Hz)}$ seconds. Note that the output switches will be held permanently OFF if pin 2 is accidentally left open-circuit.

FIG.7 SWITCH RESPONSE TIMES



SET-POINTS F1 & F2

Fig. 2 illustrates the frequency relationships between f1 and f2. Set-point f1 is always at a higher frequency than f2 and is defined simply by components R1/C1, set-point f2 is defined partly by R1/C1 and partly by R2/C2. The relationship between set-point frequency and the component values are given by:

$$f(Hz) = \frac{1}{0.7\ RC} \text{ or alternatively } RC = \frac{1}{0.7\ f(Hz)}$$

Where for f1, $RC = R1 \times C1$ ($M\Omega \times MFD$)

and for f2, $RC = (R1 \times C1) + (R2 \times C2)$

The factor 0.7 is a design constant and is subject to production tolerances of $\pm$5% maximum.

When operating in Band Mode, the inband signal channel bandwidth (BW) is defined as the frequency of f2 expressed as a percentage below f1, i.e. f1 = 100Hz, f2 = 90Hz, BW = 10%. Note that BW refers to *total* bandwidth *not* a plus or minus value about centreband.

Subject to the set-points lying within the specified frequency limits, the maximum BW permitted is 99%, i.e. frequency ratio f1 to f2 of 100:1.

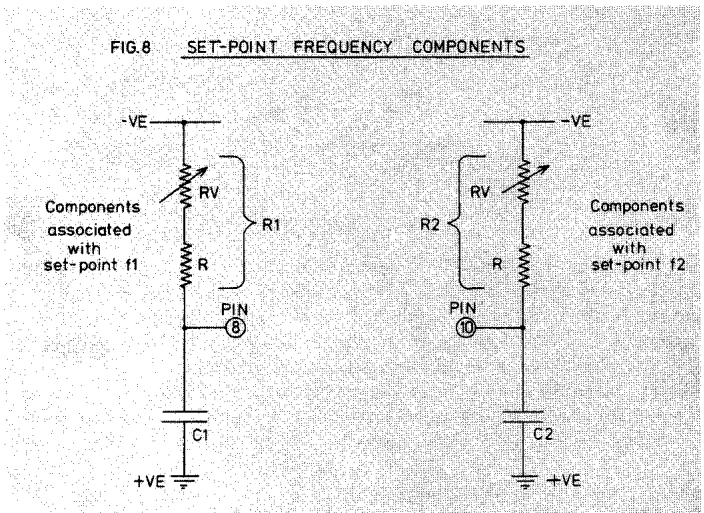
The minimum BW achievable is determined by practical limitations on the ratio of R1.C1 to R2, C2; using the minimum recommended values for R2, C2, bandwidths of 1% and upwards are obtainable depending on operating frequencies. When operating narrow-band, it is important to keep the value of C2 as large as possible by using the lowest permitted values for R2. This minimises the effects of stray wiring capacities, because if these capacities are large in relation to C2, set-point stability will suffer. When operating in *Datum mode,* a convenient method of setting f2 to a 'ghost' value about 10% below f1 is to make R1 = R2 and C2 nominally one tenth the value of C1. Alternatively minimum specified values may be fitted for R2 C2, regardless of the values used for R1 C1. The exact setting of the 'ghost' f2 has no effect on f1 stability; it only becomes important when it is very much lower than f1 and may therefore, influence the response time of the switches.

To choose a set of values, first calculate the C/R product for f1 and select those component values for R1/C1. Calculate the C/R product for f2, *subtract from this* the product already obtained for f1 and select values for R2/C2 which yield the product difference.

To adjust set-point frequencies and to allow adjustment for component tolerances, R1 and R2 may each consist of a fixed resistor in series with a variable resistor (see Fig.8). For maximum stability, the variable section should form only a small fraction of the total resistance.

For maximum set-point stability, good quality components should always be used; metal oxide resistors and polystyrene/polycarbonate capacitors are suggested.

FIG.8 SET-POINT FREQUENCY COMPONENTS



RECOMMENDED COMPONENT LIMITS

R1 & R2, 100KΩ min, no maximum limits
C1, 470pf min. 0·5MFD max
C2, 100pf min. 0·5MFD max.

BASIC TONE OPERATED SWITCH

FIG.9

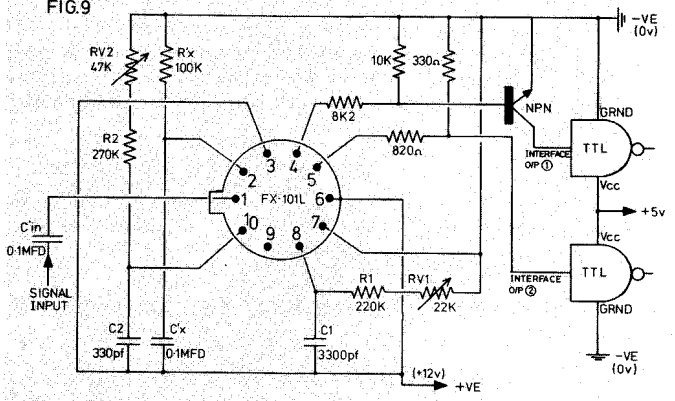


Fig. 9 shows the basic circuit arrangement for Band mode tone operated switching, and illustrates two different methods of interfacing an output switch to TTL logic elements. When the FX-101L output is ON, the output of interface (1) is at TTL logic '0' and the output of interface (2) at logic '1'.

With the component values given, the FX-101L output turns ON for an input tone of 1700Hz nominal (f1 = 1800Hz, f2 = 1600Hz), the typical recognition time (T_S) being 6mS. When the inband tone is cut-off, the switch turns OFF in 0.6 R'x C'x seconds (T_{FS}), which for the components specified is nominally equal to T_S at 6mS. If turn-off is effected by changing the inband frequency to an outband value, e.g. FSK operation, the turn-off time is $\frac{10}{f\ (Hz)}$ seconds, where f is the outband tone frequency.

By substituting suitable values for R1/C1, R2/C2 and R'x/C'x, operation at alternative tone frequencies is readily obtained.

VOICE OPERATED SWITCH

FIG.10

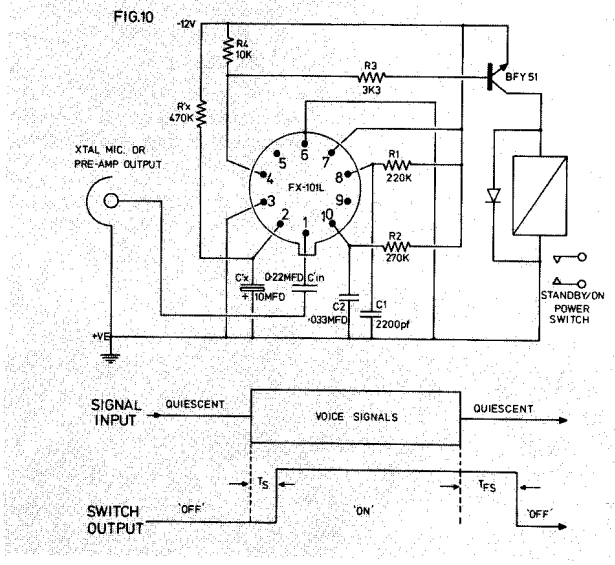


Fig. 10 shows the FX-101L arranged as a Voice Operated Switch, e.g. wideband frequency detector. Voice signals having frequencies lying between 160Hz (f2) and 3kHz (f1) turn the switch ON; when input signals cease for a specified minimum period of time, the switch turns OFF. This signal break recognition time is 2.8 seconds using the R'x/C'x values listed, other values may be used to obtain different 'dwell-over' times. If signals lying outside the voice band are applied, they may cause the switch to turn OFF prematurely ($\frac{10}{f2\ (Hz)} \approx$ 60mS); input signals outside the 160 Hz ⟶ 3kHz band should therefore be limited. The 'voice detect' switching time T_S is in the region 30 to 60mS, according to the initial frequencies present.

In this example the output switch operates a relay via a transistor driver. Note the surge suppression diode which must always be fitted with inductive loads. Other switching arrangements may be employed as required, e.g. semiconductor squelch switch.

SPECIFICATION

MAXIMUM RATINGS

FX-101L

Max, voltage between any pin and positive supply pin	−20V & +0.3V
Operating Temperature Range	−30°C to +85°C
Storage Temperature Range	−55°C to +125°C
Max. Output Switch load current	−10mA each
Max. Device Dissipation (at 25°C T'amb)	400mW

CHARACTERISTICS

(T'amb = 20°C, VDD = −12V ±2V, Set-point frequencies 10Hz to 3kHz unless specified)

Symb.	Parameter	Conditions & Notes		Min	Typ.	Max	Units
V_{DD}	SUPPLY VOLTAGE	Operating Range		−8	−12	−15	V
I_{DD}	SUPPLY CURRENT	Total, excluding switch load current			2.5		mA
V'in	SIGNAL AMPLITUDE RANGE	Sine or Pulse input signals, OHz to 100kHz, A.C. Coupled. Input impedance typically 50kΩ			0.1	15	V pk-pk
$f1/f2$	ADJUSTMENT LIMITS	Max & Min Set-Point frequencies		1Hz		20kHz	
	FREQUENCY RATIO	Permitted ratio adjustment, f2 percentage below f1		1		99	%
	SET-POINT DEFINITION	Individual set-point on/off differential as % of nominal set-point frequency.			0.1		%
Δf	SET-POINT STABILITY	Set-point deviation versus supply volts & T'amb. External components coiff. excluded.	Supply		0.05	0.08	%/%
			T'amb		0.005	0.02	%/°C
Ts	RESPONSE TIME	Overall switching time following receipt of 'switch' value frequency.	@ 3kHz		3.3		mS
			@ 500Hz		20		
R'on	SWITCH 'ON' RESISTANCE (EACH SWITCH)	Internal resistance between output pin and ground, switch 'ON' (Switch 'OFF' resistance >10M Ω)			0.3	1	KΩ
'I'	LOGIC HIGH	External logic levels to control inputs (Internal 300kΩ pull-up resistors give logic 'I' when pin O/C)	'I'	−6		−15	V
'0'	LOGIC LOW		'0'	0		−1.5	V

PRINTED CIRCUIT BOARD C-013L

The C-013L printed circuit card is designed to assist engineers in rapidly and correctly assembling a fully functional frequency operated switch module. Supplied ready punched and with component positions clearly marked, they are suitable for experimental work or as short run production P.C.B.'s.

Manufactured from 1/16" S.R.B.P. with tinned copper conductors, it measures 4" (103mm) x 3" (76mm). Card connections are shown by printed letter code. The cards are supplied complete with a set of press-in terminal posts for mounting those components most likely to be changed during experiments, thus minimising possible damage to the metal tracks. Components are not supplied. Connection to the card may be made by direct wiring or by edge connectors, using a 12 way 0.15" pitch P.C.B. socket. Normally, the FX-101L is soldered directly into position, but a 10 pin TO-100 style socket may be used if required.

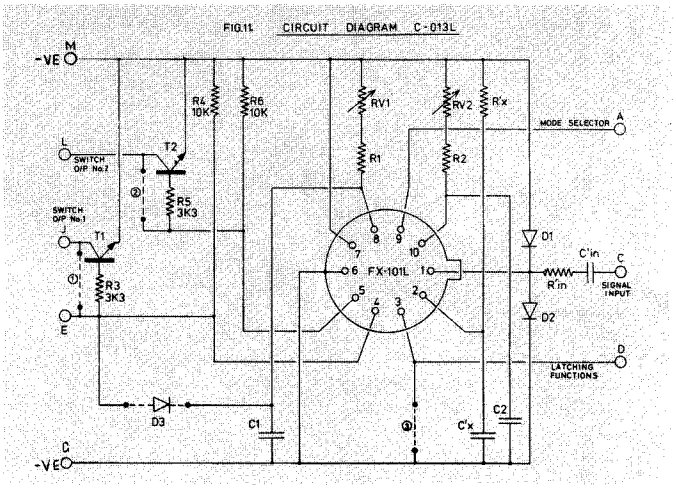
CIRCUIT DESCRIPTION C-013L

Supplies are connected to terminals M (-ve) and G (+ve). Two output terminals, L & J, are provided. Either or both may be used, directly or via transistor drivers, according to the links/components fitted. Low current loads up to -10mA, can be connected directly between the output and M, and links (1) or (2) fitted as appropriate. High current loads, up to 200mA, are connected between the output and G, in which case T1/2 and R3 through R6 should be fitted and links (1) and (2) removed.

Link 3 allows pin 3 to be permanently grounded, giving the 'Unlatched' operating mode. Alternatively, linking D to G via a N/O push-button gives Latch to OFF mode, push button to unlatch.

Diode D3 is fitted if Latch to ON is required. To unlatch, momentarily connect E to M using a push-button. Link (3) *must* be fitted if Latch to ON is used. Connecting terminal A to G gives Datum mode operation, leaving A disconnected gives Band mode. Input signals are applied to terminal C. If high voltage spikes can appear on the signal line, protective diodes D1/D2 should be fitted and a 10k Ω resistor used for R'in. If no protection is required, R'in may be a wire link.

If C'x is omitted, a wire link *must* be fitted in its place.



COMPONENT NOTES:

D1 and D2	:	(optional) 1N914 or similar.
RV	:	Plessey type WMP or similar.
TR	:	TO-5 silicon NPN rating to suit load.