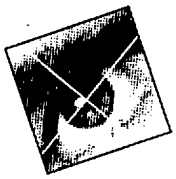

FUNCTIONAL DESCRIPTION

Pin Information and Block Diagram

Table 1 details the Bt481A's pin numbers, names, and descriptions. Figure 1 illustrates the pinout. Figure 2 is a detailed block diagram of the Bt481A.

Table 1. Pin Descriptions *(1 of 3)*

Pin Number	Pin Name	Description
7	BLANK*	Composite Blank Control Input (TTL compatible). A logic zero drives the analog outputs to the blanking level, as specified in Tables 7–9. BLANK* is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
23	SETUP	Setup Control Input (TTL compatible). This input is used to specify either a 0 IRE (logical zero) or 7.5 IRE (logical one) blanking pedestal. This pin should not be left floating
5	SYNC*	Composite Sync Control Input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the analog outputs (see Figures 8–10). SYNC* does not override any other control or data input, as shown in Tables 7–9; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK. If sync information is not required on the video outputs, SYNC* should be connected to GND.
40	CLOCK	Clock Input (TTL compatible). The rising edge of CLOCK latches the P[7:0], OL[3:0], SYNC*, and BLANK* inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK be driven by a dedicated TTL buffer to avoid reflection-induced jitter.
32–39	P[7:0]	Pixel Select Inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. They are latched on the rising edge of CLOCK. P[0] is the LSB. Unused inputs should be connected to GND.
41–44	OL[3:0]	Overlay Select Inputs (TTL compatible). These inputs specify which palette is to be used to provide color information, as specified in Table 6. When the overlay palette is accessed, the P[7:0] inputs are ignored. They are latched on the rising edge of CLOCK. OL[0] is the LSB. Unused inputs should be connected to GND.
1	COMP	Compensation Pin. If an external or internal voltage reference is used, this pin should be connected to the reference amplifier output (OPA pin). If an external current reference is used, this pin should be connected to full-scale adjust control (IREF pin). A 0.1 µF ceramic capacitor must always be used to bypass this pin to VAA. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. The PC Board Layout Considerations section contains critical layout information.

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Table 1. Pin Descriptions *(2 of 3)*

Pin Number	Pin Name	Description
31	VREF	Voltage Reference Input. If an external voltage reference is used, it must supply this input with a 1.235 V (typical) reference. If an external current reference is used, this pin should be left floating, except for the bypass capacitor. A 0.1 µF ceramic capacitor should decouple this input to GND. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. When using the internal reference, this pin should not drive any external circuitry other than the decoupling capacitor. The PC Board Layout Considerations section contains further information.
30	OPA	Reference Amplifier Output. If an external or internal voltage reference is used, this pin must be connected to COMP. When an external current reference is used, this pin should be left floating. The PC Board Layout Considerations section contains further information.
25–27	IOR, IOG, IOB	Red, Green, And Blue Current Outputs. These high-impedance current sources can directly drive a doubly-terminated 75 Ω coaxial cable. The PC Board Layout Considerations section contains further information.
28	IREF	Full-Scale Adjust Control. The IRE relationships in Figures 8–10 are maintained, regardless of the full-scale output current. When an external or internal voltage reference is used, a resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal. The relationship between RSET and the full-scale output current on each output is: RSET (Ω) = K * 1,000 * VREF (V) / Iout (mA) K is defined in the table below. It is recommended that a 147 Ω RSET resistor be used for doubly-terminated 75 Ω loads (i.e., RS-343A applications). For PS/2 applications (i.e., 0.7 V into 50 Ω with no sync), a 182 Ω RSET resistor is recommended.

Mode	Pedestal	K (with sync)	K (no sync)
6-bit	7.5 IRE	3.17	2.26
8-bit	7.5 IRE	3.195	2.28
6-bit	0 IRE	3.0	2.10
8-bit	0 IRE	3.028	2.12

See the PC Board Layout Considerations section for further information.

16	WR*	Write Control Input (TTL compatible). D[7:0] data is latched on the rising edge of WR*, and RS[2:0] are latched on the falling edge of WR* during MPU write operations. RD* and WR* should not be asserted simultaneously.
6	RD*	Read Control Input (TTL compatible). To read data from the device, RD* must be a logical zero. RS[2:0] are latched on the falling edge of RD* during MPU read operations. RD* and WR* should not be asserted simultaneously.
17–19	RS[2:0]	Register Select Inputs (TTL compatible). RS[2:0] specify the type of read or write operation being performed, as detailed in Tables 2 and 3.
8–15	D[7:0]	Data Bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.

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Table 1. Pin Descriptions *(3 of 3)*

Pin Number	Pin Name	Description
2	6*/8	6-Bit/8-Bit Select Input (TTL compatible). This pin specifies whether the MPU is reading and writing 8 bits (logical one) or 6 bits (logical zero) of color information each cycle. For 8-bit operation, MPU Bit D[7] is the most significant bit during read/write cycles. For 6-bit operation, MPU bit D[5] is the most significant bit during read/write cycles. (D[7] and D[6] are ignored during write cycles and are logical zero during read cycles.)
1	SENSE*	Sense Output (CMOS compatible). SENSE* is a logical zero if one or more of the IOR, IOG, and IOB outputs have exceeded the internal voltage reference level. SENSE* may not be stable while SYNC* is toggling. The SENSE* output can drive only one CMOS load.
20	TRUECOL*	True-Color Mode Select Input (TTL compatible). This signal is inverted and logically ORed with bit A[7] in Command Register A. A logical zero will enable the true-color modes. By programming the proper command register bits, the user can choose either 5:5:5, 5:6:5, 8:8:8, or 8:8:8:OL and determine whether the pixels are input on a single clock edge or a dual clock edge (see the Command Register section for details). The TRUECOL* pin should be tied to VAA to disable the hardware selection of the true-color mode.
4, 21, 22	VAA	Analog Power. All VAA pins must be connected together on the same PCB plane to prevent latchup.
3, 24	GND	Analog Ground. All GND pins must be connected together on the same PCB plane to prevent latchup.

Figure 1. Pinout Diagram

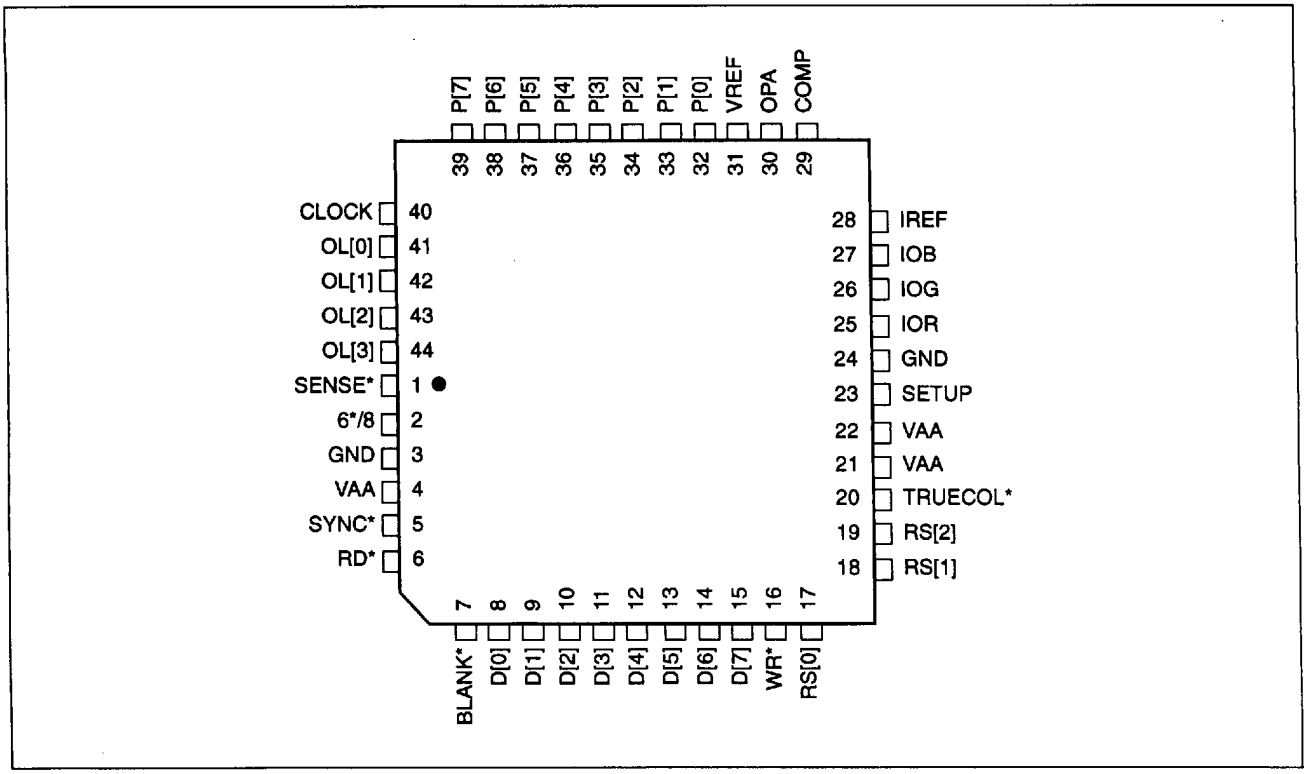

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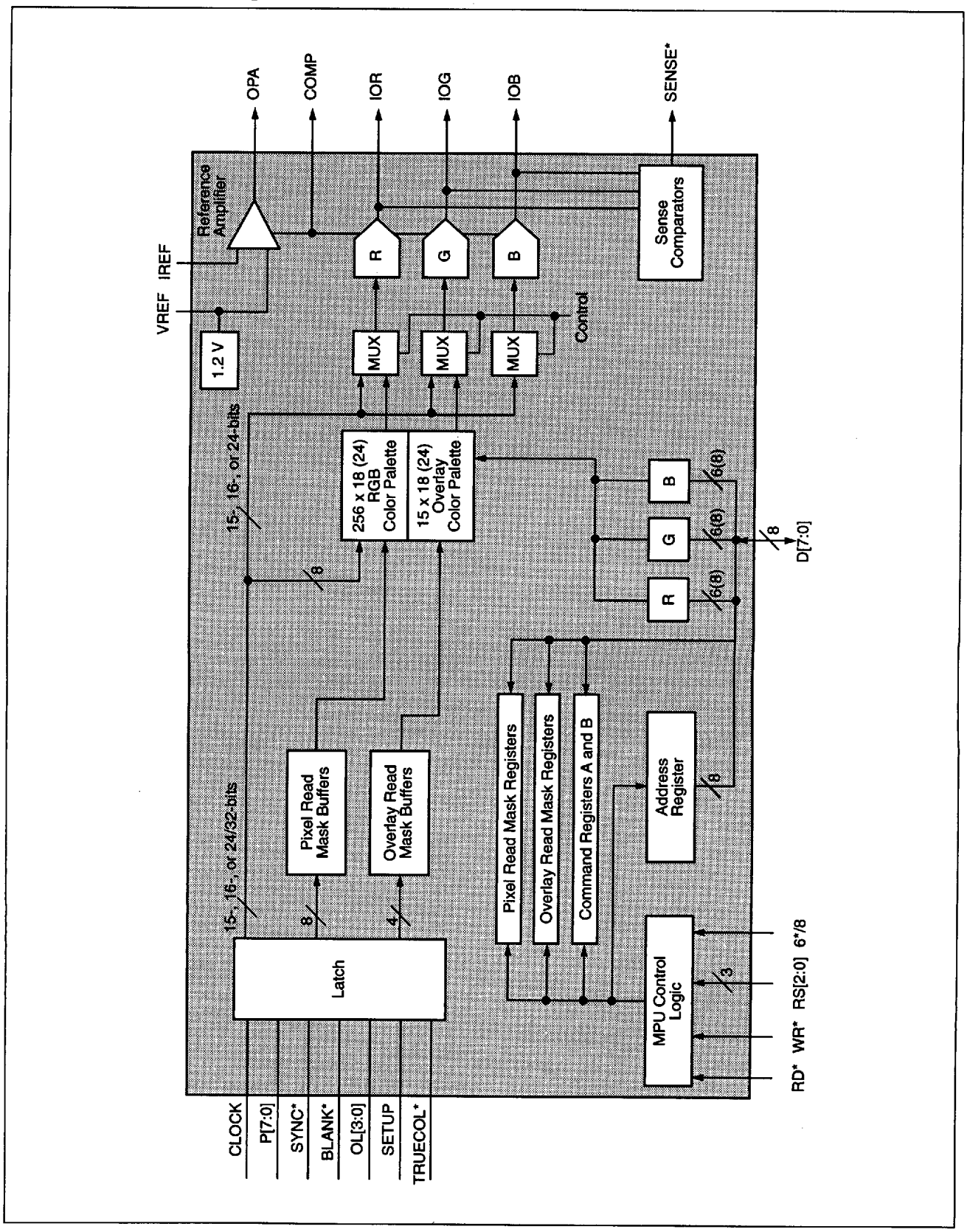
Figure 2. Detailed Block Diagram



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MPU Interface

As illustrated in the detailed block diagram (Figure 2), the Bt481A supports a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers.

The RS[2:0] select inputs specify whether the MPU is accessing the address register, color palette RAM, overlay registers, or read mask register, as shown in Table 2. The 8-bit address register addresses the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D[0] and is the least significant bit (see Table 3).

Table 2. Control Input Truth Table

RS[2]	RS[1]	RS[0]	Addressed by MPU
0	0	0	Address Register (Palette Write Mode)
0	1	1	Address Register (Palette Read Mode)
0	0	1	Color Palette RAM
0	1	0	Pixel Read Mask Register
1	0	0	Address Register (Overlay Write Mode)
1	1	1	Address Register (Overlay Read Mode)
1	0	1	Overlay Registers
1	1	0	Command Register A

Table 3. Address Register (ADDR) Operation

	Value	RS[2]	RS[1]	RS[0]	Addressed by MPU
ADDRa, (Counts Modulo 3)	00 01 10				Red Value Green Value Blue Value
ADDR[7:0] (Counts Binary)	$00–$FF 0000 0000 0000 0001 : 0000 1111	0 1 1 : 1	0 0 0 : 0	1 1 1 : 1	Color Palette RAM Reserved Overlay Color 1 : Overlay Color 15

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Writing Color Palette RAM Data

To write color data, the MPU writes the address register (RAM write mode) with the address of the color palette RAM location to be modified. The MPU performs three successive write cycles (6 or 8 bits each of red, green, and blue), using RS[2:0] to select the color palette RAM. After the blue write cycle, the 3 bytes of color information are concatenated into an 18-bit or 24-bit word and written to the location specified by the address register. The address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous RGB write cycles until the entire block has been written.

Reading Color Palette RAM Data

To read color palette RAM data, the MPU loads the address register (RAM read mode) with the address of the color palette RAM location to be read. The contents of the color palette RAM at the specified address are copied into the RGB registers, and the address register is incremented to the next RAM location. The MPU performs three successive read cycles (6 or 8 bits each of red, green, and blue), using RS[2:0] to select the color palette RAM. Following the blue read cycle, the contents of the color palette RAM at the address specified by the address register are copied into the RGB registers and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous RGB read cycles until the entire block has been read.

Writing Overlay

To write overlay data, the MPU writes the address register (overlay write mode) with the address of the overlay location to be modified. The MPU performs three successive write cycles (6 or 8 bits each of red, green, and blue), using RS[2:0] to select the overlay registers. After the blue write cycle, the 3 bytes of color information are concatenated into an 18-bit or 24-bit word and written to the overlay location specified by the address register. The address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous RGB write cycles until the entire block has been written.

Reading Overlay

To read overlay data, the MPU loads the address register (overlay read mode) with the address of the overlay location to be read. The contents of the overlay register at the specified address are copied into the RGB registers, and the address register is incremented to the next overlay location. The MPU performs three successive read cycles (6 or 8 bits each of red, green, and blue), using RS[2:0] to select the overlay registers. Following the blue read cycle, the contents of the overlay location at the address specified by the address register are copied into the RGB registers and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous RGB read cycles until the entire block has been read.

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15, 16, and 24/32 Bits-per-Pixel Operation

When the 15, 16, or 24/32 bits-per-pixel modes are activated (see Command Register A in the Internal Registers section), the inputs accept 16, 24, or 32 bits of pixel information from the 8-pin pixel port P[7:0]. The 8-bit inputs form a 16- or 24-bit pixel (B15–0/B23–B0) to directly drive the 8-bit triple video DACs. The color lookup table and the read mask register are bypassed. Internally, the unused LSBs of all DACs are forced to zero in 15 or 16 bits-per-pixel modes. The 16- and 24-bit word (B15–0/B23–B0) is assigned to the DACs according to Table 4.

Table 4. Word Assignments to DACs

8:8:8:8 True Color Format RGB	8:8:8:8 True Color Format BGR	5:6:5 XGA Format	5:5:5 TARGA Format	Comments
			B15	Ignored
B7–B0	B23–B16	B15–B11	B14–B10	Red DAC
B15–B8	B15–B8	B10–B5	B9–B5	Green DAC
B23–B16	B7–B0	B4–B0	B4–B0	Blue DAC
B31–B24	B31–B24			Palette or Masked

15, 16, and 24 Bits-per-Pixel Dual-Edge Clock

In the 15 and 16 bits-per-pixel dual-edge clock mode (see the Command Register A, bits A[7:4] description in the Internal Registers section), the least significant byte is latched on the rising edge of the pixel clock when BLANK* high is latched. Also in this mode, the most significant byte is latched on the falling edge of the pixel clock when BLANK* high is latched. Therefore, only one input clock period is required to load a 16-bit pixel.

In the 32 bits-per-pixel dual-edge clock mode, 32 bits of data, 24 bits of true-color and 8 bits of palette index are latched on two rising and two falling edges. Therefore, only two input clock cycles are required to load a 32-bit pixel. If palette indexing is not required, logical zeros can be written for the palette overlay data, as location zero in the palette RAM cannot be accessed in this mode. Or palette overlay data can be masked out through the pixel read mask register. If the palette index data is not a logical zero or masked, the data will address any one of 255 locations in the palette RAM. Palette data has priority over bypass data.

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15, 16, and 24 Bits-per-Pixel Single-Edge Clock

In the 15 and 16 bits-per-pixel single-edge clock mode (see Command Register A in the Internal Registers section), the inputs accept 16 bits of information by using two input clock cycles. The least significant byte is latched on the first rising edge of the input clock, and the most significant byte is latched on the second rising edge of the input clock. The bytes are synchronized with the BLANK* signal. The first byte latched after BLANK* goes high is the least significant byte. Since a pixel is latched in two clock cycles, the input clock must be twice as fast as the internal pipeline clock. The Bt481A has an internal divider to generate the pipeline clock from the input clock.

In the 24 bits-per-pixel single-edge clock mode, the inputs accept 24 bits of pixel data by using three input clock cycles. The red byte is latched on the first rising edge of the pixel clock when BLANK* high is latched. The next two clock cycles latch the green and blue bytes. Since a 24-bit pixel is latched in three input clock cycles, the input clock must be three times as fast as the internal pipeline clock. The Bt481A has an internal divider to generate the pipeline clock from the pixel input clock. Palette data has priority over bypass data.

Additional Information

When the MPU is accessing the color palette RAM, the address register resets to $00 following a blue read or write cycle to RAM location $FF. While the MPU is accessing the overlay color registers, the 4 most significant bits of the address register (ADDR[7:4]) are ignored.

The MPU interface operates asynchronously to the pixel clock. Data transfers between the color palette RAM/overlay registers and the color registers (R, G, and B in the block diagram) are synchronized by internal logic. Data transfers take place in the period between MPU accesses. To reduce noticeable sparkling on the CRT during MPU access to the color palette RAMs, internal logic maintains the previous output color data on the analog outputs while the transfer between lookup table RAMs and the RGB registers occurs.

To keep track of the red, green, and blue read/write cycles, the address register has 2 additional bits (ADDRa and ADDRb) that count modulo three, as shown in Table 3. They are reset to zero when the MPU writes to the address register and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other 8 bits of the address register, incremented following a blue read or write cycle (ADDR[7:0]), are accessible to the MPU. These bits are used to address color palette RAM locations and overlay registers. The MPU may read the address register at any time without modifying its contents or the existing read/write mode. The pixel clock must be active for MPU accesses to the color palette RAM.

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Accessing Command Registers

Accessing Command Register B

Command Register B is defined to select SETUP, 6-bit/8-bit, and the sleep modes of Bt481A. There are only three register select lines and all eight combinations have already been used. Therefore, Command Register B must be accessed indirectly through Pixel Read Mode Register. Bit A0 of Command Register A must be set to a logical one to enable access to extended registers.

For example, Command Register B can be accessed with the following sequence of operations:

1 Set RS[2:0] = 110 to access Command Register A.
2 Write a logical one to Command Register A, bit A[0].
3 Set RS[2:0] = 000 for address register write mode.
4 Write address register to 0000 0010 for Command Register B.
5 Set RS[2:0] = 010 for pixel read mask register.
6 Read or write Command Register B.
7 Set RS[2:0] = 110 to access Command Register A.
8 Reset Command Register A, bit A[0] to a logical zero.

Table 5 contains specifications to indirectly address other registers.

Table 5. Indirect Register Addressing Truth Table

	Value	RS[2]	RS[1]	RS[0]	Bit A[0]	Registers
ADDR 0–7 (counts binary)	0000 0000	0	1	0	1	Read Mask Register
	0000 0001	0	1	0	1	Overlay Mask Register
	0000 0010	0	1	0	1	Command Register B

Accessing Command Registers Without The RS2 Line

When the overlay functionality of the Bt481A is not used and the Register Select Line 2 (RS2) must be tied low at all times, the command registers of the Bt481A can still be accessed.

A flag will be set when the pixel read mask register (RS[1] = 1 and RS[0] = 0) is read four times consecutively. The next write to the pixel read mask register will be directed to Command Register A and can be used to set the bits in that register. Any access of the command register thereafter will also require four consecutive reads to the pixel read mask register. A write to any address other than the pixel read mask register will reset the flag.

If bit A2 in Command Register A is set to logical one, internally, the RS2 signal will also be set to logical one, even if the RS[2] pin is grounded. If bit A2 in Command Register A is set to logical zero, the state of the RS2 signal will depend on the logic state of the RS[2] pin.

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Automatic Detection Without The RS2 Line

In some applications it is necessary to detect the presence of Bt481A. This may be automated with a software routine accessing Command Register B. Bt481A's Command Register B has a unique signature which identifies its presence in the graphics system. The Pixel Read Mask Register and Command Register A must be used in order to gain access to Command Register B.

The required steps for the Bt481A auto-detect routine are listed below in the IPF protocol. These steps assume that RS2 line is grounded and is therefore not available.

o	3c6	FF	Initialize Pixel Read Mask Register to FF.
i	3c6		Read Pixel Read Mask Register 4 times consecutively, so that the next write will be directed to Command Register A.
i	3c6		
i	3c6		
i	3c6		
o	3c6	01	Write a logical 1 to A0 so that the extended register set can be accessed.
o	3c8	02	Set RS1–0 to 00 (address register write mode) and write address register to 0000 0010 (Command Register B).
i	3c6		Set RS1–0 to 10 (read mask register) and read Command Register B). This should return a value of 1Eh.
o	3c8	00	Set RS1–0 to 00 (address register write mode) and write address register to 0000 0000 (Pixel Read Mask Register).
o	3c6	FF	Restore Pixel Read Mask Register to FF.
i	3c6		Read Pixel Read Mask Register 4 times consecutively, so that the next write will be directed to Command Register A.
i	3c6		
i	3c6		
i	3c6		
o	3c6	00	Write a logical 0 to A0.

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6-Bit/8-Bit Color Selection

The command register bit B1 or the 6*/8 pin can be used to specify whether the MPU is reading and writing 6 bits or 8 bits of color information each cycle. The 6/8 bit (bit B1 in Command Register B) and the 6*/8 pin (pin #2) are logically ANDed. If the 6/8 bit is a logical one, the 6*/8 pin controls 6- or 8-bit operation. While the 6/8 bit remains at logical zero, the MPU will read and write 6 bits of color information each cycle. For 8-bit operation, D[0] is the LSB and D[7] is the MSB of color data.

For 6-bit operation, color data is contained on the lower 6 bits of the data bus; D0 is the LSB, and D5 is the MSB of color data. When color data is written, D6 and D7 are ignored. During color read cycles, D6 and D7 will be a logical zero.

Accessing the cursor RAM array does not depend on the resolution of the DACs. If the 6*/8 pin is held low (6-bit operation), the Bt481A will emulate a Bt471.

In the 6-bit mode, the Bt481A's full-scale output current will be about 1.5 percent lower than when in the 8-bit mode. This is because the 2 LSBs of each 8-bit DAC are always a logical zero when in the 6-bit mode.

Power-Down Mode

The Bt481A incorporates a power-down capability, controlled by the SLEEP command bit. While the SLEEP bit is a logical zero, the Bt481A functions normally.

While the SLEEP bit is a logical one, the DACs and power to the RAM are turned off. The RAM still retains the data. Also, the RAM may still be read or written to while the SLEEP bit is a logical one if the pixel clock is running. The RAM automatically powers up during MPU read/write cycles and shuts down when the MPU access is complete. The DACs will be turned off during sleep mode only if a voltage reference (internal or external) is used. If an external current reference is used, external circuitry should turn off the current reference (IREF = 0 mA) during sleep mode.

When an external voltage reference is used, external circuitry should turn off the voltage reference (VREF = 0 V) to further reduce power consumption caused by biasing of portions of the internal voltage reference.

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SENSE* Output

SENSE* is a logical zero if one or more of the IOR, IOG, and IOB outputs have exceeded the internal voltage reference level of the SENSE comparator circuit. This output determines the presence of a CRT monitor and, with diagnostic code, the difference between a loaded or unloaded RGB line can be discerned. The reference is generated by a voltage divider from the external 1.235 V voltage reference on the VREF pin. For proper operation of the SENSE circuit, the following levels should be applied to the comparator with the IOR, IOG, and IOB outputs:

DAC Low Voltage ≤ 310 mV
DAC High Voltage ≥ 430 mV

There is an additional ±10 percent tolerance on the above levels when the internal voltage reference or an external current reference is used. SYNC* should be a logical zero for SENSE* to be stable.

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Internal VREF and DAC Output Level

When using the internal voltage reference of Bt481A, the DAC output levels are affected by the accuracy of the DACs as well as the voltage reference accuracy.

Figure 3 shows how the internal voltage reference interacts with the Bt481A DACs. At one input of the Bt481A op amp, a voltage reference of approximately 1.2 V exists. At the other input of the op amp, the value of the RSET resistor sets the full-scale current level for the DACs. The output of the op amp controls the IREF current source and in turn is fed back to the IREF pin.

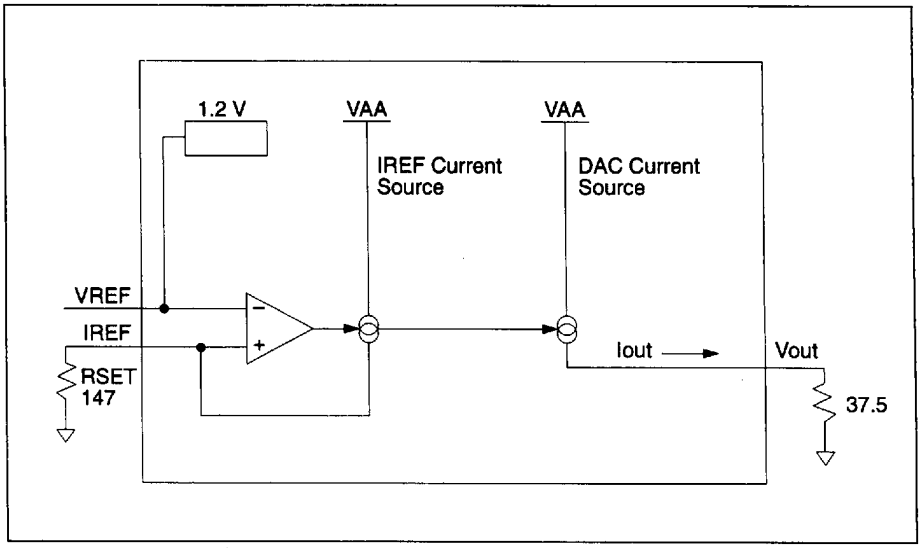
Changing the voltage reference level or the value of the RSET resistor allows control of the IREF current level. The IREF current is mirrored by the DAC current cells which set the DAC output level (Iout).

The DAC output current level is determined by the following equation:

Iout = K * VREF / RSET
(See IREF pin description for K value.)

When using Bt481A's internal voltage reference, the variation in Iout for a given RSET is the result of variation in the internal voltage reference level as well as any error due to the DAC itself. Therefore, it is more meaningful to the user to focus on the overall Iout variation, rather than the individual variation of the internal voltage reference or the DACs.

Figure 3. Bt481A Internal VREF and DAC Output



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Controller Interface

The P[7:0] and OL[3:0] inputs are used to address the color palette RAM and overlay registers, as shown in Table 6. The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bit-wise logically ANDed with the P[7:0] inputs. Bit D[0] of the pixel read mask register corresponds to pixel input P0. The contents of the overlay read mask register are bit-wise logically ANDed with the OL[3:0] inputs. Bit D[0] of the overlay read mask register corresponds to overlay input OL[0], and bit D[3] of the overlay read mask register corresponds to overlay input OL[3]. Bits D[7:4] of the overlay read mask register are ignored. Two consecutive write operations must be performed to write to the overlay read mask register. The first write is to the overlay read mask, and the second is to the pixel read mask. All 12 bits will be updated concurrently, synchronous to the pixel clock. Command Register B in the Internal Register section contains information regarding the accessibility of the overlay read mask register. The addressed locations provide 18 bits or 24 bits of color information to the three D/A converters.

The SYNC* and BLANK* inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs. This produces the specific output levels required for video applications, as illustrated in Figures 4–6. Tables 7–9 detail how the SYNC* and BLANK* inputs modify the output levels.

The SETUP input pin is logically ORed with the SETUP command bit and specifies whether a 0 or 7.5 IRE blanking pedestal is to be used.

The analog outputs of the Bt481A can directly drive a 37.5 Ω load, such as a doubly terminated 75 Ω coaxial cable.

Table 6. Pixel and Overlay Control Truth Table (Pixel Read Mask Register = $FF)

OL[3:0]	P[7:0]	Addressed by Pixel Port
$0	$00	Color Palette RAM Location $00
$0	$01	Color Palette RAM Location $01
:	:	:
$0	$FF	Color Palette RAM Location $FF
$1	$xx	Overlay Color 1
:	$xx	:
$F	$xx	Overlay Color 15

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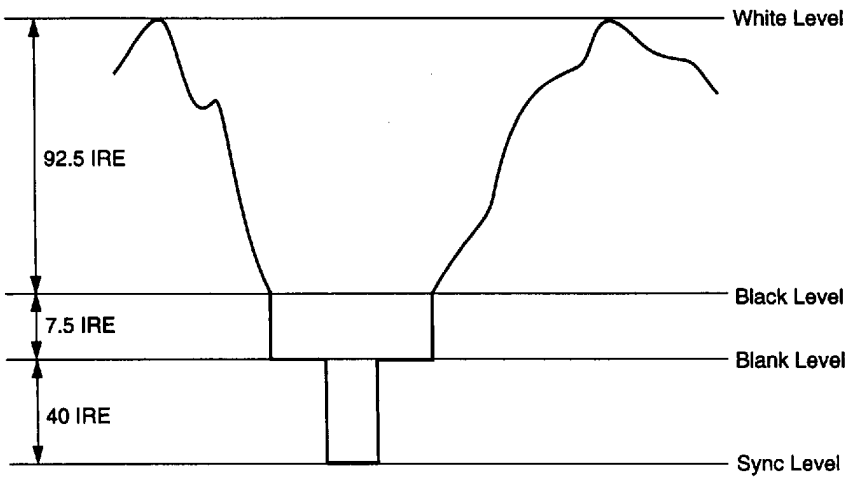
Figure 4. RS-343A Composite Video Output Waveforms (SETUP = 7.5 IRE)

No Sync		Sync	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75 Ω doubly terminated load; SETUP = 7.5 IRE. VREF = 1.235 V and RSET = 147 Ω. RS-343A levels and tolerances are assumed on all levels.

Table 7. RS-343A Video Output Truth Table (SETUP = 7.5 IRE)

Description	Sync Disabled Iout (mA)	Sync Enabled Iout (mA)	SYNC*	BLANK*	DAC Input Data
White	19.05	26.67	1	1	$FF
Data	Data + 1.44	Data + 9.05	1	1	Data
Data - Sync	Data + 1.44	Data + 1.44	0	1	Data
Black	1.44	9.05	1	1	$00
Black - Sync	1.44	1.44	0	1	$00
Blank	0	7.62	1	0	$xx
Sync	0	0	0	0	$xx

Note: 75 Ω doubly terminated load; SETUP = 7.5 IRE. VREF = 1.235 V and RSET = 147 Ω.

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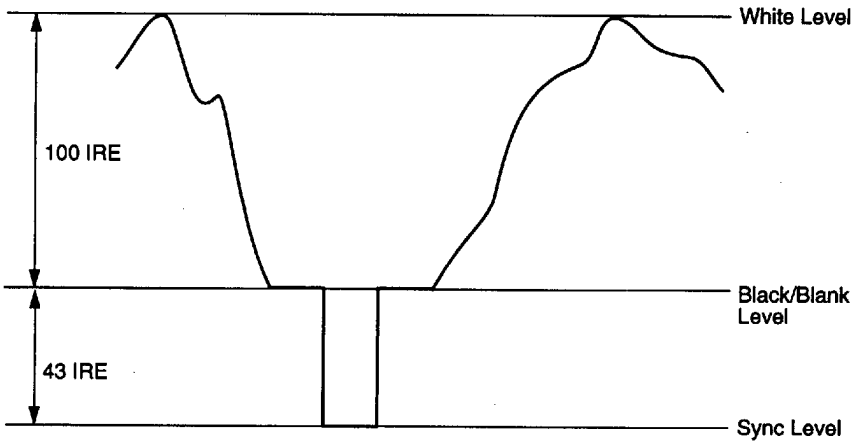
Figure 5. RS-343A Composite Video Output Waveforms (SETUP = 0 IRE)

No Sync		Sync	
MA	V	MA	V
17.62	0.660	25.24	0.950
0.00	0.000	7.62	0.286
0.00	0.000	0.00	0.000



Note: 75 Ω doubly terminated load; SETUP = 0 IRE. VREF = 1.235 V and RSET = 147 Ω. RS-343A levels and tolerances are assumed on all levels.

Table 8. RS-343A Video Output Truth Table (SETUP = 0 IRE)

Description	Sync Disabled Iout (mA)	Sync Enabled Iout (mA)	SYNC*	BLANK*	DAC Input Data
White	17.62	25.24	1	1	$FF
Data	Data	Data + 7.62	1	1	Data
Data - Sync	Data	Data	0	1	Data
Black	0	7.62	1	1	$00
Black - Sync	0	0	0	1	$00
Blank	0	7.62	1	0	$xx
Sync	0	0	0	0	$xx

Note: 75 Ω doubly terminated load; SETUP = 0 IRE. VREF = 1.235 V and RSET = 147 Ω.

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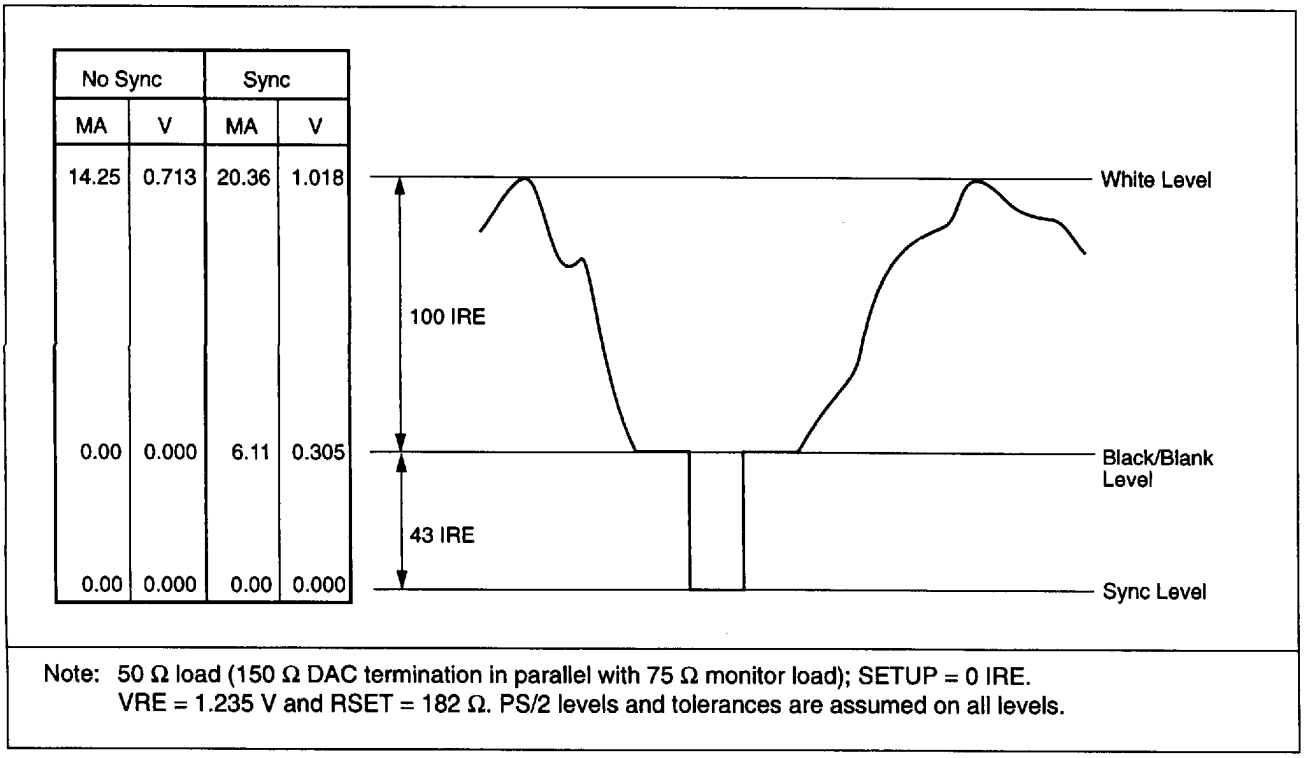
Figure 6. PS/2 Composite Video Output Waveforms (SETUP = 0 IRE)



Note: 50 Ω load (150 Ω DAC termination in parallel with 75 Ω monitor load); SETUP = 0 IRE. VRE = 1.235 V and RSET = 182 Ω. PS/2 levels and tolerances are assumed on all levels.

Table 9. PS/2 Video Output Truth Table (SETUP = 0 IRE)

Description	Sync Disabled Iout (mA)	Sync Enabled Iout (mA)	SYNC*	BLANK*	DAC Input Data
White	14.25	20.36	1	1	$FF
Data	Data	data + 6.11	1	1	Data
Data - Sync	Data	Data	0	1	Data
Black	0	6.11	1	1	$00
Black - Sync	0	0	0	1	$00
Blank	0	6.11	1	0	$xx
Sync	0	0	0	0	$xx

Note: 50 Ω load; SETUP = 0 IRE. VREF = 1.235 V and RSET = 182 Ω.

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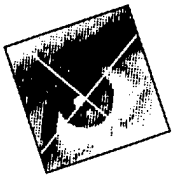

INTERNAL REGISTERS

Command Register A

This register may be written to or read by the MPU at any time. All bits are initialized to logical zero on power-up.

A logical one on bit A7 enables 15-, 16-, and 24/32-bit modes when used with bits A6, A5, and A4. If A7 is a logical zero, pseudo-color mode is enabled regardless of the state of A6, A5, or A4.

Bit A6 determines whether the device is in 15- or 16-bit-per-pixel mode.

Bit A5 determines whether the data is input on the rising edge of the input clock, or on the rising and falling edges of the input clock. A logical zero written to this bit indicates a dual-edge clock, and a logical one indicates a single-edge clock.

Bit A4 indicates a 24- or 32-bit input, i.e., a 24-bit true-color bypass only, or a 24-bit true-color bypass and an 8-bit VGA pass through. Bit A5 determines whether the pixels are input 8 bits at a time on every rising edge, or 8 bits at a time on rising and falling edges of the input clock. When bits A4 and A6 are set to logical one, the inputs are 24-bit true-color bypass, operating in single-edge clock mode.

A7	A6	A5	A4	
0	x	x	x	Pseudo Color (256 Colors)
1	0	0	0	5:5:5 Dual-Edge Clock (33 K Colors)
1	1	0	0	5:6:5 Dual-Edge Clock (65 K Colors)
1	0	1	0	5:5:5 Single-Edge Clock (33 K Colors)
1	1	1	0	5:6:5 Single-Edge Clock (65 K Colors)
1	0	0	1	8:8:8 OL Dual-Edge Clock (16.8 M Colors)
1	1	1	1	8:8:8 Single-Edge Clock Only (16.8 M Colors)

A3	Reserved (logical zero)	A logical zero must be written to this bit to ensure proper operation.
A2	RS2 Select (0) RS2 signal controlled by RS[2] pin (1) RS2 signal controlled by A2	If bit A2 in Command Register A is set to logical one, internally, the RS2 signal will also be set to logical one, even if the RS2 pin is grounded. If bit A2 in Command Register A is set to logical zero, the state of the RS2 signal will depend on the logic state of the RS[2] pin.
A1	24/32-Bit RGB or BGR Select (0) 24/32-bit RGB format selected (1) 24/32-bit BGR format selected	A logical zero written to this bit will set the 24- or 32-bit-per-pixel mode to RGB format. A logical one written to this bit will set the 24- or 32-bit-per-pixel mode to BGR format.
A0	Extended Register Select (0) Extended register set cannot be accessed (1) Extended register set can be accessed	A logical one written to this bit allows the user to indirectly access the extended register set. Included in the extended register set are Command Register B and Overlay Mask Register.

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Command Register B

This register is operational only while bit A0 in Command Register A is a logical one. This register is initialized on power-up. On power-up, bits B7, B6, B5, and B0 are set to logical zero; bits B4, B3, B2, and B1 are set to logical one to enable the Bt481A to emulate the Bt478. While the 6*/8 pin is held low, this register will be functionally ignored.

B7	Reserved (logical zero)	A logical zero must be written to this bit to ensure proper operation.
B6	Overlay Register Mask Select (0) Overlay register mask inhibited (1) Overlay register mask enabled	A logical zero written to this bit inhibits address of the overlay registers only during true-color operations. A logical one written to this bit enables address of the overlay registers only during true-color operations.
B5	SETUP Select (0) 0 IRE (1) 7.5 IRE	B5 specifies the blanking pedestal to be either 0 or 7.5 IRE.
B4	Blue Sync Enable (0) No sync on blue (1) Sync on blue	B4 specifies whether the IOB output contains sync information.
B3	Green Sync Enable (0) No sync on green (1) Sync on green	B3 specifies whether the IOG output contains sync information.
B2	Red Sync Enable (0) No sync on red (1) Sync on red	B2 specifies whether the IOR output contains sync information.
B1	6-Bit/8-Bit Select (0) 6-bit (1) 8-bit	On the Bt481A, B1 specifies whether the MPU is reading and writing 8 bits (logical one) or 6 bits (logical zero) of color information each cycle. The 6*/8 bit and 6*/8 pin are logically ANDed.
B0	SLEEP Enable (0) Normal operation (1) Sleep mode	While B0 is a logical zero, the Bt481A functions normally. If B0 is a logical one, the DACs and power to the RAM are turned off. The RAM still retains the data and may be read or written to while the pixel clock is running. The RAM automatically powers-up during MPU read/write cycles and shuts down when the MPU access is completed. About 1 second is required for the Bt481A to output valid video data after enabling normal operation (coming out of sleep mode). This time will vary depending on the size of the COMP capacitor. The DACs will be turned off during sleep mode only if a voltage reference (internal or external) is used. If an external current reference is used, external circuitry should turn the current reference off during sleep mode.

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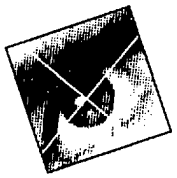

PC BOARD LAYOUT CONSIDERATIONS

For optimum performance of the Bt481A, proper CMOS RAMDAC layout techniques should be used.

The layout should be optimized for lowest noise on the Bt481A power and ground planes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of six layers is recommended. The ground layer should be used as a shield to isolate noise from the analog traces with layer 1 (top) for the analog traces, layer 2 for the ground plane, layer 3 for the analog power plane, and the remaining layers used for digital traces and digital power supplies.

Component Placement

Components should be placed as close as possible to the associated RAMDAC pin. Whenever possible, components should be placed so traces can be connected point to point.

The optimum layout enables the Bt481A to be located as close as possible to the power supply connector and the video output connector.

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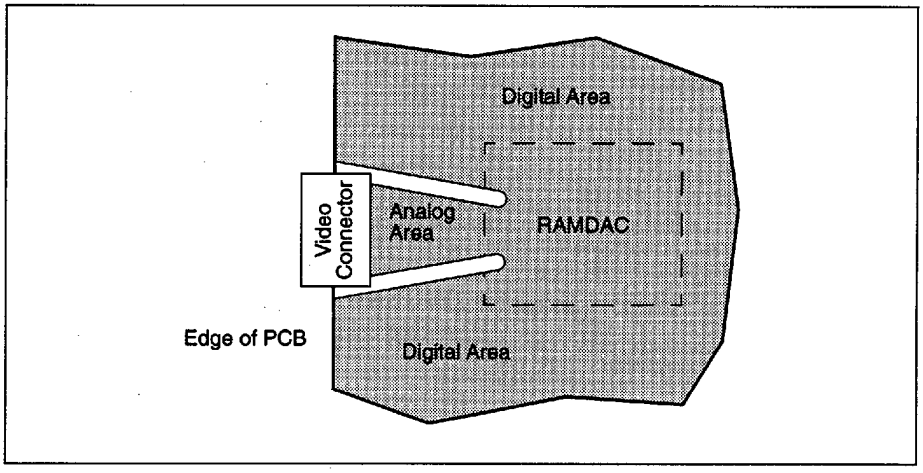
Power and Ground Planes

The power and ground planes need isolation gaps to minimize digital switching noise effects on the analog signals and components. These gaps need to be at least 1/8-inch wide. They are placed so that digital currents cannot flow through a peninsula that contains the analog components, signals, and video connector. A sample layout is shown in Figure 7.

Optionally, a low-resistance ferrite bead may be used, such as Fair-Rite 2743021447.

Figure 7. Sample Layout Showing Power and Ground Plane Isolation Gaps



Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device with short wide traces, and the shortest possible leads (consistent with reliable operation) should be used to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor in parallel with a 0.01 µF chip capacitor, decoupling each of the four groups of VAA pins to GND. The capacitors should be placed as close as possible to the device VAA and GND pins and connected with short, wide traces.

The 10 µF capacitor shown in Figures 8–10 is for low-frequency power supply ripple; the 1 µF and 0.1 µF capacitors are for high-frequency power supply noise rejection.

When a linear regulator is used, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than or equal to 200 mV. This is especially important when a switching power supply is used, and the switching frequency is close to the raster scan frequency. About 10 percent of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

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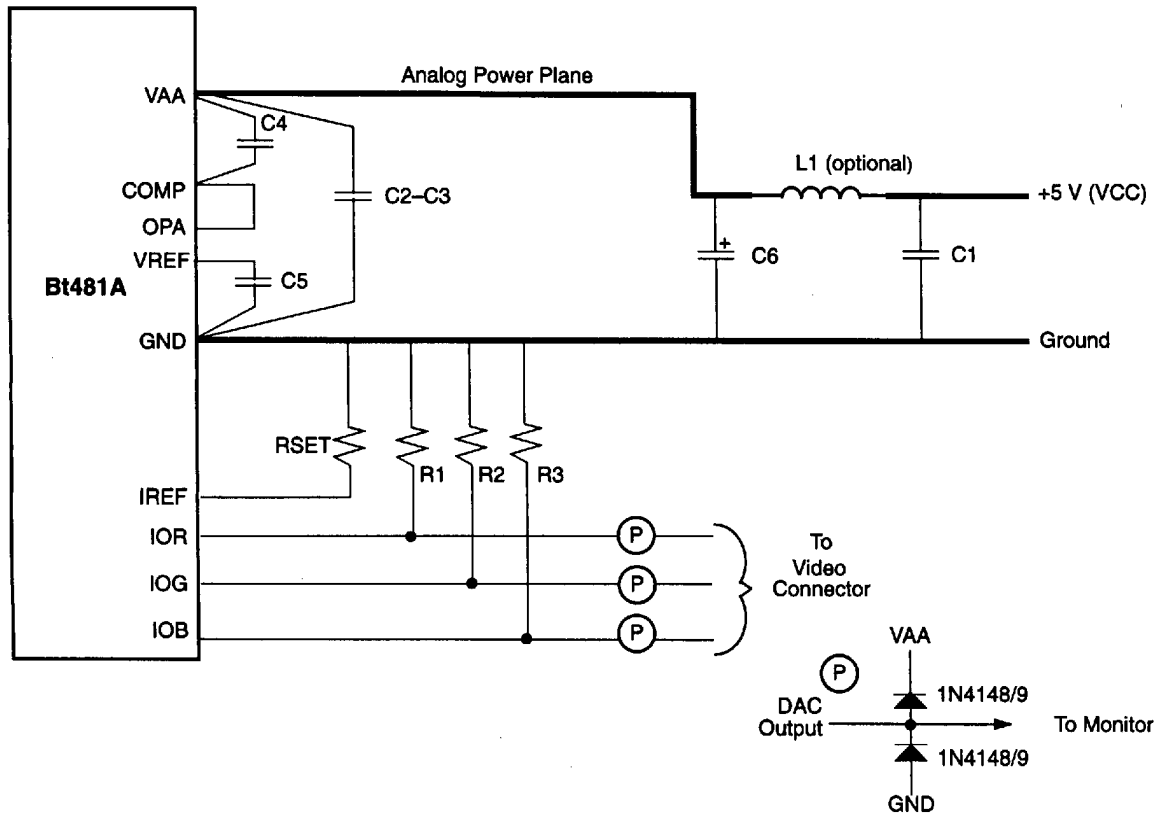
Figure 8. Typical Connection Diagram and Parts List (Internal Voltage Reference)



Note: Each pair of device VAA and GND pins must be separately decoupled.

Location	Description	Vendor Part Number
C1–C5	0.1 µF Ceramic Capacitor	Erie RPE112Z5U104M50V
C6	10 µF Capacitor	Mallory CSR13G106KM
L1	Ferrite Bead	Fair-Rite 2743021447
R1, R2, R3	75 Ω 1% Metal Film Resistor	Dale CMF-55C
RSET	1% Metal Film Resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt481A.

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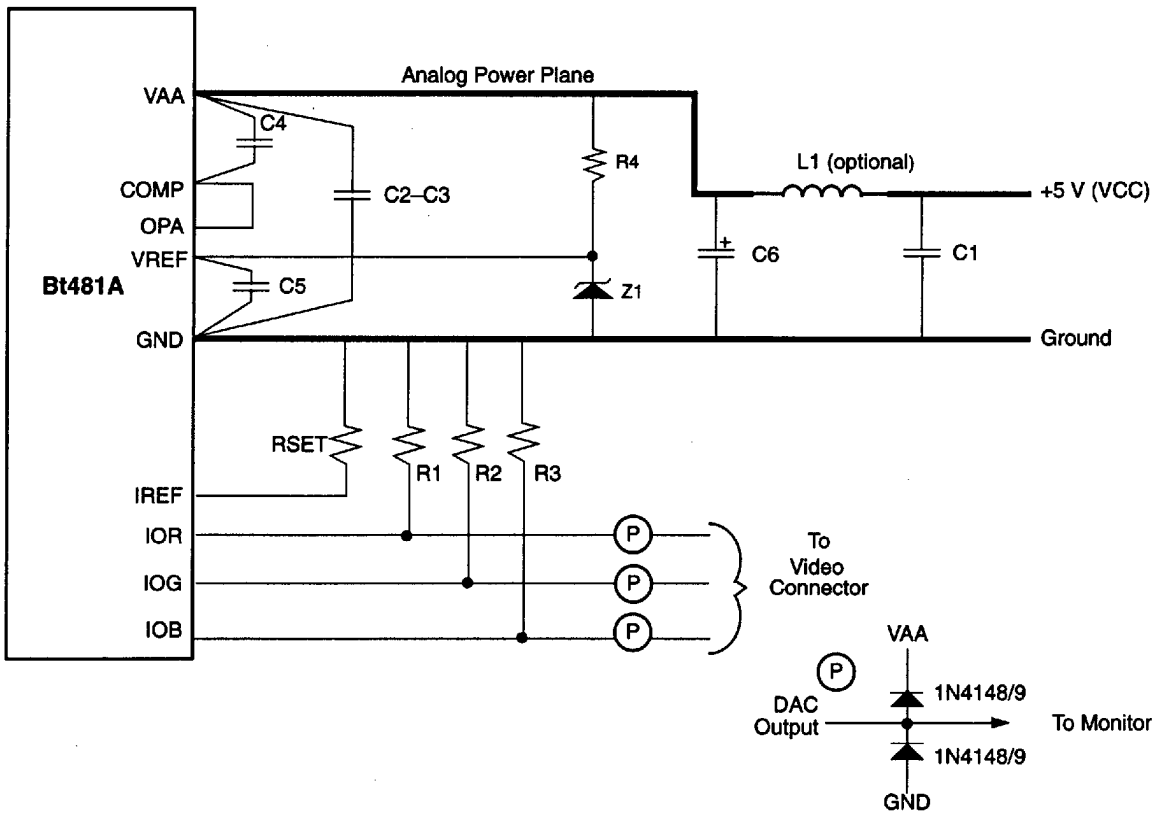
Figure 9. Typical Connection Diagram and Parts List (External Voltage Reference)



Note: Each pair of device VAA and GND pins must be separately decoupled.

Location	Description	Vendor Part Number
C1–C5	0.1 µF Ceramic Capacitor	Erie RPE112Z5U104M50V
C6	10 µF Capacitor	Mallory CSR13G106KM
L1	Ferrite Bead	Fair-Rite 2743021447
R1, R2, R3	75 Ω 1% Metal Film Resistor	Dale CMF-55C
R4	1 kΩ 5% Resistor	
RSET	1% Metal Film Resistor	Dale CMF-55C
Z1	1.2 V Voltage Reference	National Semiconductor LM385BZ-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt481A.

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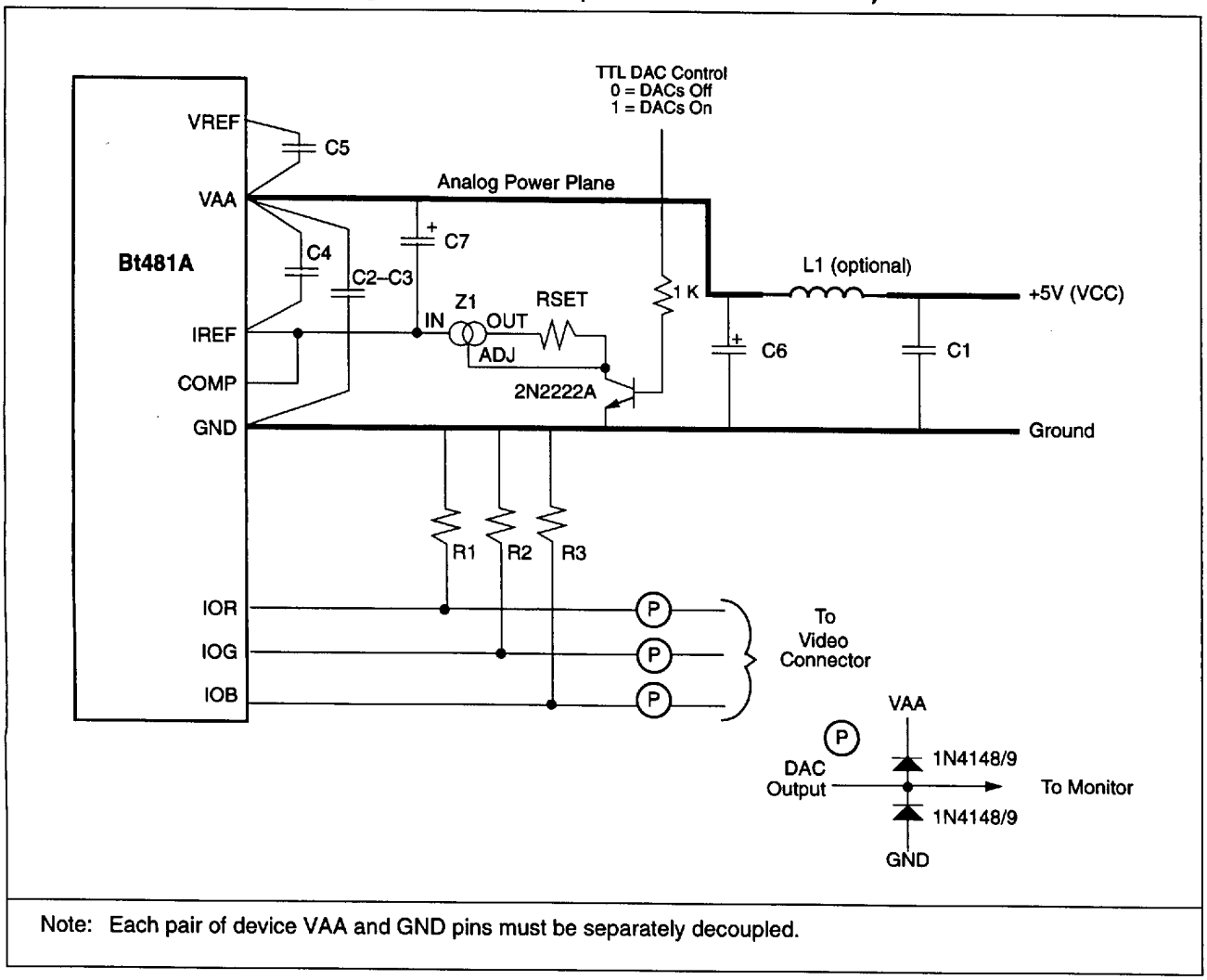
Figure 10. Typical Connection Diagram and Parts List (External Current Reference)



Note: Each pair of device VAA and GND pins must be separately decoupled.

Location	Description	Vendor Part Number
C1–C5	0.1 µF Ceramic Capacitor	Erie RPE112Z5U104M50V
C6	10 µF Capacitor	Mallory CSR13G106KM
C7	1 µF Capacitor	Mallory CSR13G106KM
L1	Ferrite Bead	Fair-Rite 2743021447
R1, R2, R3	75 Ω 1% Metal Film Resistor	Dale CMF-55C
Z1	Adjustable Regulator	National Semiconductor LM385BZ-1.2
RSET	1% Metal Film Resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt481A.

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COMP Decoupling

The COMP pin must be decoupled to the closest VAA pin, typically with a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance. Lead inductance degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

If the display has a ghosting problem, additional capacitance in parallel with the COMP capacitor may help.

VREF Decoupling

A 0.1 µF ceramic capacitor should be used to decouple this input to GND.

Digital Signal Interconnect

The digital inputs to the Bt481A should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should overlay the ground plane, not the analog power or output signals.

Most noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should not be faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower-speed applications will benefit from using lower-speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time (refer to Brooktree Application Notes AN-11 and AN-12). Line termination or line-length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without use of termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω).

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90 degree angle to any analog signals.

Analog Signal Interconnect

The Bt481A should be located as close as possible to the output connectors to minimizes noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the video output signals should overlay the ground plane, not the analog power plane.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and GND should be as close as possible to the Bt481A to minimize reflections. Unused analog outputs should be connected to GND.

Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

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Analog Output Protection

The Bt481A analog output should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching AC-coupled monitors.

The diode protection circuit (as shown in Figures 8, 9, and 10) can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

The clock driver and all other digital devices must be adequately decoupled to prevent noise generated by the digital devices from coupling into the analog circuitry.

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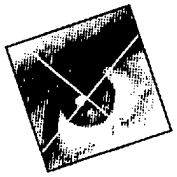

APPLICATION INFORMATION

Using Multiple Devices

When multiple Bt481As are used, each Bt481A should have its own isolated analog power plane. If the internal reference is used, each Bt481A should use its own internal reference.

Although the multiple Bt481As may be driven by a common external voltage/current reference, higher performance may be obtained if each RAMDAC uses its own reference. This will reduce the amount of color channel crosstalk and color palette interaction.

Each Bt481A must still have its own RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and reference capacitors.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. DAC power decoupling networks with large time constants should be avoided. They could delay VAA power to the device. Ferrite beads must be used only for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Reference Selection

An external voltage reference provides about ten times the power supply rejection on the analog outputs than does an external current reference.

Sleep Operation

When the internal or external voltage reference is used, the DACs will be turned off during sleep mode.

When an external voltage reference is used, some internal circuitry will still be powered during the sleep mode, resulting in 0.5 mA of power supply current being drawn (above the rated supply current specifications). This unnecessary current drain can be disabled by turning off the external voltage reference during sleep mode.

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When an external current reference is used, the DACs are not turned off during the sleep mode. To disable the DACs during sleep mode, the current reference must be turned off. As shown in Figure 9, a TTL signal and the 2N2222 transistor are used to disable the current reference during sleep mode.

Initializing the Bt481A

Following is an example of a set-up for the Bt481A.

Command Register A

Pseudo Color (256 bits)
RS2 signal controlled by RS2 pin
Enable access to Command Register B
Enable access to Pixel Mask Register in extended mode
Enable access to Overlay Register in extended mode

Command Register B

Overlay mask enabled
7.5 IRE set-up selected
Sync on Green only
8-bit MPU interface
Normal operation

Control Register Initialization	**RS2, RS1, RS0**
Write $01 to Command Reg. A	110
Write $00 to Palette Addr Reg	000
Write $FF to Read Mask Reg	010
Write $0F to Overlay Mask Reg	010
Write $6A to Command Reg B	010
Color Palette RAM Initialization	
Write $00 to Palette Write Reg	000
Write Red Data to RAM loc. $00	001
Write Grn Data to RAM loc. $00	001
Write Blu Data to RAM loc. $00	001
Write Red Data to RAM loc. $01	001
Write Grn Data to RAM loc. $01	001
Write Blu Data to RAM loc. $01	001
:	
Write Red Data to RAM loc. $FF	001
Write Grn Data to RAM loc. $FF	001
Write Blu Data to RAM loc. $FF	001

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Overlay Palette RAM Initialization	**RS2, RS1, RS0**
Write $00 to Palette Write Reg	100
Write Red Data to RAM loc. $0	101
Write Grn Data to RAM loc. $0	101
Write Blu Data to RAM loc. $0	101
Write Red Data to RAM loc. $1	101
Write Grn Data to RAM loc. $1	101
Write Blu Data to RAM loc. $1	101
:	
Write Red Data to RAM loc. $FF	101
Write Grn Data to RAM loc. $FF	101
Write Blu Data to RAM loc. $FF	101

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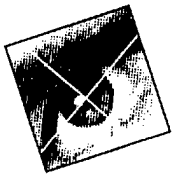

PARAMETRIC INFORMATION

DC Electrical Parameters

Table 10. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ω
External Reference Voltage	VREF		1.235		V

Table 11. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	V
Voltage on any Signal Pin(1)		GND – 0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		Indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Notes: (1). This device employs high impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

2. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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Table 12. DC Characteristics *(1 of 2)*

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)		6 8	6 8	6 8	Bits Bits
Accuracy (each DAC)					
Integral Linearity Error	IL			±1	LSB
Differential Linearity Error	DL			±1	LSB
Monotonicity			Guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	GND – 0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)[1]	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		5		pF
Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	V
3-State Current	IOZ			50	µA
Output Capacitance	CDOUT		5		pF
Analog Outputs					
Gray Scale Current Range				20	mA
Output Current					
White Level Relative to Black[2]					
Using External Vref = 1.235 V		16.74	17.62	18.50	mA
Using Internal Vref		15.66	17.02	18.55	mA
Black Level Relative to Blank					
Setup = 7.5 IRE		0.95	1.44	1.90	mA
Setup = 0 IRE		0	5	50	µA
Blank Level					
Sync Enabled		6.29	7.62	8.96	mA
Sync Disabled		0	5	50	µA
Sync Level		0	5	50	µA
LSB Size			69.1		µA

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Table 12. DC Characteristics *(2 of 2)*

Parameter	Symbol	Min	Typ	Max	Units
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	–0.3		+1.5	V
Output Impedance	RAOUT		10		k Ω
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT		18		pF
Power Supply Rejection Ratio[3] (COMP = 0.1 µF, f = 1 kHz	PSRR			0.5	% / % Δ VAA

Notes: (1). Maximum Input Low Current for pin 6*/8 is –40 µA. (Vin = 0.4 V)
(2). When the Bt481A is in the 6-bit mode, the output levels are approximately 1.5% lower than these values. White level current is tested using internal Vref. White level current using external Vref is guaranteed by characterization and is not production tested.
(3). Guaranteed by characterization, not tested.
4. Test conditions to generate RS-343A standard video signals (unless otherwise specified): "Recommended Operating Conditions" and external voltage reference with RSET = 147 Ω, VREF = 1.235 V, SETUP = 7.5 IRE, and 6*/8 pin = logical one. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, and nominal voltage, i.e., 5 V.

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AC Electrical Parameters

Table 13. AC Characteristics *(1 of 2)*

Parameter	Symbol	110 MHz Devices			Units
		Min	Typ	Max	
Input Clk Rate Pseudo Color	Fmax			110	MHz
Input Clk Rate 15-, 16-bit dual-edge clk	Fmax			66	MHz
Input Clk Rate 15-, 16-bit single-edge clk	Fmax			100	MHz
Input Clk Rate 32-bit dual-edge clk	Fmax			66	MHz
Input Clk Rate 24-bit single-edge clk	Fmax			100	MHz
RS[2:0] Setup Time	1	10			ns
RS[2:0] Hold Time	2	10			ns
RD* Asserted to Data Bus Driven	3	2			ns
RD* Asserted to Data Valid	4			40	ns
RD* Negated to Data Bus 3-Stated	5			20	ns
Read Data Hold Time	6	2			ns
Write Data Setup Time	7	10			ns
Write Data Hold Time	8	10			ns
RD*, WR* Pulse Width Low	9	50			ns
RD*, WR* Pulse Width High	10	6*p13			ns
Pixel and Control Setup Time	11	3			ns
Pixel and Control Hold Time (Pseudo Color and 15-, 16-, and 24-bit Single-Edge Clock Mode)	12	3			ns
Pixel and Control Setup Time	20	–1			ns
Pixel and Control Hold Time (15-, 16-, and 32-bit Dual-Edge Clock Mode, LSB and MSB)	21	7			ns
Clock Cycle Time (Pseudo Color Mode)	13	9.09			ns
Clock Pulse Width High Time(1)	14	3.5			ns
Clock Pulse Width Low Time(1)	15	3.5			ns
Clock Cycle Time (Single Edge True-Color Modes)	13	10			ns
Clock Pulse Width High Time(1)	14	3.5			ns
Clock Pulse Width Low Time(1)	15	3.5			ns

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Table 13. AC Characteristics *(2 of 2)*

Parameter	Symbol	110 MHz Devices			Units
		Min	Typ	Max	
Clock Cycle Time (Dual-Edge Clock)	13	15.15			ns
Clock Pulse Width High Time(1)	14	6.5			ns
Clock Pulse Width Low Time(1)	15	6.5			ns
Analog Output Delay	16			30	ns
Analog Output Rise/Fall Time	17		3		ns
Analog Output Settling Time(2)	18		13		ns
Clock and Data Feedthrough(2)			–30		dB
Glitch Impulse(2)			75		pV - sec
DAC-to-DAC Crosstalk			_23		dB
Analog Output Skew				2.5	ns
SENSE* Output Delay	19		1		µS
VAA Supply Current	IAA				
Normal Operation(3)				300	mA
Sleep Enabled(4)			2		mA
Pipeline Delay					Clocks
Pseudo Color		7	7	7	
5:5:5 Dual-Edge Clock Mode		7	7	7	
5:6:5 Dual-Edge Clock Mode		7	7	7	
8:8:8:8 Dual-Edge Clock Mode		8	8	8	
5:5:5 Single-Edge Clock Mode		8	8	8	
5:6:5 Single-Edge Clock Mode		8	8	8	
8:8:8 Single-Edge Clock Mode		9	9	9	

Notes: (1). These pulse widths are specified at VIL = 0.8 V for clock pulse width low and VIH = 2.0V for clock pulse width high. Minimum clock pulse width is not production tested and is guaranteed by characterization.

(2). Clock and data feedthrough is a function of the number of edge rates, and the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2 x clock rate.

(3). At Fmax. IAA (typ) at VAA = 5.0 V. IAA (max) at VAA (max).

(4). External current or voltage reference disabled during sleep mode. Test Conditions: +25° to +70° C, pixel and data ports at 0.4 V.

5. Test conditions (unless otherwise specified): "Recommended Operating Conditions" and external voltage reference with RSET = 147 Ω, VREF= 1.235, SETUP = 7.5 IRE, and 6*/8 pin = logical one. TTL input values are 0–3 V with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points are at 50% for inputs and outputs unless otherwise noted. Analog output load ≤ 10 pF. SENSE*, D[7:0] output load ≤ 75 pF. See the Timing Waveforms section. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

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Timing Waveforms

Figure 11. MPU Read/Write Timing

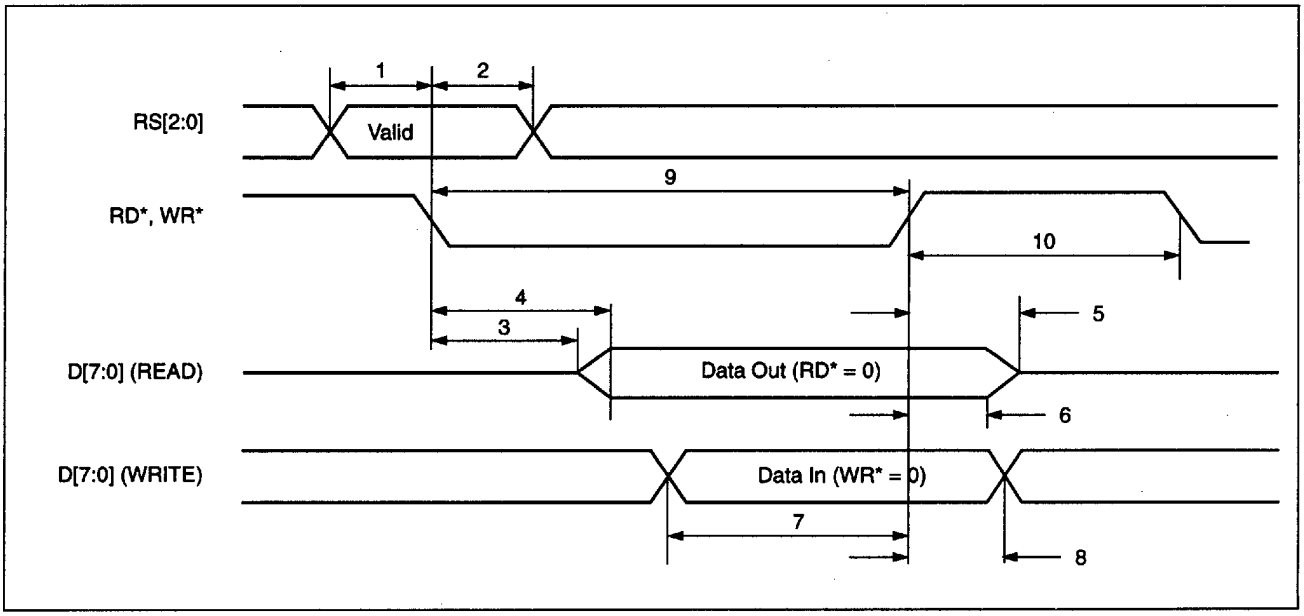

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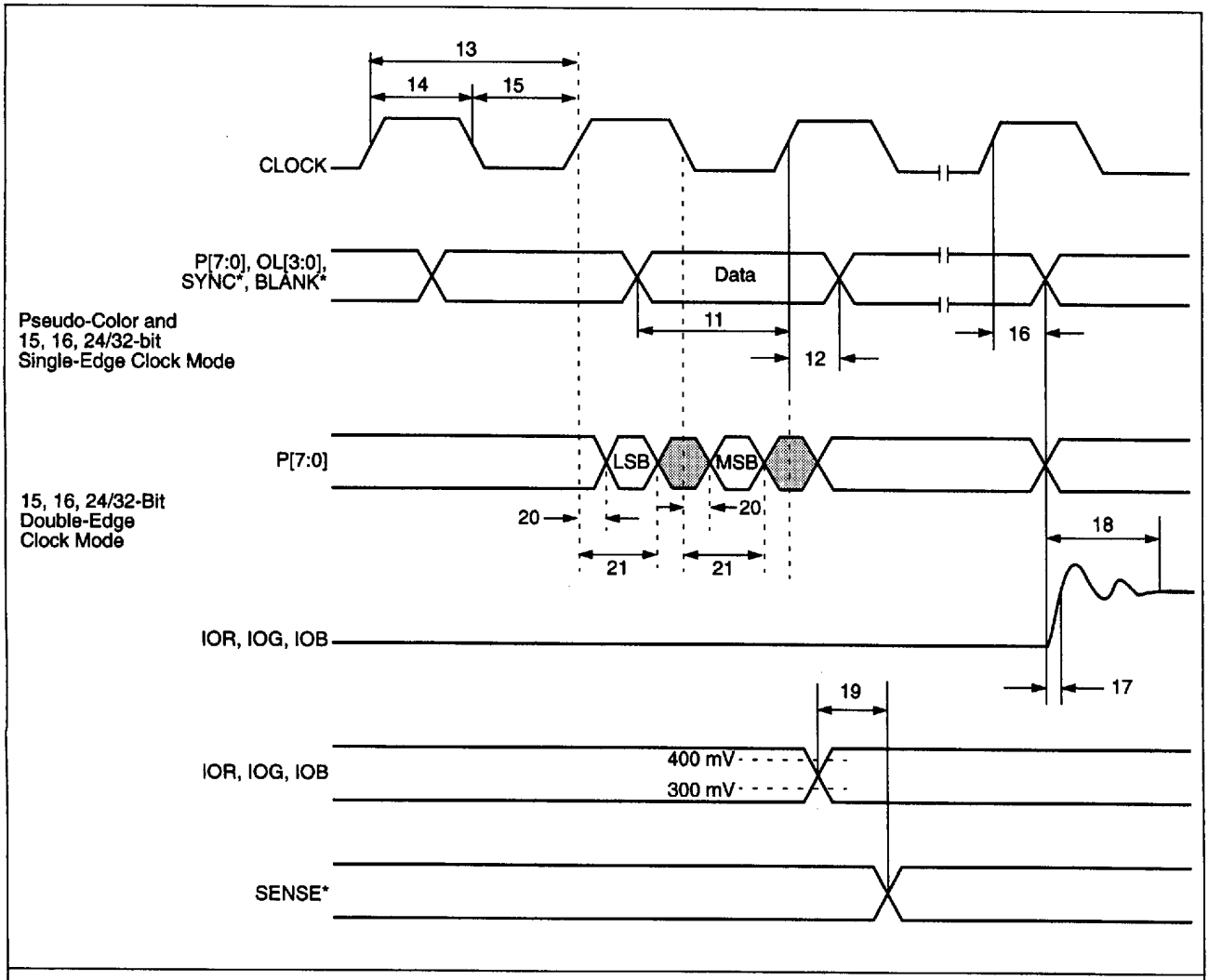
Figure 12. Video Input/Output Timing



Notes:
1. Output delay is measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition.
2. Settling time is measured from the 50% point of full-scale transition to the output remaining within ±1 LSB.
3. Output rise/fall time is measured between the 10% and 90% points of full-scale transition.

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Figure 13. 15-, 16-, and 24-Bit-Per-Pixel (RGB) Timing, Dual-Edge Clock Mode

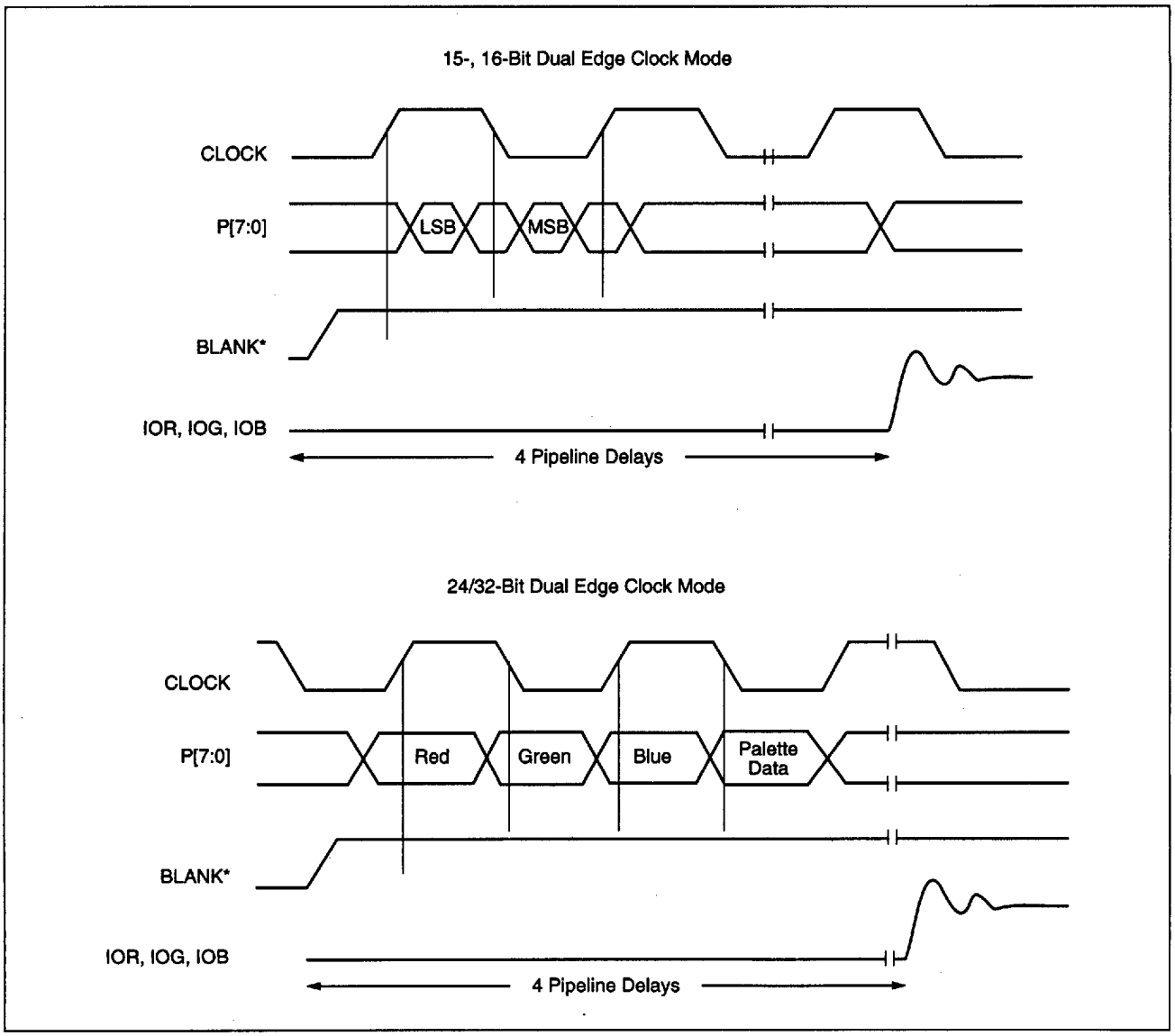

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Figure 14. 15-, 16-, and 32-Bit-Per-Pixel (BGR) Timing, Dual-Edge Clock Mode

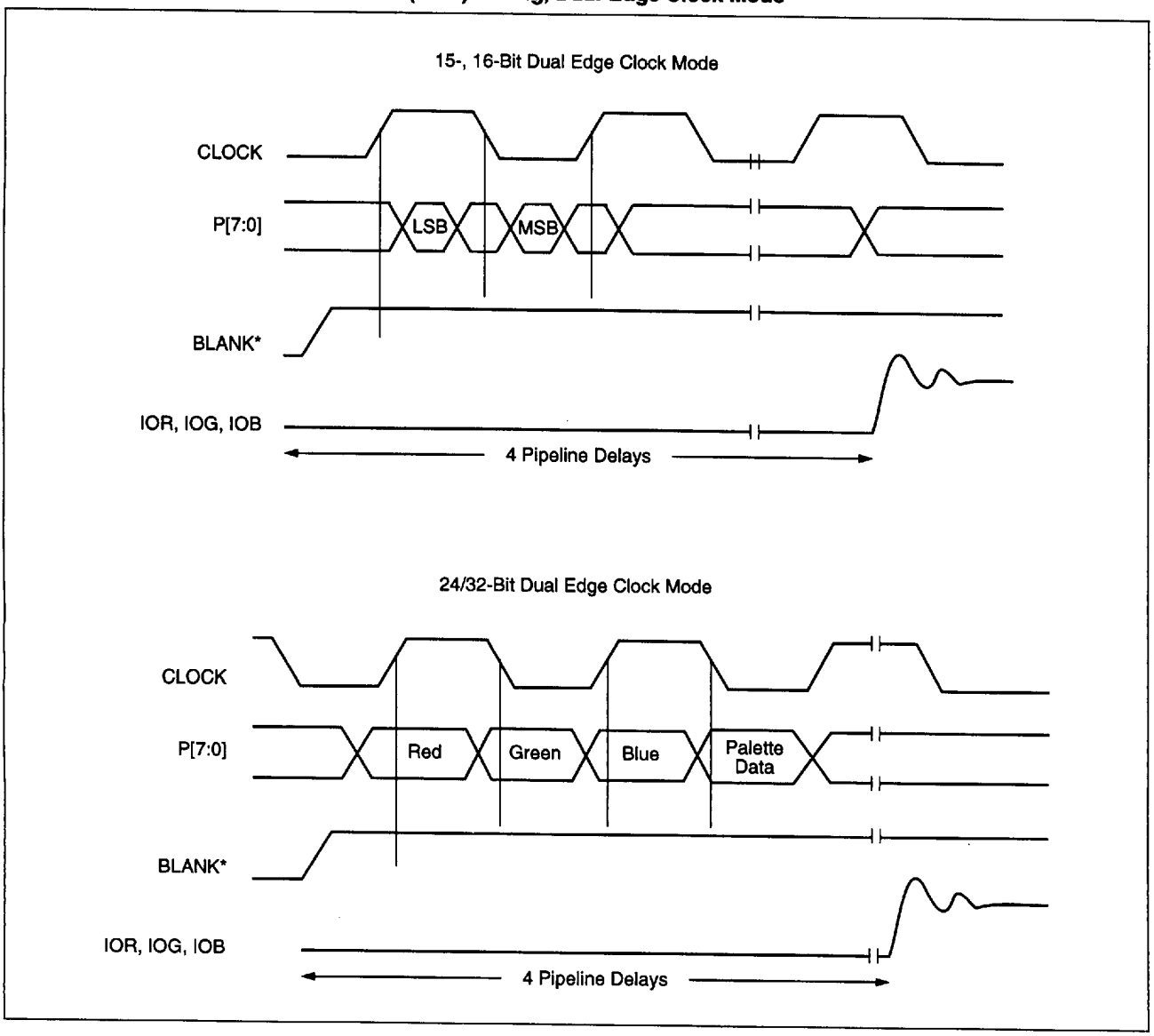

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Figure 15. 15-, 16-, and 24-Bit-Per-Pixel (RGB) Timing, Single-Edge Clock Mode

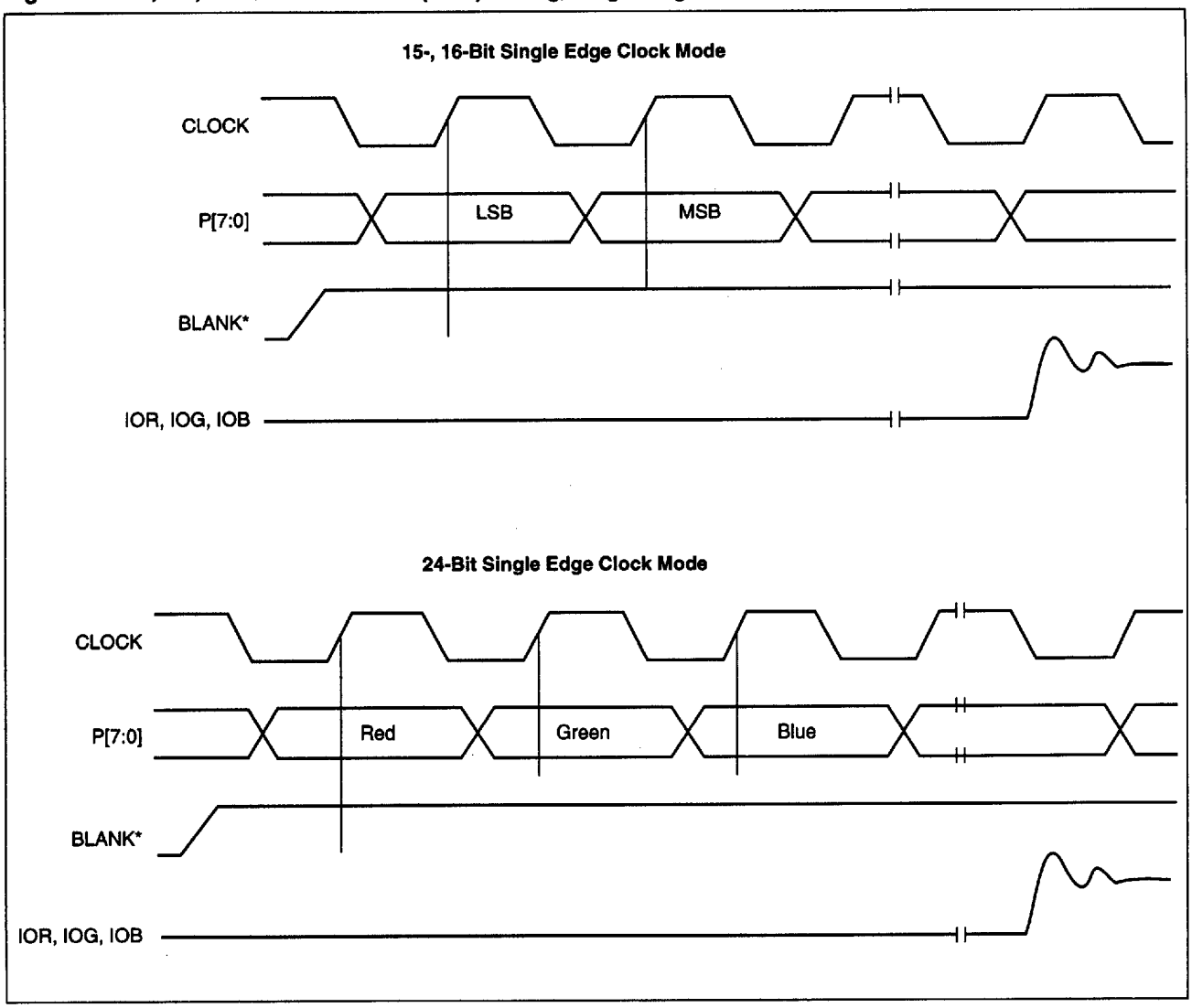

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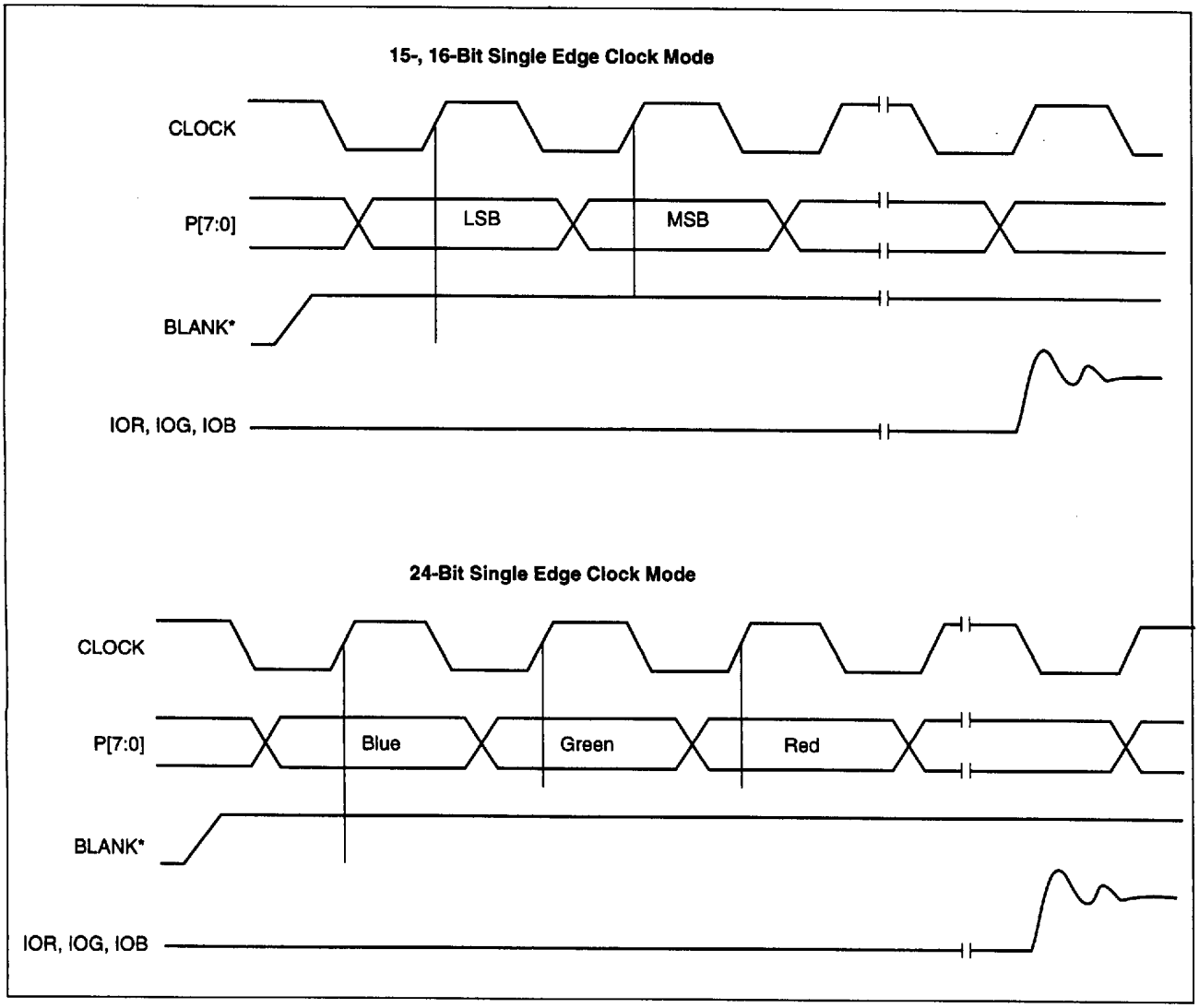
Figure 16. 15-, 16-, and 24-Bit-Per-Pixel (BGR) Timing, Single-Edge Clock Mode



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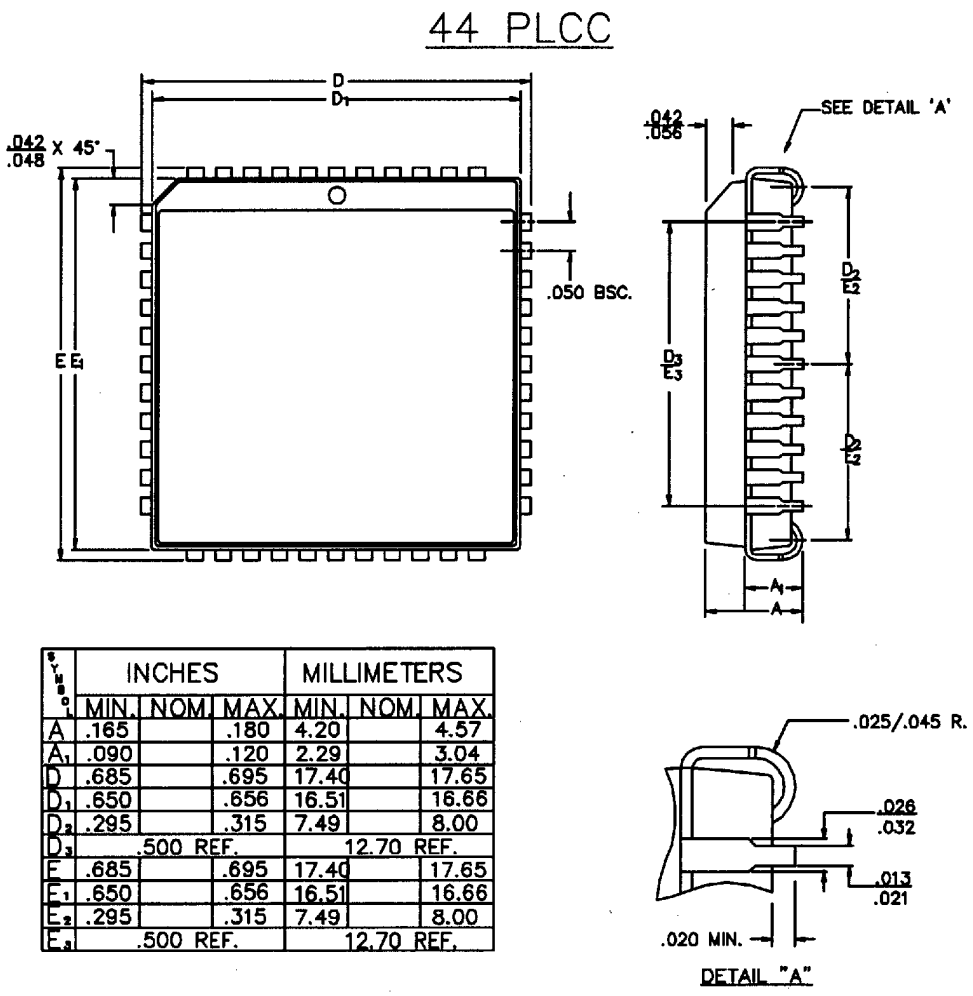
Package Drawing

Figure 17. 44-Pin Plastic J-Lead (PLCC)



SYMBOL	INCHES			MILLIMETERS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	.165		.180	4.20		4.57
A_1	.090		.120	2.29		3.04
D	.685		.695	17.40		17.65
D_1	.650		.656	16.51		16.66
D_2	.295		.315	7.49		8.00
D_3	.500 REF.			12.70 REF.		
E	.685		.695	17.40		17.65
E_1	.650		.656	16.51		16.66
E_2	.295		.315	7.49		8.00
E_3	.500 REF.			12.70 REF.		

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Revision History

Revision	Changes from Previous Revision
A	Advance Release.
B	Removed 85 MHz operation from datasheet.
C	PC Board Layout Considerations section revised. Addition of Initialization information to Applications section.

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