T-52-33-43

Preliminary Information

This document contains information on new product. The parametric information, although not fully characterized, is the result of testing initial devices.

Bt481

Bt482

256-Word Color Palette 15-, 16-, and 24-bit True Color Power-Down RAMDACs™

4

Distinguishing Features

- 85 and 75 MHz Operation
- Supports 8:8:8:8, 24-bit True Color and VGA Overlay
- Supports 8:8:8 24-bit True-Color Format
- Supports 5:6:5 XGA True-Color Format
- Supports 5:5:5 TARGA True-Color Format
- 32 x 32 x 2 User-Definable Hardware Cursor
- Bt471/475/476/477/478 Pin Compatible
- Power-On-Reset for Internal Registers
- Power-Down Mode
- Antisparkle Circuitry
- Analog Output Comparators
- Triple 6-bit (8-bit) D/A Converters
- 256 x 18 (24) Color Palette RAM
- 3 x 18 (24) Cursor Color Palette
- 15 x 18 (24) Overlay Registers
- Optional Internal Voltage Reference
- Programmable Pedestal
- Sync on all Three Channels
- Standard MPU Interface
- 44-pin PLCC Package

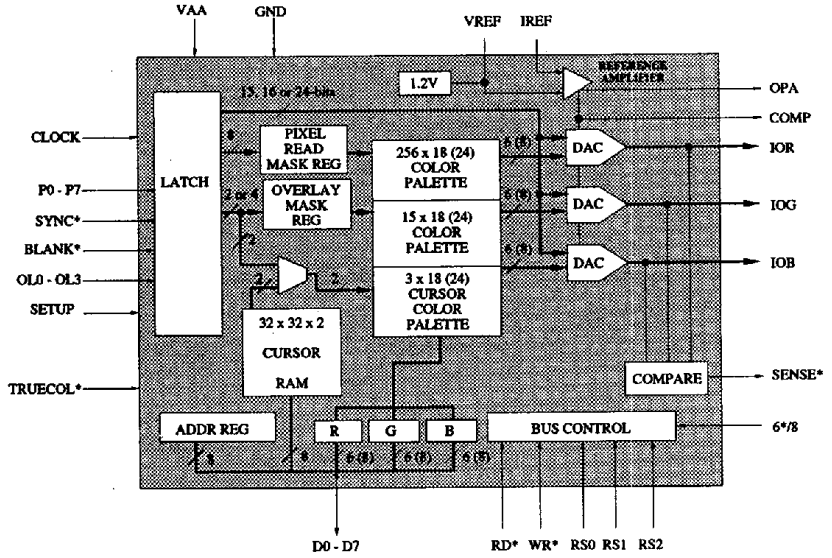
Applications

- High-Resolution Color Graphics
- CAE/CAD/CAM
- Image Processing
- Instrumentation
- Desktop Publishing
- Laptop Computers

Related Products

- Bt471
- Bt475
- Bt476
- Bt477
- Bt478

Functional Block Diagram



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L482001 Rev. C

4-121

Product Description

The Bt481 and Bt482 RAMDACs are designed specifically for high-performance color graphics.

Both the Bt481 and Bt482 support three true-color modes: 15-bit (5:5:5, 32K colors) TARGA format, 16-bit (5:6:5, 65K colors) XGA format, and 24-bit (8:8:8, 16.8M colors) true-color format. They also support 8-bit pseudo-color format (256 colors).

The Bt482 has a 256 x 18(24) lookup table RAM, 15x18(24) overlay registers, 32 x 32 x 2 user-definable cursor, 4 x 24 cursor color palette and triple 8-bit D/A converters. Both 6-bit and 8-bit color modes are supported. The Bt481 is identical to the Bt482, but the Bt481 has no 32 x 32 x 2 cursor RAM. Both devices can support an external cursor. External cursor data is routed through the 3 x 24 cursor color palette to provide three modes for color selection. Mode 1 is a three-color cursor, Mode 2 is referred to as PM/Window or XGA cursor, and Mode 3 is referred to as an X-Windows cursor.

A power-down mode is available on both the Bt481 and the Bt482 to reduce power requirements when the analog outputs are not used. This is useful in laptop computer systems that require the option to drive an external RGB monitor.

Both the Bt481 and the Bt482 have on-chip analog output comparators to simplify diagnostics and debugging, with the result output onto the SENSE* pin. Also included

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Product Description *(continued)*

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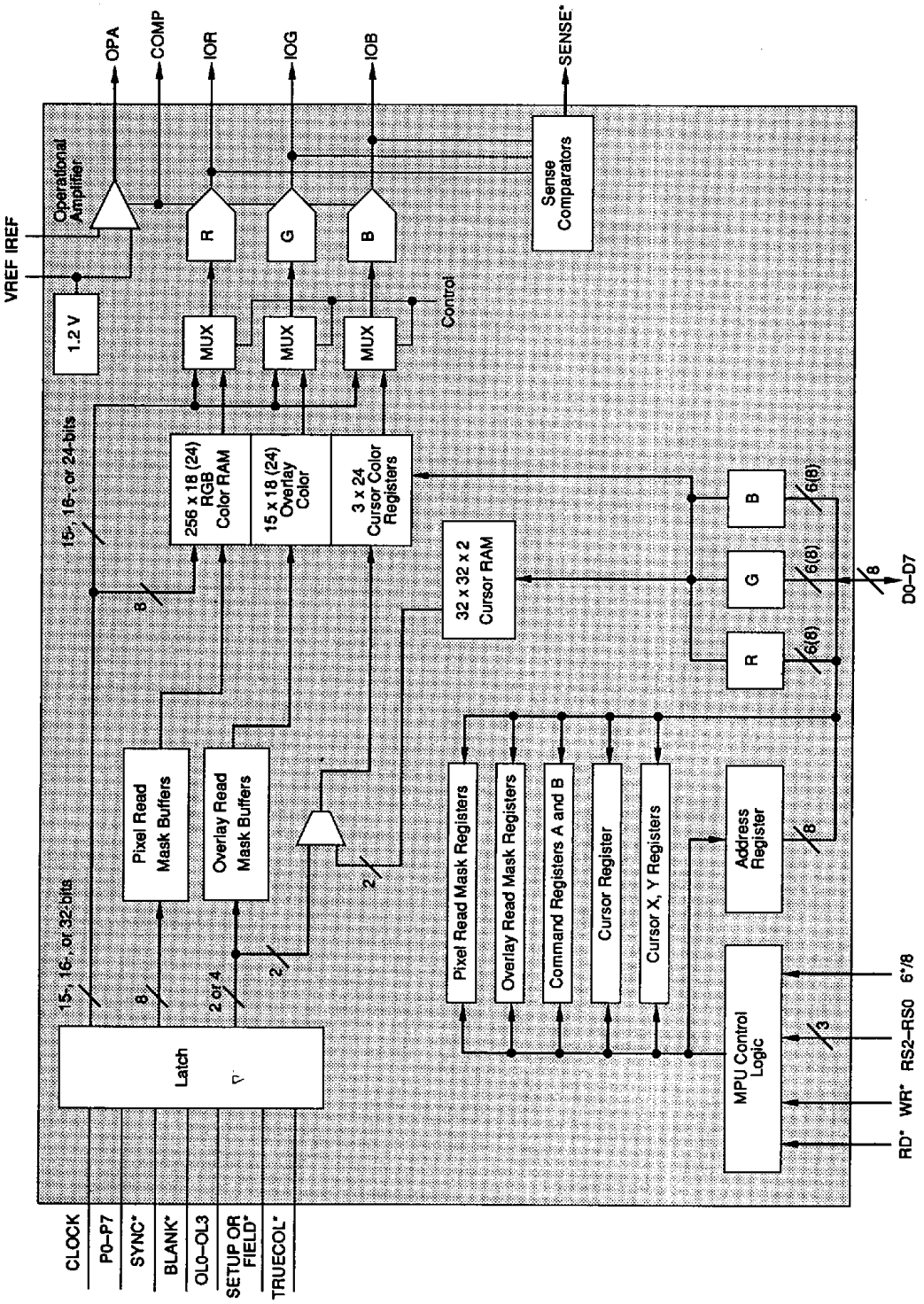
is an on-chip voltage reference to simplify use of the device.

On power-up, the Bt481 and Bt482 behave as the Bt471 or Bt478, including their antisparkle capabilities, on-chip voltage reference, and analog output comparators. A power-on reset is available on the Bt481/482 devices to initialize internal registers.

The Bt481 and Bt482 generate RS-343-compatible video signals into a doubly-terminated 75 Ω load.



Detailed Block Diagram.

Circuit Description

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MPU Interface

As illustrated in the functional block diagram, the Bt481 and Bt482 support a standard MPU bus interface, allowing the MPU direct access to the color palette RAM and overlay color registers.

The RS0–RS2 select inputs specify whether the MPU is accessing the address register, color palette RAM, overlay registers, or read mask register, as shown in Table 1. The 8-bit address register addresses the color palette RAM and overlay registers, eliminating the requirement for external address multiplexers. ADDR0 corresponds to D0 and is the least significant bit.

Writing Color Palette RAM Data

To write color data, the MPU writes the address register (RAM write mode) with the address of the color palette RAM location to be modified. The MPU performs three successive write cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM. After the blue write cycle, the 3 bytes of color information are concatenated into an 18-bit or 24-bit word and written to the location specified by the address register. The address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous RGB write cycles until the entire block has been written.

Reading Color Palette RAM Data

To read color palette RAM data, the MPU loads the address register (RAM read mode) with the address of the color palette RAM location to be read. The contents of the color palette RAM at the specified address are copied into the RGB registers, and the address register is incremented to the next RAM location. The MPU performs three successive read cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select the color palette RAM. Following the blue read cycle, the contents of the color palette RAM at the address specified by the address register are copied into the RGB registers and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous RGB read cycles until the entire block has been read.

Writing Overlay and Cursor Color Data

To write overlay or cursor color data, the MPU writes the address register (overlay write mode) with the address of the overlay or cursor color location to be modified. The MPU performs three successive write cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select the overlay or cursor color registers. After the blue write cycle, the 3 bytes of color information are concatenated into an 18-bit or 24-bit word and written to the overlay or cursor color location specified by the address register. The address register then increments to the next location, which the MPU may modify by writing another sequence of red, green, and blue data. A block of color values in consecutive locations may be written to by writing the start address and performing continuous RGB write cycles until the entire block has been written. In order to write the cursor color registers, bit CR3 in the cursor register must be a logical zero (see Table 2).

Reading Overlay and Cursor Color Data

To read overlay or cursor color data, the MPU loads the address register (overlay read mode) with the address of the overlay or cursor color location to be read. The contents of the overlay or cursor color register at the specified address are copied into the RGB registers, and the address register is incremented to the next overlay or cursor color location. The MPU performs three successive read cycles (6 or 8 bits each of red, green, and blue), using RS0–RS2 to select the overlay or cursor color registers. Following the blue read cycle, the contents of the overlay or cursor color location at the address specified by the address register are copied into the RGB registers and the address register again increments. A block of color values in consecutive locations may be read by writing the start address and performing continuous RGB read cycles until the entire block has been read. In order to read the cursor color registers, bit CR3 in the cursor register must be a logical zero (see Table 2).

RS2	RS1	RS0	Addressed by MPU
0	0	0	address register (palette & cursor RAM write mode)
0	1	1	address register (palette & cursor RAM read mode)
0	0	1	color palette RAM
0	1	0	pixel read mask register
1	0	0	address register (overlay & cursor color write mode)
1	1	1	address register (overlay & cursor color read mode)
1	0	1	overlay registers
1	1	0	command register A

Table 1. Control Input Truth Table.

Circuit Description *(continued)*

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	Value	RS2	RS1	RS0	CR3	Addressed by MPU
ADDRa, b (counts modulo 3)	00 01 10					red value green value blue value
ADDR0–7 (counts binary)	$00–$FF	0	0	1	x	color palette RAM
	0000 0000	1	0	1	x	reserved
	0000 0001	1	0	1	x	overlay color 1
	:	:	:	:	:	:
	0000 1111	1	0	1	x	overlay color 15
	0001 0000	1	0	1	0	reserved
	0001 0001	1	0	1	0	cursor color register 1
	0001 0010	1	0	1	0	cursor color register 2
	0001 0011	1	0	1	0	cursor color register 3
	$00–$FF	1	0	1	1	cursor RAM

Table 2. Address Register (ADDR) Operation.

15-, 16-, and 24/32-Bits-per-Pixel Operation

When the 15-, 16-, or 24/32-bit per pixel modes are activated (see Command Register A in the Internal Registers section), the inputs accept 16, 24, or 32 bits of pixel information from the 8-pin pixel port P0–P7. The 8-bit inputs form a 16- or 24-bit pixel (B15–0/B23–B0) to directly drive the 8-bit triple video DACs. The color lookup table and the read mask register are bypassed. Internally, the unused LSBs of all DACs are forced to zero in 15- or 16-bits-per-pixel modes. The 16- and 24-bit word (B15–0/B23–B0) is assigned to the DACs in the following format:

8:8:8:8 True-Color Format	5:6:5 XGA Format	5:5:5 TARGA Format	Comments
		B15	Ignored
B7 – B0	B15 – B11	B14 – B10	Red DAC
B15 – B8	B10 – B5	B9 – B5	Green DAC
B23 – B16	B4 – B0	B4 – B0	Blue DAC
B31 – B24			Palette or Masked

15-, 16-, and 24-Bits-per-Pixel Dual-Edge Clock

In the 15- and 16-bit-per-pixel dual-edge clock mode (see the command register bits A7–A4 description in the Internal Registers section), the least significant byte is latched on the rising edge of the pixel clock when BLANK* high is latched. Also in this mode, the most significant byte is latched on the falling edge of the pixel clock when BLANK* high is latched. Therefore, only one input clock period is required to load a 16-bit pixel.

In the 32-bit-per-pixel dual-edge clock mode, 32 bits of data, 24 bits of true color and 8 bits of palette index are latched on two rising and two falling edges. Therefore, only two input clock cycles are required to load a 32-bit pixel. If palette indexing is not required, logical zeros can be written for the palette overlay data, as *location zero in the palette RAM cannot be accessed in this mode*. Or palette overlay data can be masked out through the pixel read mask register. If the palette index data is not a logical zero or masked, the data will address any one of 255 locations in the palette RAM. Palette data has priority over bypass data.

15-, 16-, and 24-Bits-per-Pixel Single-Edge Clock

In the 15- and 16-bit-per-pixel single-edge clock mode (see Command Register A in the Internal Registers section), the inputs accept 16 bits of information by using two input clock cycles. The least significant byte is latched on the first rising edge of the input clock, and the most significant byte is latched on the second rising edge of the input clock. The bytes are synchronized with the BLANK* signal. The first byte latched after BLANK* goes high is the least significant byte. Since a pixel is latched in two clock cycles, the input clock must be twice as fast as the internal pipeline clock. The Bt481 and Bt482 each have an internal divider to generate the pipeline clock from the input clock.

In the 24-bit-per-pixel single-edge clock mode, the inputs accept 24 bits of pixel data by using three input clock cycles. The red byte is latched on the first rising edge of the pixel clock when BLANK* high is latched. The next two clock cycles latch the green and blue bytes. Since a 24-bit pixel is

Circuit Description *(continued)*

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latched in three input clock cycles, the input clock must be three times as fast as the internal pipeline clock. The Bt481 and Bt482 each have an internal divider to generate the pipeline clock from the pixel input clock. Palette data has priority over bypass data.

Additional Information

When the MPU is accessing the color palette RAM, the address register resets to $00 following a blue read or write cycle to RAM location $FF. While the MPU is accessing the overlay color registers, the 4 most significant bits of the address register (ADDR4–7) are ignored.

The MPU interface operates asynchronously to the pixel clock. Data transfers between the color palette RAM/overlay registers and the color registers (R, G, and B in the block diagram) are synchronized by internal logic. Data transfers take place in the period between MPU accesses. To reduce noticeable sparkling on the CRT during MPU access to the color palette RAMs, internal logic maintains the previous output color data on the analog outputs while the transfer between lookup table RAMs and the RGB registers occurs.

To keep track of the red, green, and blue read/write cycles, the address register has 2 additional bits (ADDRa and ADDRb) that count modulo three, as shown in Table 2. They are reset to zero when the MPU writes to the address register and are not reset to zero when the MPU reads the address register. The MPU does not have access to these bits. The other 8 bits of the address register, incremented following a blue read or write cycle (ADDR0–7), are accessible to the MPU. These bits are used to address color palette RAM locations and overlay registers, as specified in Table 2. The MPU may read the address register at any time without modifying its contents or the existing read/write mode. *The pixel clock must be active for MPU accesses to the color palette RAM.*

Accessing Cursor Control Registers and Control Register B

A cursor register, CR; four cursor position registers; and a second control register, B, were defined to control the cursor, setup select, 6- or 8-bit select, and the sleep modes of the Bt481/482. Since there are only three register select lines (and all eight combinations have already been used), the cursor register; cursor X,Y registers; and Command Register B must be accessed indirectly.

For example, the cursor register is accessed with the following sequence of operations:

1. Set RS2 – RS0 = 110 in Command Register A.
2. Write a logical one to command register bit A0.
3. Set RS2 – RS0 = 000 in address register write mode.
4. Write address register to 0000 0011.
5. Set RS2 – RS0 = 010 in read mask register.
6. Read or write cursor register.

Table 3 contains specifications to indirectly address other registers.

Accessing Command Registers without the RS2 line

When the cursor or overlay functionality of the Bt481/482 is not used and the Register Select Line 2 (RS2) must be tied low at all times, the command registers of the Bt481/482 can still be accessed.

A flag will be set when the pixel read mask register (RS1 = 1 and RS0 = 0) is read four times consecutively. The next write to the pixel read mask register will be directed to Command Register A and can be used to set the bits in that register. Any access of the command register thereafter will also require four consecutive reads to the pixel read mask register. A write to any address or a read to any address other than the pixel read mask register will reset the flag.

When the extended registers are accessed (Bit A0 = 1), this feature is disabled.

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Accessing the Cursor RAM Array (Bt482 only)

The 32 x 32 x 2 cursor RAM is accessed in a planar format. In the planar format only 7 address bits are used. The eighth bit determines which plane (0 or 1) data of the cursor RAM array is accessed. A single address presented to the cursor RAM accesses eight bit locations in plane 0 or 1, depending on the state of address bit 7.

After each access in the planar format, the address increments. The MPU uses ADDR, a binary address counter, to access the cursor RAM array (see Table 2). ADDR is the same binary counter used for RGB autoincrementing. Any write to ADDR after cursor autoincrementing has been initiated resets the cursor autoincrementing logic until cursor RAM array has again been accessed. Cursor autoincrementing will then begin from the address written. A read from the ADDR does not reset the cursor autoincrementing logic. To access the 32 x 32 x 2 cursor RAM, a logical one must be written to bit CR3 in the cursor register. The cursor register must be indirectly accessed.

Cursor Operation (Bt482 only)

The Bt482 has an on-chip, three-color, 32 x 32 x 2 pixel user-definable cursor. This cursor works with both interlaced and noninterlaced systems.

The pattern for the cursor is provided by the cursor RAM, which may be accessed by the MPU at any time. The cursor is positioned through the cursor position register (Xp,Yp) (see Figure 1). A (0,0) written to the cursor position registers will place the cursor completely offscreen. A (1,1) written to the cursor position registers will place the lower right pixel of the cursor on the upper left corner of the screen. Only one cursor pattern per frame is displayed at the location specified for both interlaced and noninterlaced display formats, regardless of the number of updates to (Xp,Yp). The cursor's vertical or horizontal location is not affected during any frame displayed. There are no restrictions on updating (Xp,Yp) other than both cursor position registers must be written when the cursor location is updated. Internal x and y position regis-

Circuit Description *(continued)*

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	Value	RS2	RS1	RS0	Bit A0	Registers
ADDR 0–7 (counts binary)	0000 0000	0	1	0	1	Read Mask Register
	0000 0001	0	1	0	1	Overlay Mask Register
	0000 0010	0	1	0	1	Command Register B
	0000 0011	0	1	0	1	Cursor Register
	0000 0100	0	1	0	1	Cursor X Low Register
	0000 0101	0	1	0	1	Cursor X High Register
	0000 0110	0	1	0	1	Cursor Y Low Register
	0000 0111	0	1	0	1	Cursor Y High Register

Table 3. Indirect Register Addressing Truth Table.

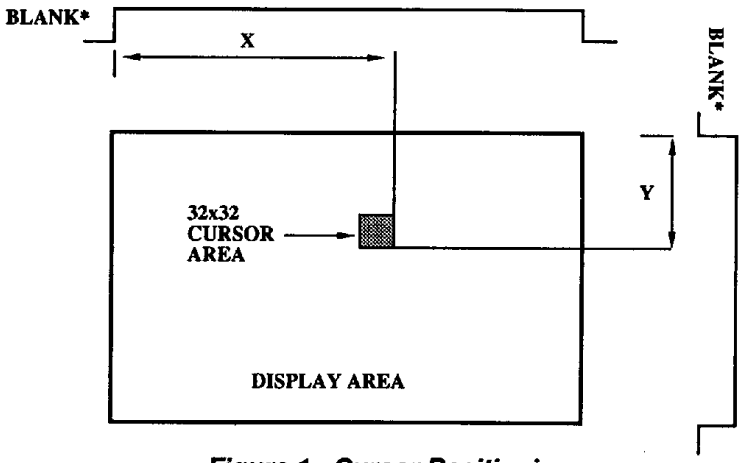

Figure 1. Cursor Positioning.

ters are loaded after the upper byte of Yp has been written to ensure one cursor pattern per frame at the correct location. The cursor pattern is displayed at the last cursor location written. Cursor positioning is relative to BLANK* (see Figure 1). The reference point of the cursor, row 0, column 0, is in the lower right corner. The cursor Xp position is relative to the first rising edge of pixel clock when BLANK* is sampled at logical one. The cursor Yp position is relative to the first rising edge of pixel clock when BLANK* is sampled at logical one after the vertical blanking interval has been determined. If a BLANK* transition from logical zero to logical one does not occur within 2048 pixel clocks, vertical blanking has been asserted.

The cursor pattern can be displayed in an interlaced system if bit CR4 in the cursor register is a logical one. When bit CR4 in the cursor register has been set to logical one, the SETUP pin will become the FLD* pin. The SETUP can then be controlled only through bit B5 in Command Register B (see the Pin Description and Cursor Register sections). If Yp is greater than 32 ($0020) and less than or equal to 4095 ($0FFF), the first cursor line displayed depends on the state of the FLD* pin and the value of Yp. If Yp is an even number, the data in row 0 of the cursor RAM array will be displayed during the even field, and the data in row 31 of the cursor RAM will be displayed during the odd field, starting at the position specified by (Xp,Yp). Each subsequent scan line displayed in the even field will correspond to every alternate active cursor line after row 0 in the cursor RAM array. During the odd fields, row 1 of the cursor RAM array is displayed on the first odd scan line at the position specified by (Xp, Yp). Each subsequent scan line displayed in the odd field will correspond to every alternate active cursor line after row 1 in the cursor RAM array.

If Yp is an odd number, the data in row 0 of the cursor RAM array will be displayed during the odd field, and the data in row 31 of the cursor RAM will be displayed during the even field, starting at the position specified by (Xp,Yp). Each subsequent scan line displayed in the odd field will correspond to

Circuit Description *(continued)*

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every alternate active cursor line after row 0 in the cursor RAM array. During even fields, row 1 of the cursor RAM array is displayed on the first even scan line, at the position specified by (Xp, Yp). Each subsequent scan line displayed in the even field will correspond to every alternate active cursor line after row 1 in the cursor RAM array.

If Yp is less than 32 ($0020), cursor display does not depend on whether Yp is odd or even. If the FLD* pin is a logical zero, the first line of the cursor is displayed on scan line one. Every alternate active cursor line in the cursor RAM array relative to the first active cursor line in the even field, will correspond to subsequent scan lines in the even field. If the FLD* pin is a logical one, the second active cursor line in the cursor RAM array is displayed on scan line two. Each subsequent scan line displayed in the odd field corresponds to alternate cursor lines in the cursor RAM array relative to the first active cursor line in the odd field.

If bit CR4 is a logical zero, the cursor must be displayed in a noninterlaced system. Scan lines displayed in a frame correspond to sequential cursor lines in the cursor RAM relative to the first active cursor line in the frame.

Figure 2 is a visual explanation of planar pixel format and cursor RAM array pixel mapping.

External Cursor Support

The Bt481 does not have an onboard cursor RAM but can support an external cursor. The external cursor data can be input via the two MSB overlay pins (OL3 and OL2). When external cursor data is accepted, only the first four locations of the overlay palette can be addressed, since the MSB bits become cursor inputs. When a Bt481 is used, bits CR5, CR4, and CR3 in the cursor register are set to logical 1, 0, and 0, respectively. All cursor X,Y registers are no longer valid. The Bt481, like the Bt482, has a 4 x 24 cursor color register to support three cursor modes (see Cursor Color Support and Table 4). When a Bt482 is used, only one type of cursor can be used, either internal or external, at any given time. Bit CR5 in the cursor register controls cursor type.

Cursor Color Support

The cursor has three modes for color selection. Bits CR0 and CR1 in the cursor register determine which cursor mode is to be used. Mode 1 is a three-color cursor, Mode 2 is referred to as a PM/Window cursor, and Mode 3 is referred to as an X-Windows cursor (see Table 4).

Highlight Logic

The highlight logic is enabled in Cursor Mode 2 when cursor index data (plane 1 and plane 0) is logical one (see Table 5). When the highlight logic is enabled, the pixel highlighted will have a unique color because the highlight logic bit-wise complements the 24/18-bit palette or bypass data supplied to the DACs.

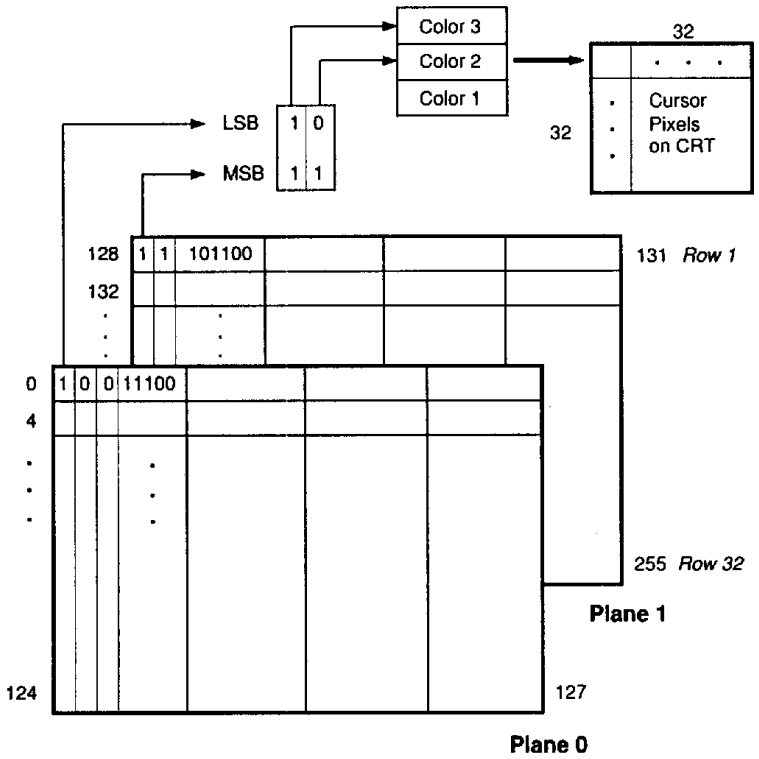

Figure 2. Planar Cursor Pixel Format and Mapping.

Circuit Description *(continued)*

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Cursor Interlaced/Noninterlaced Display Operation

For the cursor display, the output sequence is dependent on the CR4 command bit and the FLD* input, e.g., when either interlaced or noninterlaced operation is selected, the current field is displayed.

Scan line 1 is always displayed first in the interlaced mode and is considered the first line of the EVEN field. In the noninterlaced mode, scan line 2 immediately follows scan line 1. In the interlaced mode, scan line 2 is considered to be the first line of the ODD field and is displayed only after the entire EVEN field has been displayed and the FLD* pin has been toggled.

Only the ODD lines or only the EVEN lines will be displayed, if the FLD* does not change.

Figure 3 shows the interlaced and noninterlaced display scan. Noninterlaced display scan is equal to one frame. Interlaced display scan is equal to one frame with odd and even fields.

Plane 1	Plane 0	MODE 1	MODE 2	MODE 3
0	0	Palette/OL Data	Cursor Color 1	Palette/OL Data
0	1	Cursor Color 1	Cursor Color 2	Palette/OL Data
1	0	Cursor Color 2	Palette/OL Data	Cursor Color 1
1	1	Cursor Color 3	Palette/OL Data Complement	Cursor Color 2

Table 4. Cursor Color Modes. (Planes 1 and 0 refer to the Internal Cursor RAM.)

Cursor Mode	CR5	OL3–OL0	P0–P7	Addressed by Pixel Port
	1	0000	$xx	palette data/bypass
	1	0001	$xx	overlay color 1
	1	0010	$xx	overlay color 2
	1	0011	$xx	overlay color 3
Mode 1	1	00xx	$xx	palette/OL data
Mode 1	1	01xx	$xx	cursor color register 1
Mode 1	1	10xx	$xx	cursor color register 2
Mode 1	1	11xx	$xx	cursor color register 3
Mode 2	1	00xx	$xx	cursor color register 1
Mode 2	1	01xx	$xx	cursor color register 2
Mode 2	1	10xx	$xx	palette/OL data
Mode 2	1	11xx	$xx	palette/OL data complement
Mode 3	1	00xx	$xx	palette/OL data
Mode 3	1	01xx	$xx	palette/OL data
Mode 3	1	10xx	$xx	cursor color register 1
Mode 3	1	11xx	$xx	cursor color register 2

The cursor data has priority over the overlay data. OL3 and OL2 are used for external cursor support.

Table 5. External Cursor Color and Overlay Control Truth Table (Pixel/OL Read Mask Register = $FF).

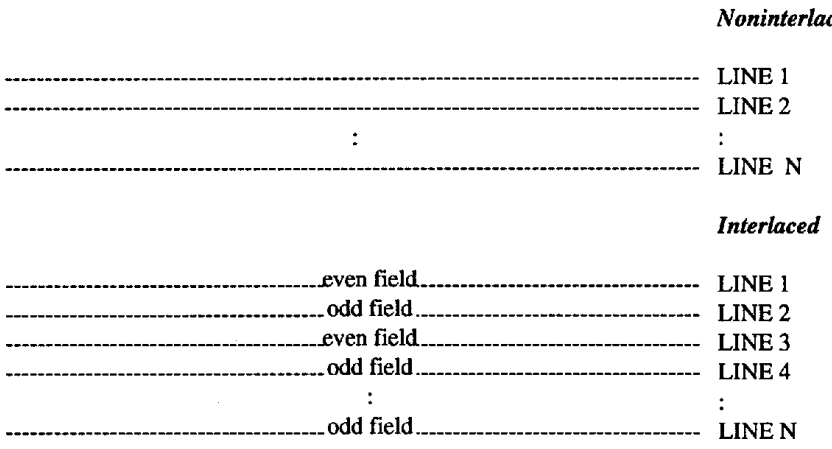

Figure 3. Interlaced / Noninterlaced Display Operation.

6-Bit/8-Bit Color Selection

The command register bit B1 or the 6*/8 pin can be used to specify whether the MPU is reading and writing 6 bits or 8 bits of color information each cycle. The 6*/8 bit (bit B1 in Command Register B) and the 6*/8 pin (pin #2) are logically ANDed. If the 6*/8 bit is a logical one, the 6*/8 pin controls 6- or 8-bit operation. While the 6*/8 bit remains at logical zero, the MPU will read and write 6 bits of color information each cycle. For 8-bit operation, D0 is the LSB and D7 is the MSB of color data.

For 6-bit operation, color data is contained on the lower 6 bits of the data bus; D0 is the LSB, and D5 is the MSB of color data. When color data is written, D6 and D7 are ignored. During color read cycles, D6 and D7 will be a logical zero.

Accessing the cursor RAM array does not depend on the resolution of the DACs. If the 6*/8 pin is held low (6-bit operation), the Bt481/482 will emulate a Bt471.

In the 6-bit mode, the Bt481/482's full-scale output current will be about 1.5 percent lower than when in the 8-bit mode. This is because the 2 LSBs of each 8-bit DAC are always a logical zero when in the 6-bit mode.

Power-Down Mode

The Bt481 and Bt482 incorporate a power-down capability, controlled by the SLEEP command bit. While the SLEEP bit is a logical zero, the Bt481/482 functions normally.

While the SLEEP bit is a logical one, the DACs and power to the RAM are turned off. The RAM still retains the data. Also, the RAM may still be read or written to while the SLEEP bit is a logical one if the pixel clock is running. The RAM automatically powers up during MPU read/write cycles and shuts down when the MPU access is complete. The DACs will be turned off during sleep mode only if a voltage reference (internal or external) is used. If an external current reference is used, external circuitry should turn off the current reference (IREF = 0 mA) during sleep mode.

When an external voltage reference is used, external circuitry should turn off the voltage reference (VREF = 0 V) to further reduce power consumption caused by biasing of portions of the internal voltage reference.

SENSE* Output

SENSE* is a logical zero if one or more of the IOR, IOG, and IOB outputs have exceeded the internal voltage reference level of the SENSE comparator circuit. This output is used to determine the presence of a CRT monitor and, with diagnostic code, the difference between a loaded or unloaded RGB line can be discerned. The reference is generated by a voltage divider from the external 1.235 V voltage reference on the VREF pin. For proper operation of the SENSE circuit, the following levels should be applied to the comparator with the IOR, IOG, and IOB outputs:

DAC Low Voltage ≤ 310 mV (see Note)
DAC High Voltage ≥ 430 mV (see Note)

There is an additional ±10 percent tolerance on the above levels when the internal voltage reference or an external current reference is used. SYNC* should be a logical zero for SENSE* to be stable.

Note: SENSE values are subject to change upon completion of characterization.

Circuit Description *(continued)*

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Controller Interface

The P0–P7 and OL0–OL3 inputs are used to address the color palette RAM and overlay registers, as shown in Table 6. The contents of the pixel read mask register, which may be accessed by the MPU at any time, are bit-wise logically ANDed with the P0–P7 inputs. Bit D0 of the pixel read mask register corresponds to pixel input P0. The contents of the overlay read mask register are bit-wise logically ANDed with the OL0–OL3 inputs. Bit D0 of the overlay read mask register corresponds to overlay input OL0, and bit D3 of the overlay read mask register corresponds to overlay input OL3. Bits D4–D7 of the overlay read mask register are ignored. Two consecutive write operations must be performed to write to the overlay read mask register. The first write is to the overlay read mask, and the second is to the pixel read mask. All 12 bits will be updated concurrently, synchronous to the pixel clock. Command Register B in the Internal Register section contains information regarding the accessability of the overlay read mask register. The addressed locations provide 18 bits or 24 bits of color information to the three D/A converters.

The SYNC* and BLANK* inputs, also latched on the rising edge of CLOCK to maintain synchronization with the color data, add appropriately weighted currents to the analog outputs. This produces the specific output levels required for video applications, as illustrated in Figures 4–6. Tables 7–9 detail how the SYNC* and BLANK* inputs modify the output levels.

The SETUP input pin is logically ORed with the SETUP command bit and is used to specify whether a 0 or 7.5 IRE blanking pedestal is to be used. If bit CR4 in the cursor register is set to logical one, the SETUP pin will become the field input (see Cursor Register in the Internal Register section) in order to support an interlaced cursor. The blanking pedestal can then be controlled only with the SETUP command bit (see Command Register B in the Internal Register section).

The analog outputs of the Bt482 can directly drive a 37.5 Ω load, such as a doubly-terminated 75 Ω coaxial cable.

CR5	OL0–OL3	P0–P7	Addressed by Pixel Port
0	$0	$00	color palette RAM location $00
0	$0	$01	color palette RAM location $01
:	:	:	:
0	$0	$FF	color palette RAM location $FF
0	$1	$xx	overlay color 1
:	:	$xx	:
0	$F	$xx	overlay color 15

Table 6. Pixel and Overlay Control Truth Table (Pixel Read Mask Register = $FF).

Circuit Description *(continued)*

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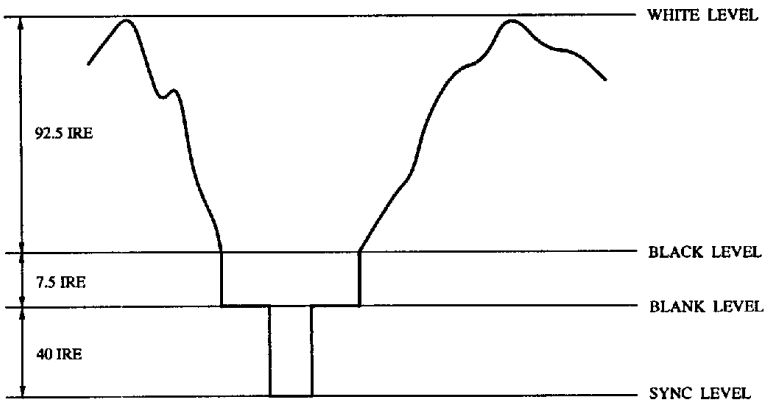
NO SYNC		SYNC	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000



Note: 75 Ω doubly-terminated load; SETUP = 7.5 IRE. VREF = 1.235 V and RSET = 143 Ω. RS-343A levels and tolerances are assumed on all levels.

Figure 4. RS-343A Composite Video Output Waveforms (SETUP = 7.5 IRE).

Description	Sync Disabled Iout (mA)	Sync Enabled Iout (mA)	SYNC*	BLANK*	DAC Input Data
WHITE	19.05	26.67	1	1	$FF
DATA	data + 1.44	data + 9.05	1	1	data
DATA - SYNC	data + 1.44	data + 1.44	0	1	data
BLACK	1.44	9.05	1	1	$00
BLACK - SYNC	1.44	1.44	0	1	$00
BLANK	0	7.62	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 75 Ω doubly-terminated load; SETUP = 7.5 IRE. VREF = 1.235 V and RSET = 143 Ω.

Table 7. RS-343A Video Output Truth Table (SETUP = 7.5 IRE).

Circuit Description *(continued)*

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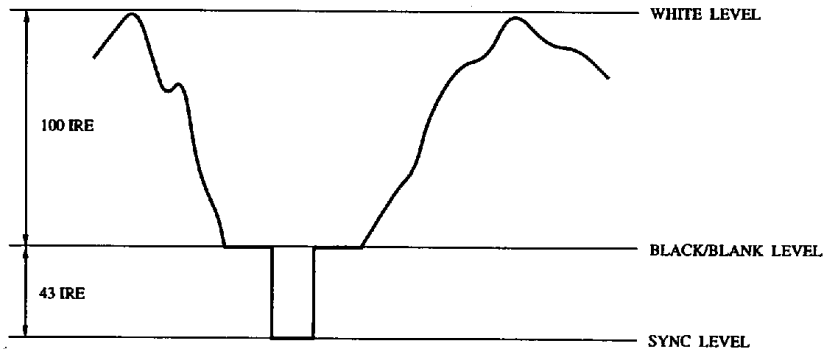
NO SYNC		SYNC	
MA	V	MA	V
17.62	0.660	25.24	0.950
0.00	0.000	7.62	0.286
0.00	0.000	0.00	0.000



Note: 75 Ω doubly-terminated load; SETUP = 0 IRE. VREF = 1.235V and RSET = 143 Ω. RS-343A levels and tolerances are assumed on all levels.

Figure 5. RS-343A Composite Video Output Waveforms (SETUP = 0 IRE).

Description	Sync Disabled	Sync Enabled	SYNC*	BLANK*	DAC Input Data
	Iout (mA)	Iout (mA)			
WHITE	17.62	25.24	1	1	$FF
DATA	data	data + 7.62	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	0	7.62	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	0	7.62	1	0	$xx
SYNC	0	0	0	0	$xx

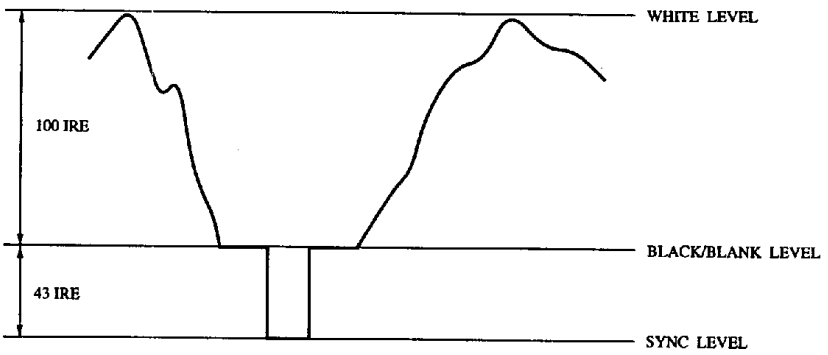
Note: 75 Ω doubly-terminated load; SETUP = 0 IRE. VREF = 1.235 V and RSET = 143 Ω.

Table 8. RS-343A Video Output Truth Table (SETUP = 0 IRE).

Circuit Description *(continued)*

T-52-33-43

NO SYNC		SYNC	
MA	V	MA	V
14.25	0.713	20.36	1.018
0.00	0.000	6.11	0.305
0.00	0.000	0.00	0.000



Note: 50 Ω load; SETUP = 0 IRE. VREF = 1.235 V and RSET = 176 Ω. PS/2 levels and tolerances are assumed on all levels.

Figure 6. PS/2 Composite Video Output Waveforms (SETUP = 0 IRE).

Description	Sync Disabled	Sync Enabled	SYNC*	BLANK*	DAC Input Data
	Iout (mA)	Iout (mA)			
WHITE	14.25	20.36	1	1	$FF
DATA	data	data + 6.11	1	1	data
DATA - SYNC	data	data	0	1	data
BLACK	0	6.11	1	1	$00
BLACK - SYNC	0	0	0	1	$00
BLANK	0	6.11	1	0	$xx
SYNC	0	0	0	0	$xx

Note: 50 Ω load; SETUP = 0 IRE. VREF = 1.235 V and RSET = 176 Ω.

Table 9. PS/2 Video Output Truth Table (SETUP = 0 IRE).

Internal Registers

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Command Register A

This register may be written to or read by the MPU at any time. All bits are initialized to logical zero on power-up.

A7	A6	A5	A4	
0	x	x	x	Pseudo Color (256 Colors)
1	0	0	0	5:5:5 Dual-Edge Clock (33K Colors)
1	1	0	0	5:6:5 Dual-Edge Clock (65K Colors)
1	0	1	0	5:5:5 Single-Edge Clock (33K Colors)
1	1	1	0	5:6:5 Single-Edge Clock (65K Colors)
1	0	0	1	8:8:8:OL Dual-Edge Clock (16.8M Colors)
1	1	1	1	8:8:8 Single-Edge Clock Only (16.8M Colors)

A logical one on Bit A7 enables 15-, 16-, and 24/32-bit modes when used with Bits A6, A5, and A4. If A7 is a logical zero, pseudo-color mode is enabled regardless of the state of A6, A5, or A4.

Bit A6 determines whether the device is in 15- or 16-bit-per-pixel mode.

Bit A5 determines whether the data is input on the rising edge of the input clock, or on the rising and falling edges of the input clock. A logical zero written to this bit indicates a dual-edge clock, and a logical one indicates a single-edge clock.

Bit A4 indicates a 24- or 32-bit input, i.e., a 24-bit true-color bypass, only, or a 24-bit true-color bypass and an 8-bit VGA passthrough. Bit A5 determines whether the pixels are input 8 bits at a time on every rising edge, or 8 bits at a time on rising and falling edges of the input clock. When bits A4 and A6 are set to logical one, the inputs are 24-bit true-color bypass, operating in single-edge clock mode.

A3, A2, A1 Reserved (logical zero)

A logical zero must be written to these bits to ensure proper operation.

A0 Extended Register Select

(0) Extended register set cannot be accessed.
(1) Extended register set can be accessed.

A logical one written to this bit allows the user to indirectly access the extended register set. Included in the extended register set are the cursor register and the cursor X,Y registers.

Internal Registers *(continued)*

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Command Register B

This register is operational only while bit A0 in Command Register A is a logical one. This register is initialized on power-up. On power-up, bits B7, B6, B5, and B0 are set to logical zero; bits B4, B3, B2, and B1 are set to logical one to enable the Bt481/482 to emulate the Bt478. While the 6*/8 pin is held low, this register will be functionally ignored.

B7	Reserved (logical zero)	A logical zero must be written to this bit to ensure proper operation.
B6	Overlay Register Mask Select (0) Overlay register mask inhibited (1) Overlay register mask enabled	A logical *zero* written to this bit *inhibits* address of the overlay registers only during true-color operations. A logical *one* written to this bit *enables* address of the overlay registers only during true-color operations.
B5	SETUP select (0) 0 IRE (1) 7.5 IRE	This bit specifies the blanking pedestal to be either 0 or 7.5 IRE. When the interlaced mode is set (bit CR4 = 1), only this bit will be able to control the SETUP select; the SETUP pin will become the field input (ODD/EVEN). While the 6*/8 pin is held low, the SETUP pin will act as the pedestal control rather than the field input.
B4	Blue sync enable (0) no sync on blue (1) sync on blue	This bit specifies whether the IOB output contains sync information.
B3	Green sync enable (0) no sync on green (1) sync on green	This bit specifies whether the IOG output contains sync information.
B2	Red sync enable (0) no sync on red (1) sync on red	This bit specifies whether the IOR output contains sync information.
B1	6-bit/8-bit select (0) 6-bit (1) 8-bit	On the Bt481 and Bt482, this bit specifies whether the MPU is reading and writing 8 bits (logical one) or 6 bits (logical zero) of color information each cycle. The 6*/8 bit and 6*/8 pin are logically ANDed.
B0	SLEEP enable (0) normal operation (1) sleep mode	While this bit is a logical zero, the Bt482 functions normally. If this bit is a logical one, the DACs and power to the RAM are turned off. The RAM still retains the data and may be read or written to while the pixel clock is running. The RAM automatically powers-up during MPU read/write cycles and shuts down when the MPU access is completed. About 1 second is required for the Bt482 to output valid video data after enabling normal operation (coming out of sleep mode). This time will vary depending on the size of the COMP capacitor. The DACs will be turned off during sleep mode only if a voltage reference (internal or external) is used. If an external current reference is used, external circuitry should turn the current reference off during sleep mode.

Internal Registers *(continued)*

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Cursor Register

This register is operational only when Bit A0 in Command Register A is a logical one. All bits are initialized to logical zero on power-up.

CR7, CR6	Reserved (logical zero)	A logical zero must be written to these bits to ensure proper operation.
CR5	Cursor Select (0) Internal Cursor Selected (1) External Cursor Mode/Overlay	This bit determines whether the internal cursor is used or external cursor data is input with the two MSB overlay pins of the Bt482 (OL3 and OL2). When the internal cursor is enabled, all 15 locations of the overlay palette can be selected. When an external cursor is enabled, only the first four locations of the overlay palette can be selected.
CR4	Display Mode Select (0) Noninterlaced (1) Interlaced	When this bit is a logical zero, the display format is noninterlaced. When it is a logical one, the display format is interlaced, and the odd/even fields are input with the SETUP pin. The mode must be set properly to ensure proper operation of the internal cursor.
CR3	Cursor RAM or Cursor Palette Select (0) Cursor Color Palette Selected (1) Cursor RAM Selected	A logical one written to this bit enables the user to access the 32 x 32 x 2 cursor RAM. A logical zero written to this bit enables the user to access the three cursor color palette locations.
CR2	Reserved (logical zero)	A logical zero must be written to this bit to ensure proper operation.
CR0, CR1	Cursor Mode Select (00) Cursor Disabled (01) 3-Color Cursor (10) 2-Color/Complement Cursor (11) 2-Color/X-Windows Cursor	These bits determine the functionality of the onboard 32 x 32 x 2 cursor.

Internal Registers *(continued)*

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Cursor (x,y) Registers

These registers specify the (x,y) coordinate of the 32 x 32 x 2 hardware cursor. The cursor (x) register is made up of the cursor (x) low register (CXLR) and the cursor (x) high register (CXHR); the cursor (y) register is made up of the cursor (y) low register (CYLR) and the cursor (y) high register (CYHR). The last value written by the MPU to these registers is the value returned on a read. These registers may be written to or read by the MPU at any time.

CXLR and CXHR are cascaded to form a 12-bit cursor (x) register. Similarly, CYLR and CYHR are cascaded to form a 12-bit cursor (y) register. Bits D4–D7 of CXHR and CYHR are always logical zeros.

	Cursor (x) High (CXHR)				Cursor (x) Low (CXLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
X Address	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0

	Cursor (y) High (CYHR)				Cursor (y) Low (CYLR)							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Y Address	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

The cursor (x) value to be written is calculated as follows:

Xp = desired display screen (x) position + 32 (or $0020)

where

the (x) reference point for the display screen, x = 0, is the upper left corner of the screen. The Xp position equation places the upper left corner of the cursor RAM array to the desired screen location. This allows the cursor position to be defined in the same coordinate space as the screen.

Values from 0 (or $0000) to 4095 ($0FFF) may be written into the cursor (x) register. If Xp is equal to zero, the cursor will be entirely offscreen (see Cursor Operation in the Circuit Description section).

The cursor (y) value to be written is calculated as follows:

Yp = desired display screen (y) position + 32 (or $0020)

where

the (y) reference point for the display screen, y = 0, is the upper left corner of the screen. The Yp position equation places the upper left corner of the cursor RAM array to the desired screen location. This allows the cursor position to be defined in the same coordinate space as the screen.

Values from 0 (or $0000) to 4095 (or $0FFF) may be written into the cursor (y) register. If Yp is equal to zero, the cursor will be entirely offscreen (see Cursor Operation in the Circuit Description section).

Pin Descriptions

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Pin Name & Number		Description
BLANK*	(7)	Composite blank control input (TTL compatible). A logic zero drives the analog outputs to the blanking level, as specified in Tables 7–9. BLANK* is latched on the rising edge of CLOCK. When BLANK* is a logical zero, the pixel and overlay inputs are ignored.
SETUP or FLD*	(23)	SETUP is setup control input (TTL compatible). This input is used to specify either a 0 IRE (logical zero) or 7.5 IRE (logical one) blanking pedestal. FLD* is odd/even field input (TTL Compatible). This signal should be changed only during vertical blanking. This input ensures proper operation of the onboard cursor when interlaced operation (command register bit CR4 = 1) is selected. When it is a logical zero, an even field is specified. When this input is a logical one, an odd field is specified. If CR4 = 1, SETUP can be controlled only through Bit B5 in Command Register B. This input becomes the SETUP control if noninterlaced operation is selected (CR4 = 0). This pin should not be left floating.
SYNC*	(5)	Composite sync control input (TTL compatible). A logical zero on this input switches off a 40 IRE current source on the analog outputs (see Figures 4–6). SYNC* does not override any other control or data input, as shown in Tables 7–9; therefore, it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK. If sync information is not required on the video outputs, SYNC* should be connected to GND.
CLOCK	(40)	Clock input (TTL compatible). The rising edge of CLOCK latches the P0–P7, OL0–OL3, SYNC*, and BLANK* inputs. It is typically the pixel clock rate of the video system. It is recommended that CLOCK be driven by a dedicated TTL buffer to avoid reflection-induced jitter.
P0–P7	(32–39)	Pixel select inputs (TTL compatible). These inputs specify, on a pixel basis, which one of the 256 entries in the color palette RAM is to be used to provide color information. They are latched on the rising edge of CLOCK. P0 is the LSB. Unused inputs should be connected to GND.
OL0–OL3	(41–44)	Overlay select inputs (TTL compatible). These inputs specify which palette is to be used to provide color information, as specified in Table 6. When the overlay palette is accessed, the P0–P7 inputs are ignored. They are latched on the rising edge of CLOCK. OL0 is the LSB. Unused inputs should be connected to GND. OL2 and OL3 are used for external cursor inputs when external cursor is selected.
COMP	(29)	Compensation pin. If an external or the internal voltage reference is used, this pin should be connected to OPA. If an external current reference is used, this pin should be connected to IREF. A 0.1 µF ceramic capacitor must always be used to bypass this pin to VAA. The COMP capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. The PC Board Layout Considerations section contains critical layout criteria.
VREF	(31)	Voltage reference input. If an external voltage reference is used, it must supply this input with a 1.235 V (typical) reference. If an external current reference is used, this pin should be left floating, except for the bypass capacitor. A 0.1 µF ceramic capacitor should decouple this input to GND. The decoupling capacitor must be as close to the device as possible to keep lead lengths to an absolute minimum. When using the internal reference, this pin should not drive any external circuitry other than the decoupling capacitor. The PC Board Layout Considerations section contains further information.
OPA	(30)	Reference amplifier output. If an external or the internal voltage reference is used, this pin must be connected to COMP. When an external current reference is used, this pin should be left floating. The PC Board Layout Considerations section contains further information.
IOR, IOG, IOB	(25–27)	Red, green, and blue current outputs. These high-impedance current sources can directly drive a doubly-terminated 75 Ω coaxial cable. The PC Board Layout Considerations section contains further information.
VAA	(4, 21, 22)	Analog power. All VAA pins must be connected together on the same PCB plane to prevent latchup.

Pin Descriptions *(continued)*

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Pin Name & Number	Description
GND (3, 24)	Analog ground. All GND pins must be connected together on the same PCB plane to prevent latchup.
IREF (28)	Full-scale adjust control. The IRE relationships in Figures 4–6 are maintained, regardless of the full-scale output current. When an external or the internal voltage reference is used, a resistor (RSET) connected between this pin and GND controls the magnitude of the full-scale video signal. The relationship between RSET and the full-scale output current on each output is: RSET (Ω) = K * 1,000 * VREF (V) / Iout (mA) K is defined in the table below. It is recommended that a 143 Ω RSET resistor be used for doubly-terminated 75 Ω loads (i.e., RS-343A applications). For PS/2 applications (i.e., 0.7 V into 50 Ω with no sync), a 176 Ω RSET resistor is recommended. When an external current reference is used, the relationship between IREF and the full-scale output current on each output is: IREF (mA) = Iout (mA) / K **Mode / Pedestal / K (with sync) / K (no sync)** 6-bit / 7.5 IRE / 3.078 / 2.211 8-bit / 7.5 IRE / 3.102 / 2.230 6-bit / 0 IRE / 2.910 / 2.044 8-bit / 0 IRE / 2.934 / 2.063 See the PC Board Layout Considerations section for further information.
WR* (16)	Write control input (TTL compatible). D0–D7 data is latched on the rising edge of WR*, and RS0–RS2 are latched on the falling edge of WR* during MPU write operations. RD* and WR* should not be asserted simultaneously.
RD* (6)	Read control input (TTL compatible). To read data from the device, RD* must be a logical zero. RS0–RS2 are latched on the falling edge of RD* during MPU read operations. RD* and WR* should not be asserted simultaneously.
RS0, RS1, RS2 (17–19)	Register select inputs (TTL compatible). RS0–RS2 specify the type of read or write operation being performed, as detailed in Tables 1 and 2.
D0–D7 (8–15)	Data bus (TTL compatible). Data is transferred into and out of the device over this 8-bit bidirectional data bus. D0 is the least significant bit.
6*/8 (2)	6-bit/8-bit select input (TTL Compatible). This pin specifies whether the MPU is reading and writing 8 bits (logical one) or 6 bits (logical zero) of color information each cycle. For 8-bit operation, MPU Bit D7 is the most significant bit during read/write cycles. For 6-bit operation, MPU Bit D5 is the most significant bit during read/write cycles. (D7 and D6 are ignored during write cycles and are logical zero during read cycles.)
SENSE* (1)	Sense output (CMOS compatible). SENSE* is a logical zero if one or more of the IOR, IOG, and IOB outputs have exceeded the internal voltage reference level. SENSE* may not be stable while SYNC* is toggling.
TRUECOL* (20)	True-color mode select input (TTL compatible). This signal is inverted and logically ORed with Bit A7 in Command Register A. A logical zero will enable the true-color modes. By programming the proper command register bits, the user can choose either 5:5:5, 5:6:5, 8:8:8, or 8:8:8:OL and determine whether the pixels are input on a single clock edge or a dual clock edge (see the Command Register section for details). The TRUECOL* pin should be tied to VAA to disable the hardware selection of the true-color mode.

Pin Descriptions *(continued)*

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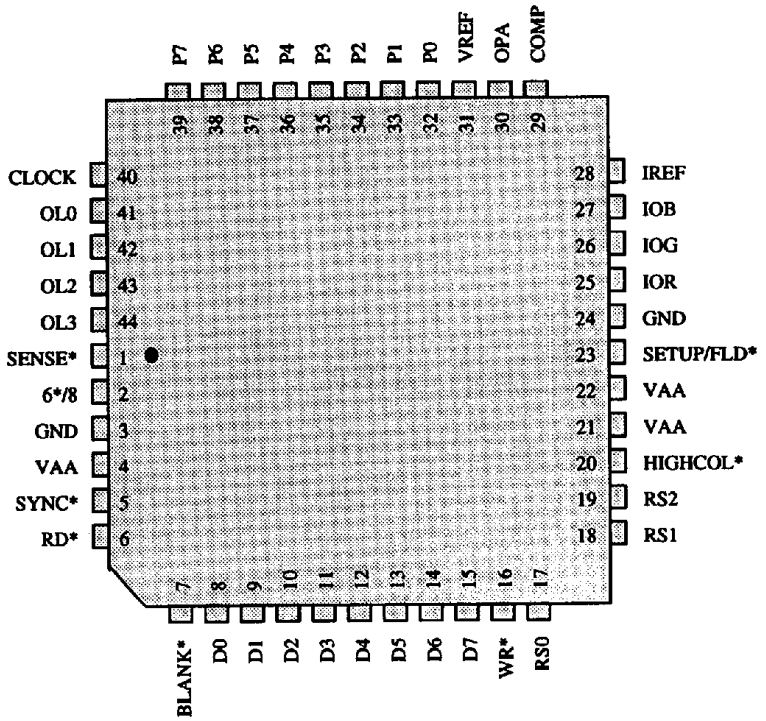

PC Board Layout Considerations

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PC Board Considerations

For optimum performance of the Bt481/482, proper CMOS RAMDAC layout techniques should be studied in the Bt451/7/8 Evaluation Module Operation and Measurements, Application Note (AN-16). This application note can be found in Brooktree's *Applications Handbook*.

The layout should be optimized for lowest noise on the Bt481/482 power and ground planes by providing good decoupling. The trace length between groups of VAA and GND pins should be as short as possible to minimize inductive ringing.

A well-designed power distribution network is critical to eliminating digital switching noise. The ground plane must provide a low-impedance return path for the digital circuits. A PC board with a minimum of four layers is recommended, with layers 1 (top) and 4 (bottom) for signals and layers 2 and 3 for power and ground.

Component Placement

Components should be placed as close as possible to the associated RAMDAC pin. Whenever possible, components should be placed so traces can be connected point to point.

The optimum layout enables the Bt481/482 to be located as close as possible to the power supply connector and the video output connector.

Ground Planes

For optimum performance, a common digital and analog ground plane is recommended.

Power Planes

Separate digital and analog power planes are recommended. The digital power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt481/482 power pins, VREF circuitry, and COMP and VREF decoupling. There should be at least a 1/8-inch gap between the digital power plane and the analog power plane.

The analog power plane should be connected to the digital power plane (VCC) at a single point through a ferrite bead, as illustrated in Figures 7–9. This bead should be located within 3 inches of the Bt481/482. The bead provides resistance to switching currents, acting as a resistance at high frequencies. A low-resistance bead should be used, such as Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001.

Device Decoupling

For optimum performance, all capacitors should be located as close as possible to the device, and the shortest possible leads (consistent with reliable operation) should be used to reduce the lead inductance. Chip capacitors are recommended for minimum lead inductance. Radial lead ceramic capacitors may be substituted for chip capacitors and are better than axial lead capacitors for self-resonance. Values are chosen to have self-resonance above the pixel clock.

Power Supply Decoupling

The best power supply decoupling performance is obtained with a 0.1 µF ceramic capacitor, decoupling each of the two groups of VAA pins to GND. For operation above 75 MHz, a 0.1 µF capacitor in parallel with a 0.01 µF chip capacitor is recommended. The capacitors should be placed as close as possible to the device VAA and GND pins and connected with short, wide traces.

The 10 µF capacitor shown in Figures 7–9 is for low-frequency power supply ripple; the 0.1 µF capacitors are for high-frequency power supply noise rejection.

When a linear regulator is used, the power-up sequence must be verified to prevent latchup. A linear regulator is recommended to filter the analog power supply if the power supply noise is greater than or equal to 200 mV. This is especially important when a switching power supply is used, and the switching frequency is close to the raster scan frequency. About 10 percent of the power supply hum and ripple noise less than 1 MHz will couple onto the analog outputs.

COMP Decoupling

The COMP pin must be decoupled to VAA, typically with a 0.1 µF ceramic capacitor. Low-frequency supply noise will require a larger value. The COMP capacitor must be as close as possible to the COMP and VAA pins. A surface-mount ceramic chip capacitor is preferred for minimal lead inductance. Lead inductance degrades the noise rejection of the circuit. Short, wide traces will also reduce lead inductance.

If the display has a ghosting problem, additional capacitance in parallel with the COMP capacitor may help.

VREF Decoupling

A 0.1 µF ceramic capacitor should be used to decouple this input to GND.

PC Board Layout Considerations *(continued)*

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Digital Signal Interconnect

The digital inputs to the Bt481/482 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane or analog output signals.

Most of the noise on the analog outputs will be caused by excessive edge rates (less than 3 ns), overshoot, undershoot, and ringing on the digital inputs.

The digital edge rates should not be faster than necessary, as feedthrough noise is proportional to the digital edge rates. Lower-speed applications will benefit from using lower-speed logic (3–5 ns edge rates) to reduce data-related noise on the analog outputs.

Transmission lines will mismatch if the lines do not match the source and destination impedance. This will degrade signal fidelity if the line length reflection time is greater than one fourth the signal edge time (refer to Brooktree Application Notes AN-11 and AN-12). Line termination or line-length reduction is the solution. For example, logic edge rates of 2 ns require line lengths of less than 4 inches without use of termination. Ringing may be reduced by damping the line with a series resistor (30–300 Ω). The RS-select inputs and RD*/WR* lines must be verified for proper levels with no ringing, undershoot, or overshoot. Ringing on these lines can cause improper operation.

Radiation of digital signals can also be picked up by the analog circuitry. This is prevented by reducing the digital edge rates (rise/fall time), minimizing ringing with damping resistors, and minimizing coupling through PC board capacitance by routing the digital signals at a 90 degree angle to any analog signals.

The clock driver and all other digital devices must be adequately decoupled to prevent noise generated by the digital devices from coupling into the analog circuitry.

Clock Interfacing

The Bt481/482 requires a pixel clock with monotonic clock edges for proper operation. Impedance mismatch on the pixel clock line will induce reflections on the pixel clock, which may cause erratic operation.

The Pixel Clock Pulse Width High Time and Pixel Clock Pulse Width Low Time minimum specifications (see the AC Characteristics section) must not be violated, or erratic operation can occur.

The pixel clock line must be terminated to prevent impedance mismatch. A series termination of 33–68 Ω placed at the pixel clock driver may be used, or a parallel termination may be used at the pixel clock input to the RAMDAC. A parallel termination of 220 Ω to VCC and 330 Ω to ground will provide a Thevinen equivalent of a 110 Ω termination, which is normally sufficient to absorb reflections. The series or parallel resistor values should be adjusted to provide the optimum clock signal fidelity.

MPU Control Signal Interfacing

The Bt481/482 uses the RD*, WR*, and RS lines to determine which MPU accesses will take place. Glitches or ringing on any of these lines may cause improper MPU operation. When a VGA controller with edge rate control is used on these lines, a series termination is not necessary. In non-VGA controller application or in applications where the MPU control signals are daisy chained, a series termination, pull-down resistors, or additional capacitance to ground should be used to prevent glitches that could cause improper MPU accesses.

Analog Signal Interconnect

The Bt481/482 should be located as close as possible to the output connectors to minimize noise pickup and reflections caused by impedance mismatch.

The analog outputs are susceptible to crosstalk from digital lines; digital traces must not be routed under or adjacent to the analog output traces.

To maximize the high-frequency power supply rejection, the video output signals should not overlay the analog power plane.

For maximum performance, the analog video output impedance, cable impedance, and load impedance should be the same. The load resistor connection between the video outputs and GND should be as close as possible to the Bt481/482 to minimize reflections. Unused analog outputs should be connected to GND.

Analog output video edges exceeding the CRT monitor bandwidth can be reflected, producing cable-length dependent ghosts. Simple pulse filters can reduce high-frequency energy, reducing EMI and noise. The filter impedance must match the line impedance.

Analog Output Protection

The Bt481/482 analog output should be protected against high-energy discharges, such as those from monitor arc-over or from hot-switching AC-coupled monitors.

The diode protection circuit shown in Figures 7–9 can prevent latchup under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 parts are low-capacitance, fast-switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

PC Board Layout Considerations *(continued)*

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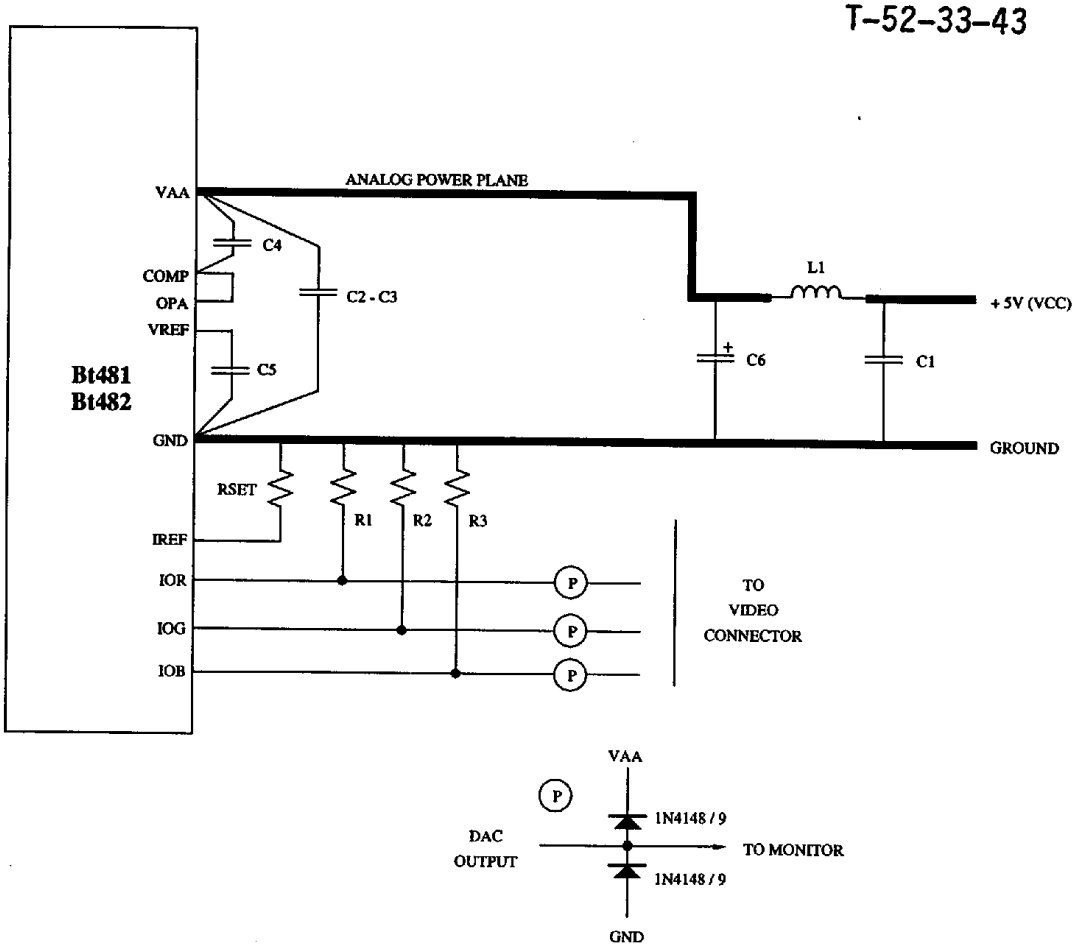

Note: Each pair of device VAA and GND pins must be separately decoupled.

Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
RSET	1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt481/482.

Figure 7. Typical Connection Diagram and Parts List (Internal Voltage Reference).

PC Board Layout Considerations *(continued)*

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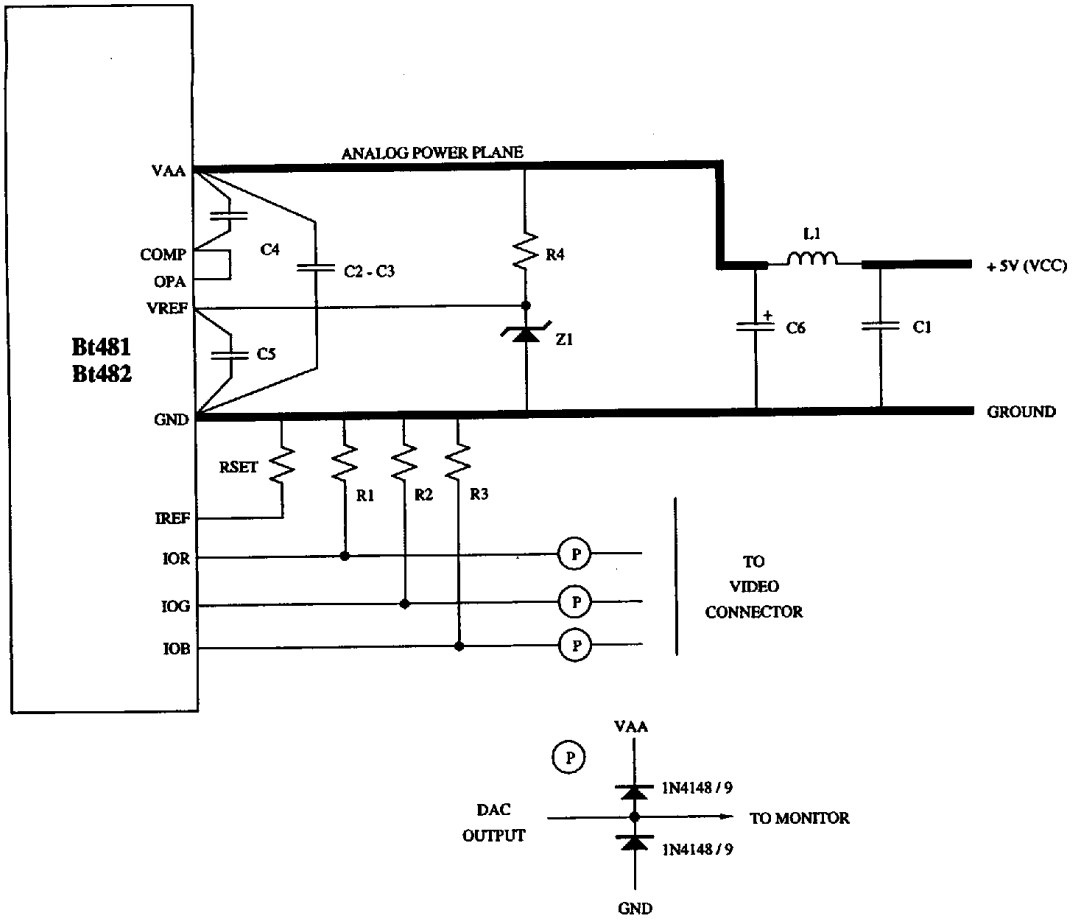


Note: Each pair of device VAA and GND pins must be separately decoupled.

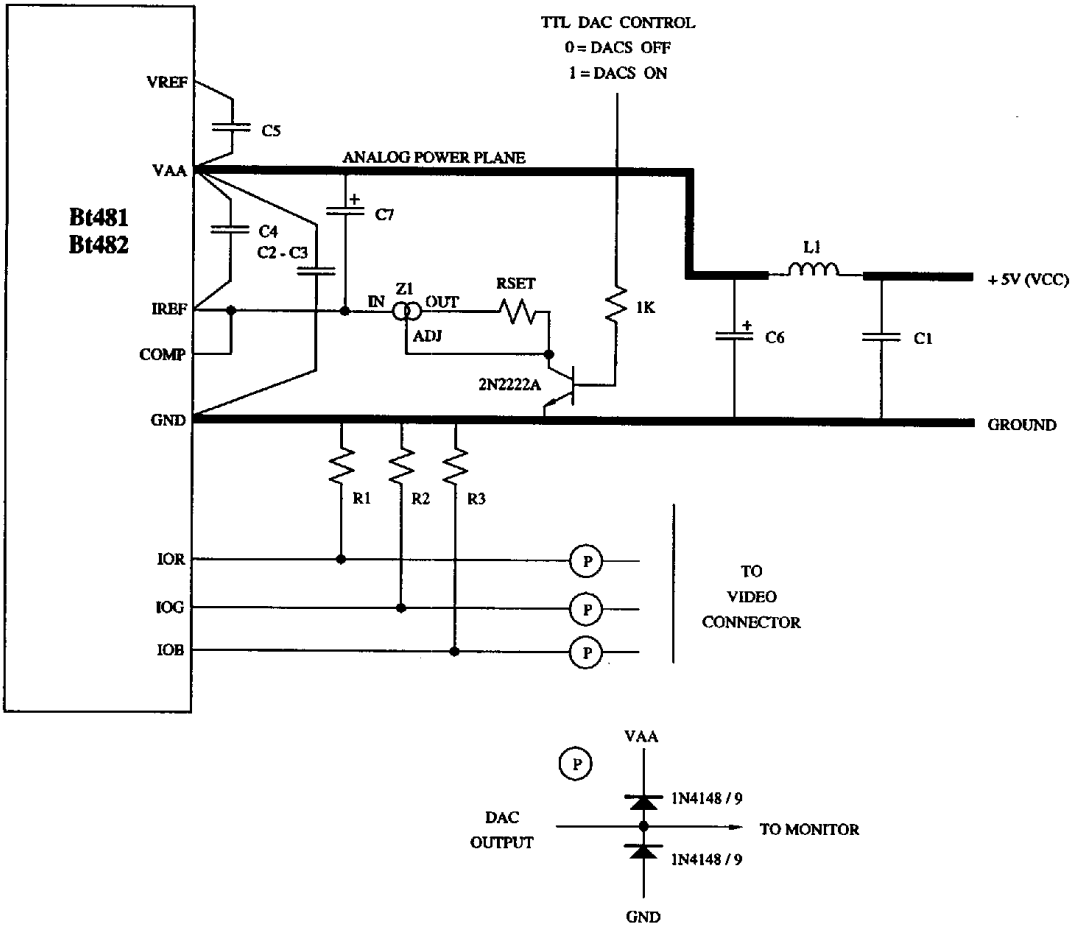
Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
R4	1 kΩ 5% resistor	
RSET	1% metal film resistor	Dale CMF-55C
Z1	1.2 V voltage reference	National Semiconductor LM385BZ-1.2

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt481/482.

Figure 8. Typical Connection Diagram and Parts List (External Voltage Reference).

PC Board Layout Considerations *(continued)*

T-52-33-43



Note: Each pair of device VAA and GND pins must be separately decoupled.

Location	Description	Vendor Part Number
C1–C5	0.1 µF ceramic capacitor	Erie RPE112Z5U104M50V
C6	10 µF capacitor	Mallory CSR13G106KM
C7, C8	1 µF capacitor	Mallory CSR13G105KM
L1	ferrite bead	Fair-Rite 2743001111
R1, R2, R3	75 Ω 1% metal film resistor	Dale CMF-55C
Z1	adjustable regulator	National Semiconductor LM317LZ
RSET	1% metal film resistor	Dale CMF-55C

Note: The vendor numbers above are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt481/482.

Figure 9. Typical Connection Diagram and Parts List (External Current Reference).

Application Information

T-52-33-43

Using Multiple Devices

When multiple Bt482s are used, each Bt482 should have its own power plane ferrite bead. If the internal reference is used, each Bt482 should use its own internal reference.

Although the multiple Bt482s may be driven by a common external voltage/current reference, higher performance may be obtained if each RAMDAC uses its own reference. This will reduce the amount of color channel crosstalk and color palette interaction.

Each Bt482 must still have its own RSET resistor, analog output termination resistors, power supply bypass capacitors, COMP capacitor, and reference capacitors.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat leaky inputs.

All logic inputs should be held low until power to the device has settled to the specified tolerance. DAC power decoupling networks with large time constants should be avoided. They could delay VAA power to the device. Ferrite beads must be used only for analog power VAA decoupling. Inductors cause a time constant delay that induces latchup.

Latchup can be prevented by ensuring that all VAA pins are at the same potential and that the VAA supply voltage is applied before the signal pin voltages. The correct power-up sequence ensures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.

Reference Selection

An external voltage reference provides about ten times the power supply rejection on the analog outputs than does an external current reference.

Sleep Operation

When the internal or external voltage reference is used, the DACs will be turned off during sleep mode.

When an external voltage reference is used, some internal circuitry will still be powered during the sleep mode, resulting in 0.5 mA of power supply current being drawn (above the rated supply current specifications). This unnecessary current drain can be disabled by turning off the external voltage reference during sleep mode.

When an external current reference is used, the DACs are not turned off during the sleep mode. To disable the DACs during sleep mode, the current reference must be turned off. As shown in Figure 9, a TTL signal and the 2N2222 transistor are used to disable the current reference during sleep mode.

Recommended Operating Conditions

T-52-33-43

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA				
85 and 75 MHz Parts		4.75	5.00	5.25	V
Ambient Operating Temperature	TA	0		+70	°C
Output Load	RL		37.5		Ω
Voltage Reference Configuration					
Reference Voltage	VREF	1.14	1.235	1.26	V
Current Reference Configuration					
IREF Current	IREF				
Standard RS-343A		–3	–8.39	–10	mA
PS/2 Compatible		–3	–8.88	–10	mA

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Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	V
Voltage on any Signal Pin (Note 1)		GND–0.5		VAA + 0.5	V
Analog Output Short Circuit Duration to any Power Supply or Common	ISC		indefinite		
Ambient Operating Temperature	TA	–55		+125	°C
Storage Temperature	TS	–65		+150	°C
Junction Temperature	TJ			+150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: This device employs high impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

T-52-33-43

Parameter	Symbol	Min	Typ	Max	Units
Resolution (each DAC)					
Bt482 and Bt481		6	6	6	Bits
Bt482 and Bt481		8	8	8	Bits
Accuracy (each DAC)					
Integral Linearity Error	IL				
Bt482 and Bt481				±1	LSB
Differential Linearity Error	DL				
Bt482 and Bt481				±1	LSB
Gray-Scale Error				±5	% Gray Scale
Monotonicity			guaranteed		
Coding					Binary
Digital Inputs					
Input High Voltage	VIH	2.0		VAA + 0.5	V
Input Low Voltage	VIL	GND–0.5		0.8	V
Input High Current (Vin = 2.4 V)	IIH			1	µA
Input Low Current (Vin = 0.4 V)	IIL			–1	µA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		5		pF
Digital Outputs					
Output High Voltage (IOH = –400 µA)	VOH	2.4			V
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	V
3-State Current	IOZ			50	µA
Output Capacitance	CDOUT		5		pF

See test conditions on next page.

DC Characteristics *(continued)*

T-52-33-43

Parameter	Symbol	Min	Typ	Max	Units
Analog Outputs					
Gray Scale Current Range				20	mA
Output Current					
White Level Relative to Black (Note 1)		16.74	17.62	18.50	mA
Black Level Relative to Blank					
Setup = 7.5 IRE		0.95	1.44	1.90	mA
Setup = 0 IRE		0	5	50	µA
Blank Level					
Sync Enabled		6.29	7.62	8.96	mA
Sync Disabled		0	5	50	µA
Sync Level		0	5	50	µA
LSB Size					
Bt482 and Bt481			69.1		µA
DAC-to-DAC Matching			2	5	%
Output Compliance	VOC	–0.5		+1.5	V
Output Impedance	RAOUT		10		kΩ
Output Capacitance (f = 1 MHz, IOUT = 0 mA)	CAOUT		18		pF
Internal Reference Output	VREF	TBD	TBD	TBD	V
Power Supply Rejection Ratio (Note 2) (COMP = 0.1 µF, f = 1 kHz)	PSRR			0.5	% / % ΔVAA

Test conditions to generate RS-343A standard video signals (unless otherwise specified): "Recommended Operating Conditions" and external voltage reference with RSET = 143 Ω, VREF = 1.235 V, SETUP = 7.5 IRE, and 6*/8 pin = logical one. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

When the internal voltage reference is used, RSET may require adjustment to meet these limits. Also, the gray-scale output current (white level relative to black) will have a typical tolerance of ±10 percent rather than the ±5 percent specified above.

Note 1: When the Bt482 or Bt481 is in the 6-bit mode, the output levels are approximately 1.5 percent lower than these values.

Note 2: Guaranteed by characterization, not tested.

Bt481/482

Brooktree®

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AC Characteristics

Parameter	Symbol	85 MHz Devices Min	85 MHz Devices Typ	85 MHz Devices Max	75 MHz Devices Min	75 MHz Devices Typ	75 MHz Devices Max	Units
Input Clk Rate Pseudo Color	Fmax			85			75	MHz
Input Clk Rate 15-, 16-bit dual-edge clk	Fmax			50			50	MHz
Input Clk Rate 15-, 16-bit single-edge clk	Fmax			85			85	MHz
Input Clk Rate 32-bit dual-edge clk	Fmax			50			50	MHz
Input Clk Rate 24-bit single-edge clk	Fmax			85			85	MHz
RS0–RS2 Setup Time	1	10			10			ns
RS0–RS2 Hold Time	2	10			10			ns
RD* Asserted to Data Bus Driven	3	2			2			ns
RD* Asserted to Data Valid	4			40			40	ns
RD* Negated to Data Bus 3-Stated	5			20			20	ns
Read Data Hold Time	6	2			2			ns
Write Data Setup Time	7	10			10			ns
Write Data Hold Time	8	10			10			ns
RD*, WR* Pulse Width Low	9	50			50			ns
RD*, WR* Pulse Width High	10	6*p13			6*p13			ns
Pixel and Control Setup Time	11	3			3			ns
Pixel and Control Hold Time	12	3			3			ns
(Pseudo Color and 15-, 16-, and 24-bit Single-Edge Clock Mode)								
Pixel and Control Setup Time	20	–1			–1			ns
Pixel and Control Hold Time	21	7			7			ns
(15-, 16-, and 32-bit Dual-Edge Clock Mode, LSB and MSB)								
Clock Cycle Time (p13)	13	11.77			13.33			ns
Pseudo Color Mode								
Clock Pulse Width High Time (Note 1)	14	4			4			ns
Clock Pulse Width Low Time (Note 1)	15	4			4			ns
Single Edge True Color Modes								
Clock Pulse Width High Time (Note 1)	14	5			5			ns
Clock Pulse Width Low Time (Note 1)	15	5.5			5.5			ns
Clock Cycle Time (Dual-Edge Clock)	13	20			20			ns
Clock Pulse Width High Time	14	9			9			ns
Clock Pulse Width Low Time	15	9			9			ns
Analog Output Delay	16			30			30	ns
Analog Output Rise/Fall Time	17		3			3		ns
Analog Output Settling Time (Note 2)	18		13			13		ns
Clock and Data Feedthrough (Note 2)			–30			–30		dB
Glitch Impulse (Note 2)			75			75		pV - sec
DAC-to-DAC Crosstalk			–23			–23		dB
Analog Output Skew				2			2	ns
SENSE* Output Delay	19		1			1		µS
VAA Supply Current (Note 3)	IAA			270			270	mA
normal operation								
sleep enabled (Note 4)			2			2		mA

AC Characteristics *(continued)*

T-52-33-43

Parameter	85 MHz Devices Min	85 MHz Devices Typ	85 MHz Devices Max	75 MHz Devices Min	75 MHz Devices Typ	75 MHz Devices Max	Units
Pipeline Delay							Clocks
Pseudo Color	7	7	7	7	7	7	
5:5:5 Dual-Edge Clock Mode	7	7	7	7	7	7	
5:6:5 Dual-Edge Clock Mode	7	7	7	7	7	7	
8:8:8:8 Dual-Edge Clock Mode	8	8	8	8	8	8	
5:5:5 Single-Edge Clock Mode	8	8	8	8	8	8	
5:6:5 Single-Edge Clock Mode	8	8	8	8	8	8	
8:8:8 Single-Edge Clock Mode	9	9	9	9	9	9	

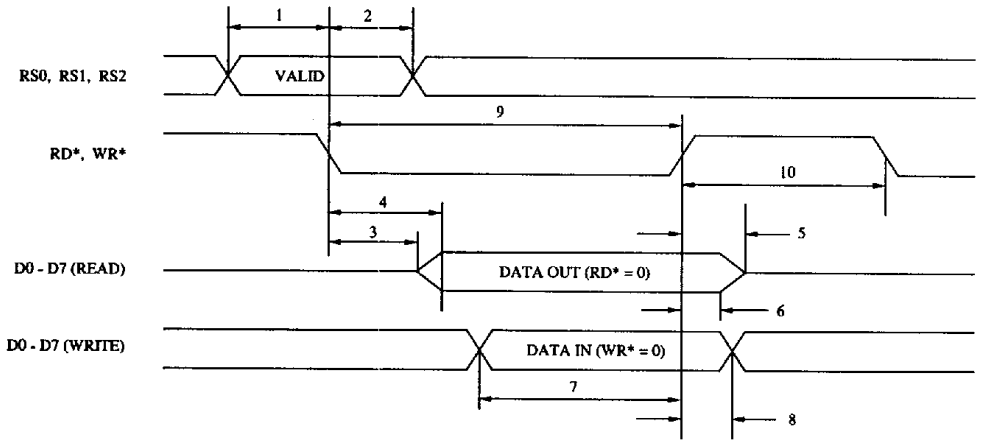
Test conditions (unless otherwise specified): "Recommended Operating Conditions" and external voltage reference with RSET = 143 Ω, VREF = 1.235 V, SETUP = 7.5 IRE, and 6*/8 pin = logical one. TTL input values are 0–3 V with input rise/fall times ≤ 3 ns, measured between the 10-percent and 90-percent points. Timing reference points are at 50 percent for inputs and outputs unless otherwise noted. Analog output load ≤ 10 pF. SENSE*, D0–D7 output load ≤ 75 pF. See the timing notes on the following page. As the above parameters are guaranteed over the full temperature range, temperature coefficients are not specified or required. Typical values are based on nominal temperature, i.e., room temperature, and nominal voltage, i.e., 5 V.

Note 1: These pulse widths are specified at VIL = 0.8 V for clock pulse width low and VIH = 2.0 V for clock pulse width high.

Note 2: Clock and data feedthrough is a function of the number of edge rates, and the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to ground and are driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough, and –3 dB test bandwidth = 2 x clock rate.

Note 3: At Fmax. IAA (typ) at VAA = 5.0 V. IAA (max) at VAA (max).

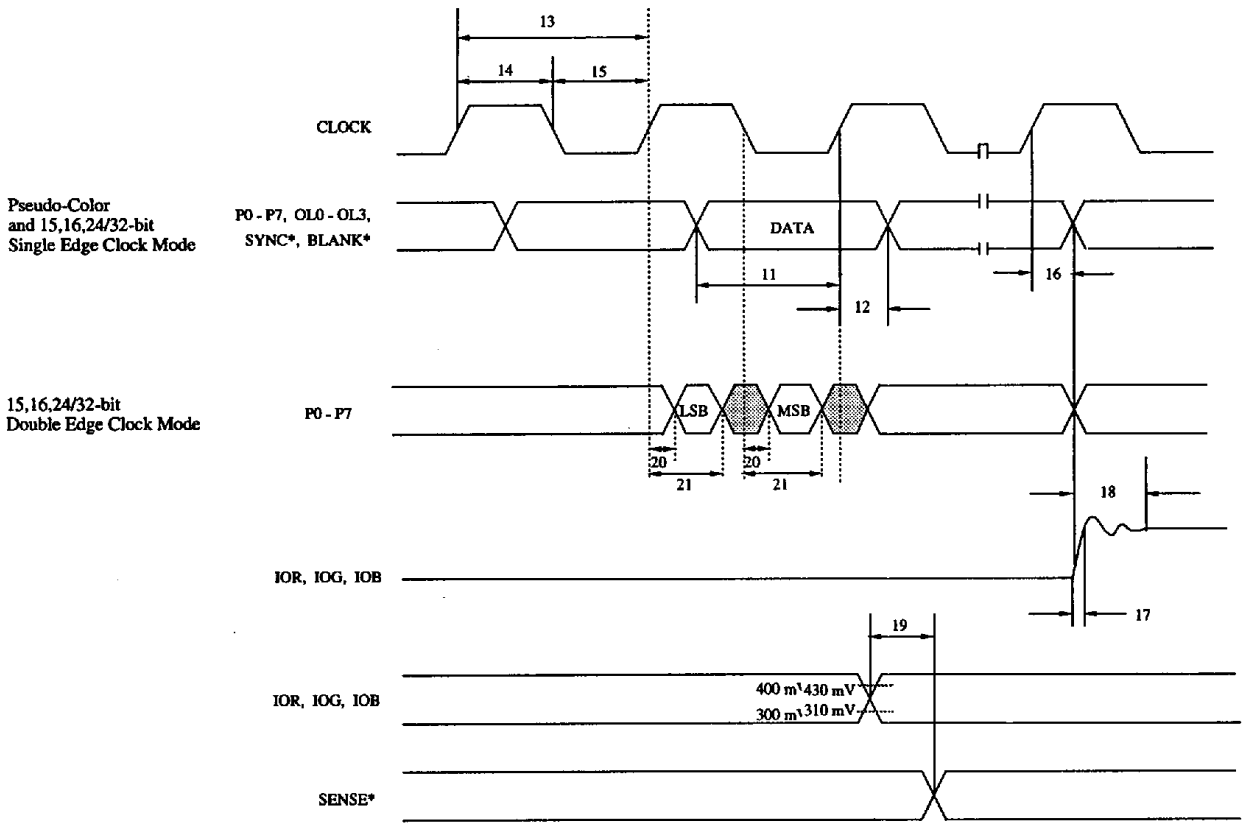
Note 4: External current or voltage reference disabled during sleep mode. Test Conditions: +25° to +70° C, pixel and data ports at 0.4 V.



MPU Read/Write Timing.

Timing Waveforms

T-52-33-43



Note 1: Output delay is measured from the 50-percent point of the rising edge of CLOCK to the 50-percent point of full-scale transition.

Note 2: Settling time is measured from the 50-percent point of full-scale transition to the output remaining within ±1 LSB.

Note 3: Output rise/fall time is measured between the 10-percent and 90-percent points of full-scale transition.

Video Input/Output Timing.

Timing Waveforms

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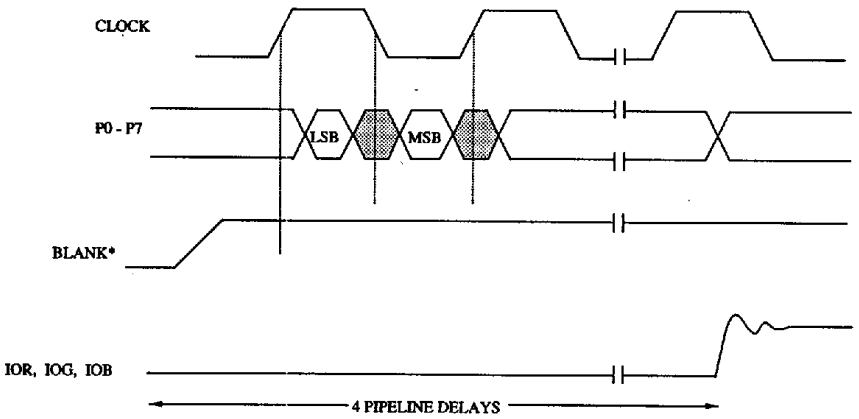
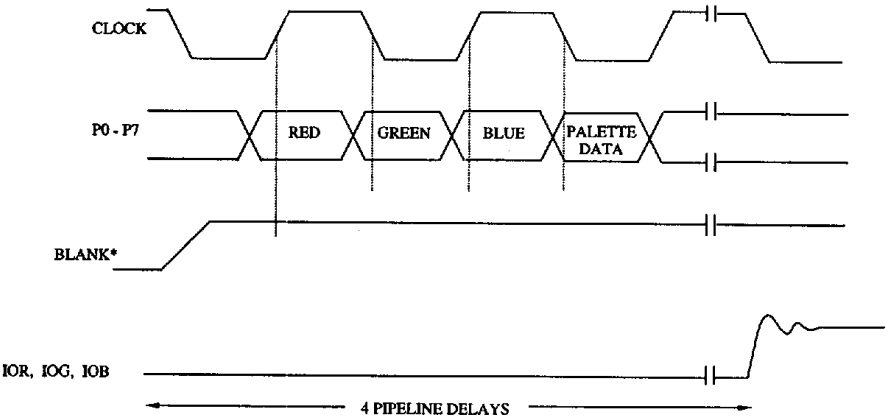
15,16-bit
Dual Edge Clock Mode



24/32-bit
Dual Edge Clock Mode

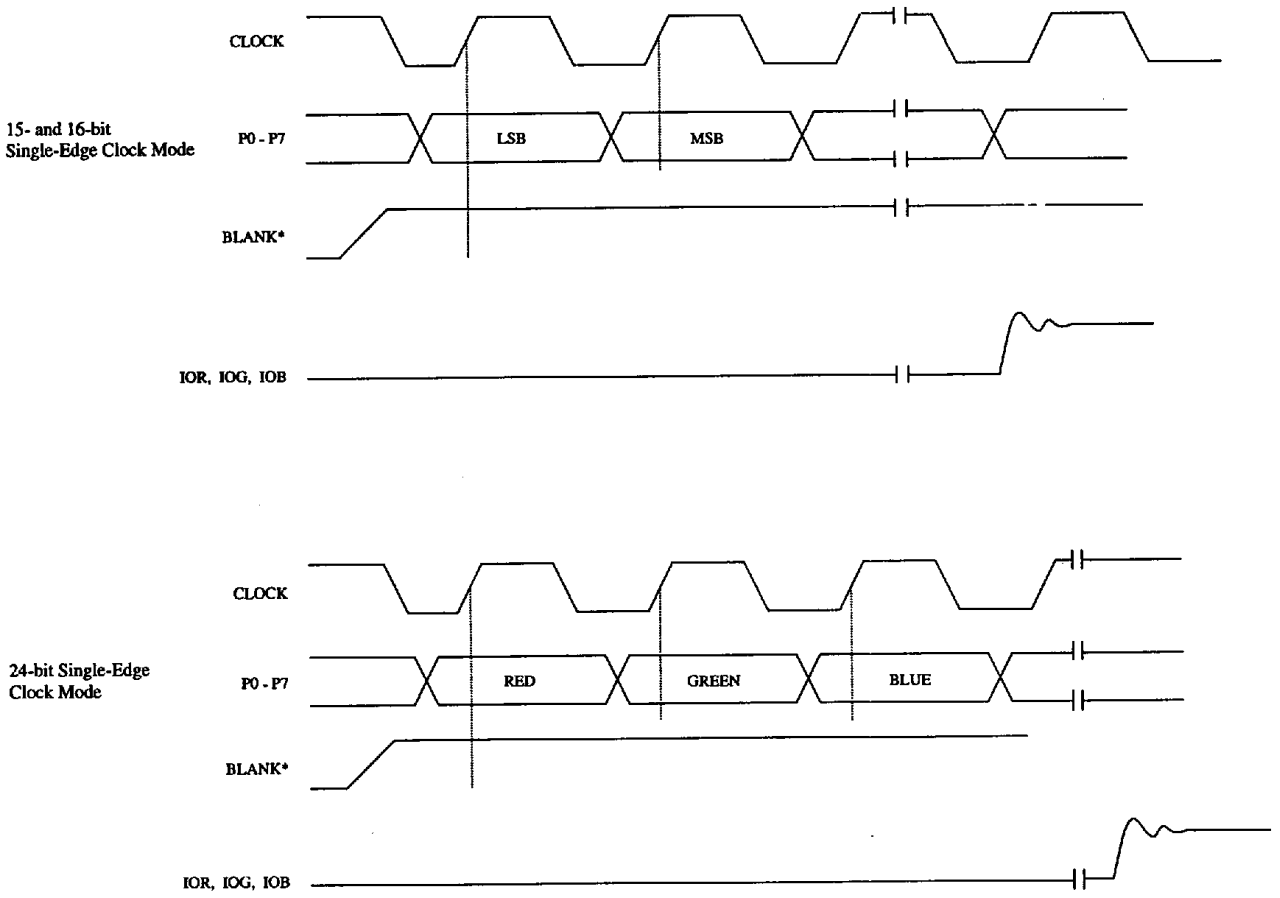


15-, 16-, and 32-bit-per-Pixel Timing, Dual-Edge Clock Mode.

4

Timing Waveforms

T-52-33-43



15-, 16-, and 24-bit-per-Pixel Timing, Single-Edge Clock Mode.

Ordering Information

T-52-33-43

Model Number	Color Palette RAM	Overlay Palette	Speed	Package	Ambient Temperature Range
Bt481KPJ85	256 x 24	15 x 24	85 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt481KPJ75	256 x 24	15 x 24	75 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt482KPJ85	256 x 24	15 x 24	85 MHz	44-pin Plastic J-Lead	0° to +70° C
Bt482KPJ75	256 x 24	15 x 24	75 MHz	44-pin Plastic J-Lead	0° to +70° C