YAMAHA

YTD428

APPLICATION MANUAL

IDSU

ISDN DSU for Terminal Equipment

YAMAHA CORPORATION

YTD428 APPLICATION MANUAL
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Contents

1. INTRODUCTION

YTD428 is a LSI which provides the ISDN subscriber interface (two-wire time compression multiplexing operation) and the NT side of the ISDN Basic Rate user-network interface function (digital four-wire time-division full-duplex operation). It is capable of providing the electric characteristics conforming to TTC Standard JT-I430 and JT-G961.

YTD428 incorporates the circuit termination and line termination functions on a single chip allowing the user to easily configure a DSU (Digital Service Unit) that consumes small amount of power at a minimal cost.

In addition, a TTL interface is provided at the T reference point (layer 1 level). This feature is especially effective when combined with YAMAHA's ISDN LSI for S/T reference point interface, YTD423 or YTD418. It allows considerable cost reduction on parts around the pulse transformer when constructing a device with a built-in DSU.

The driver/receiver section of the T reference point interface can be separated from the DSU section and be used independently. The user can enable or disable this feature as necessary.

1.1 Features

■ Circuit Termination Section

- ■ Conforms to TTC Standard JT-I430 and JT-G961
- • Digital four-wire time-division full-duplex operation
- • Two-wire time compression multiplexing operation
- • Transmission rate at U reference point: 320 kbit/s, at T reference point: 192 kbit/s
- • Frame assembling and disassembling function
- • State transition control
- • Loopback function
- • T reference point timing control
  (switch between short passive bus / extended passive bus, point-to-point)
- • U reference point driver control

■ Line Termination Section

- ■ Conforms to TTC Standard JT-G961
- • $\sqrt{f}$ equalizer
- • Bridged tap equalizer

■ T Reference Point Interface Section

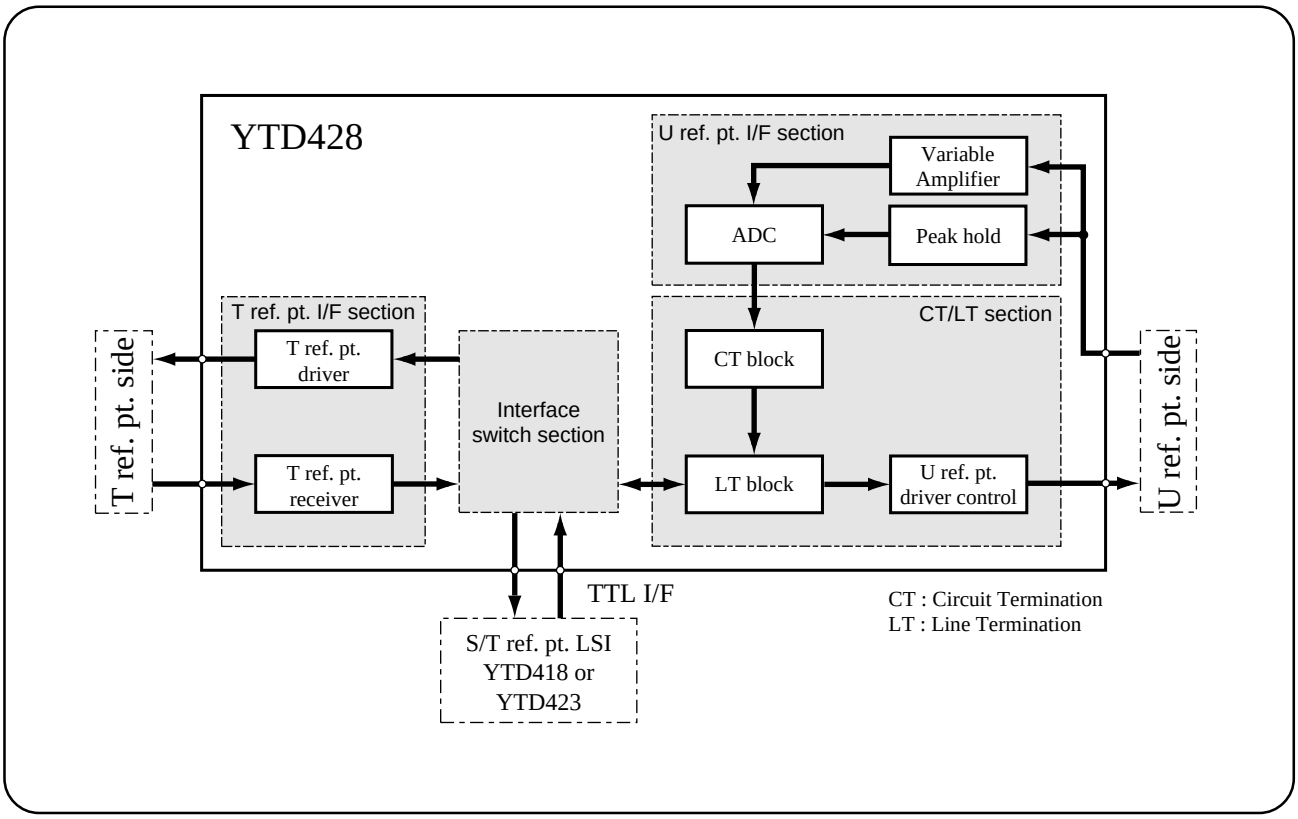
- • The T reference point driver / receiver section can be separated from DSU section, and use independently (TE mode). The user can enable or disable this feature as necessary.

■ Others

- • +5 V single power supply
- • Low power consumption
- • 100 pin SQFP

2. BLOCK DIAGRAM

2.1 Internal Block Diagram

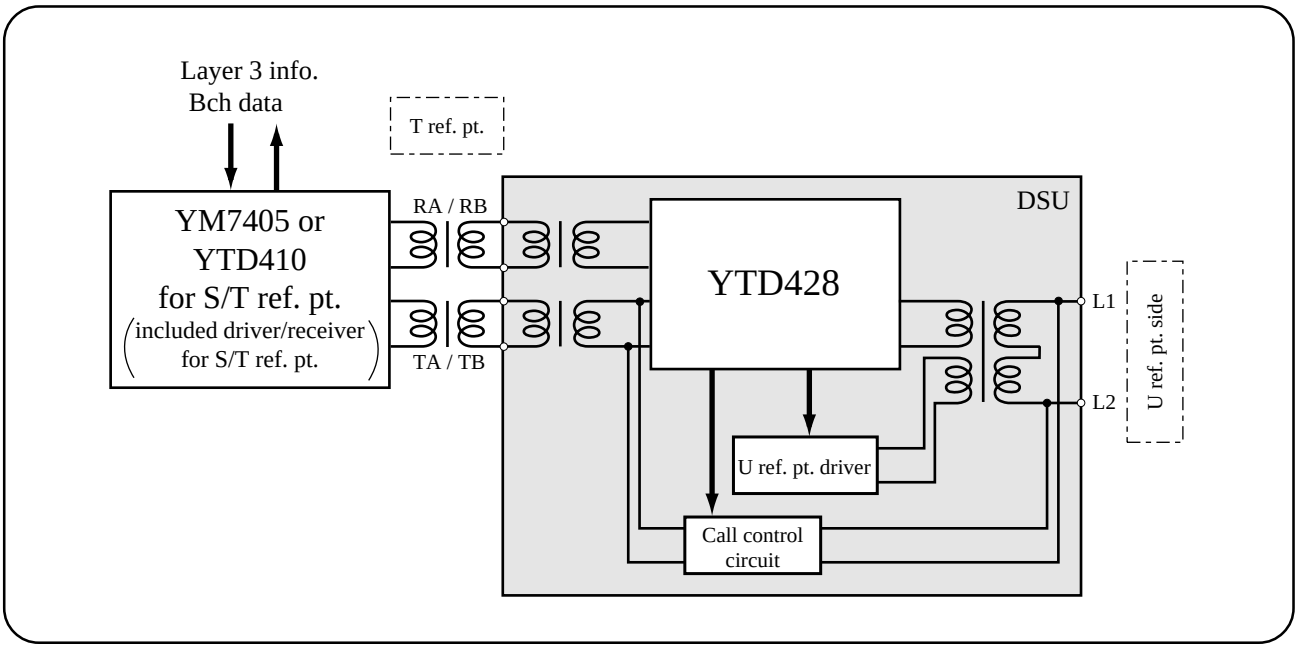


2.2 DSU Configuration Example

YTD428 incorporates the circuit termination, line termination, T reference point interface and U reference point interface functions on a single chip allowing the user to easily configure a DSU that consumes small amount of power at a minimal cost. The user can select from the two types of configurations. One is the general configuration in which a transformer is used at the T reference point interface. The other is a configuration in which a TTL interface is used to directly connect to the T reference point LSI.

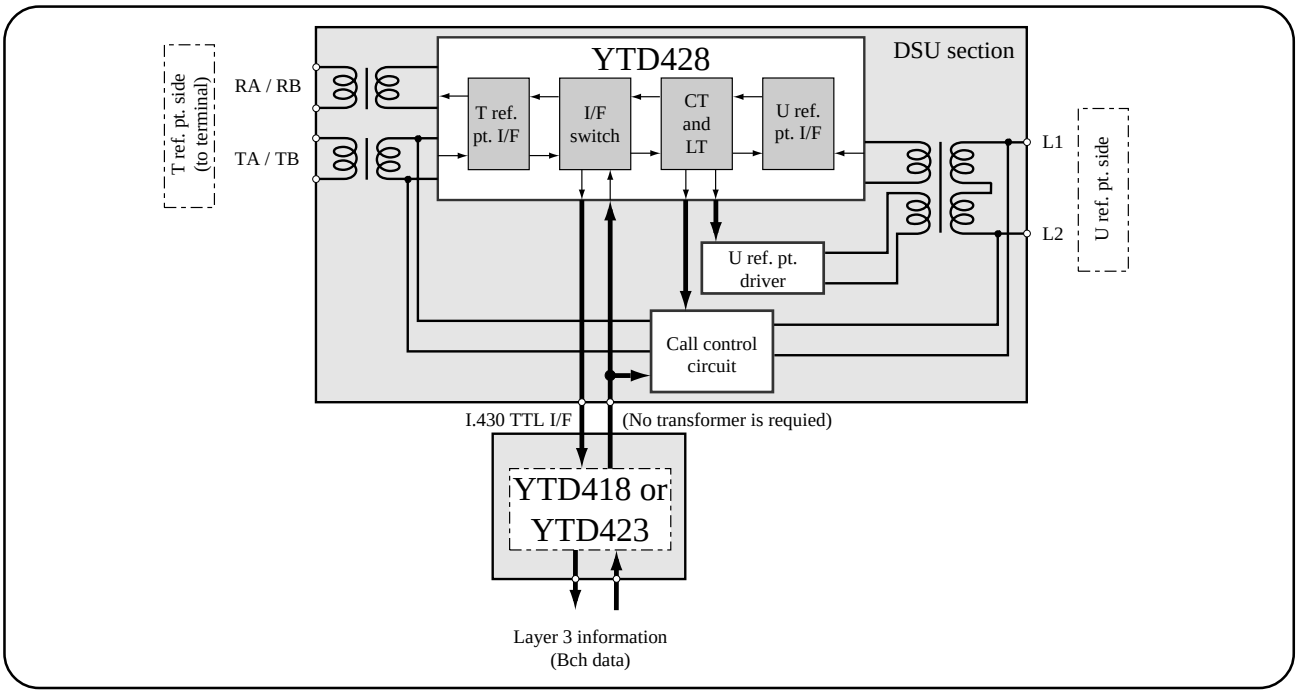
■ Configuration example of a general DSU

Various functions are incorporated on a single chip allowing the user to create a low power-consuming product at a low cost.



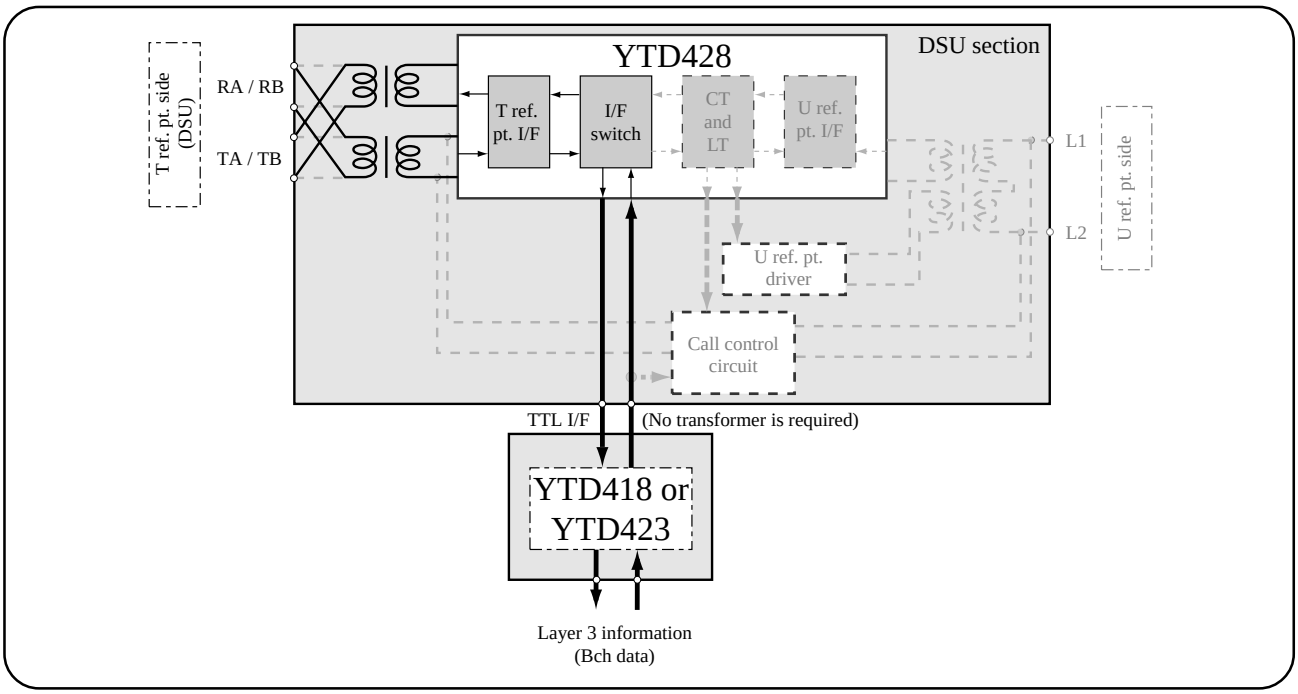
■ Configuration example of a device with a built-in DSU that uses an I.430 TTL interface at the T ref. pt.

When using YTD428 with YAMAHA'S S/T reference point interface LSI to create a device with a built-in DSU, they can be connected directly through the I.430 TTL interface. This results in a reduction of pulse transformer parts.



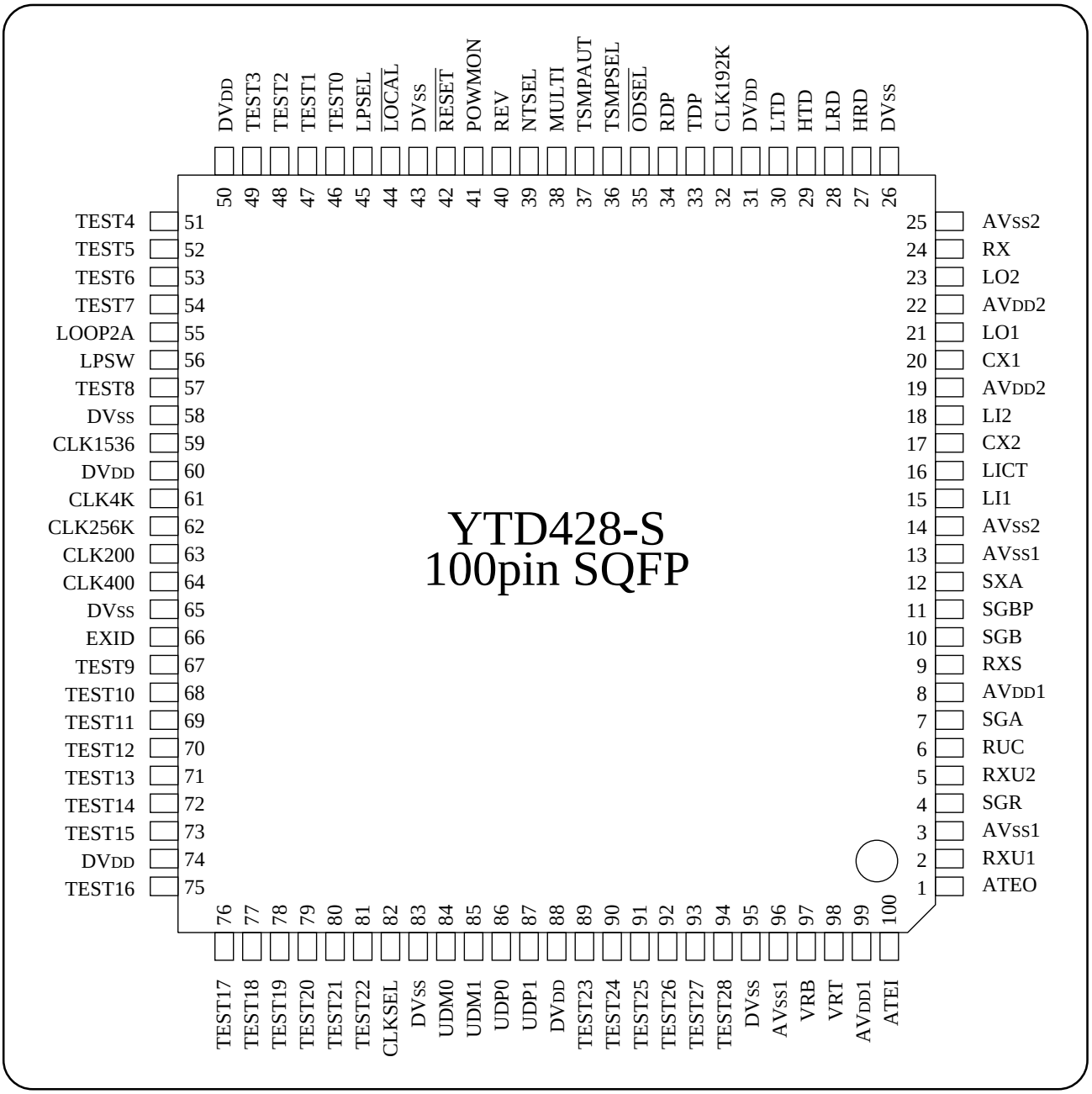
■ Example of using T reference point driver / receiver section independently

By setting the Interface switch, the drive / receiver of the T reference point interface section can be separated from the circuit termination (CT) and line termination (LT) section and be used independently.
The user can enable or disable this feature as necessary.



3. PIN DESCRIPTIONS

3.1 Pin Assignments



3.2 Pin Functions

■ Common Section

Pin No.	Pin Name	I/O	Function	Remarks
3, 13, 96	$AV_{SS}1$	GND	Analog ground 1 (U ref. pt.)	
14, 25	$AV_{SS}2$	GND	Analog ground 2 (T ref. pt.)	
26, 43, 58, 65, 83, 95	DV_{SS}	GND	Digital ground	
8, 99	$AV_{DD}1$	PWR	+5 V ± 5 % analog power supply 1 (U ref. pt.)	
19, 22	$AV_{DD}2$	PWR	+5 V ± 5 % analog power supply 2 (T ref. pt.)	
31, 50, 60 74, 88	DV_{DD}	PWR	+5 V ± 5 % digital power supply	
59	CLK1536	IN	System clock (15.36 MHz ± 50 ppm or less)	
41	POWMON	IN	Power supply monitor of the equipment on the T ref. pt. side "H": Power supply OFF "L": Power supply ON	
42	$\overline{\text{RESET}}$	IN	Haerdware reset Apply the reset pulse for 1 ms or more after the clock oscillation to operate hardware reset. If the pulse is less than 1 ms, the operation is unpredictable. Hardware reset is required when all following conditions are met. 1. operated by local power 2. LPSEL = "H" 3. U ref. pt. polarity is positive.	

Note Connect input pins that are not normally used to the power supply pin or ground pin.
In the same fashion, do not leave pins with pull-up resistor open. Connect them to the power supply pin or ground pin.

■ Mode Setting Section

Pin No.	Pin Name	I/O	Function	Remarks
33	TDP	IN	HTD, LTD pulse polarity setting "H": positive polarity "L": negative polarity	with pull-up resistor
34	RDP	IN	HRD, LRD pulse polarity setting "H": positive polarity "L": negative polarity	with pull-up resistor
35	$\overline{\text{ODSEL}}$	IN	T ref. pt. transmit signal setting "H": HRD, LRD pins normal output "L": HRD, LRD pins open drain	with pull-up resistor
36	TSMPSEL	IN	T ref. pt. receive data sampling timing setting "H": fixed timing (short passive bus) When T ref. pt. data sampling mode is set to "automatic" (TSMPAUT = "L"), set this pin to "H". "L": adaptive timing (point-to-point connection, extended passive bus)	with pull-up resistor
37	TSMPAUT	IN	T ref. pt. data sampling mode setting "H": manual setting (TSMPSEL pin state is valid) "L": automatic setting (set TSMPSEL pin to "H")	with pull-up resistor
38	MULTI	IN	T ref. pt. multiframe support setting "H": support multiframe "L": do not support multiframe	with pull-up resistor
39	NTSEL	IN	T ref. pt. mode setting "H": NT mode "L": TE mode (T ref. pt. I/F block operates independently of DSU block)	with pull-up resistor
44	$\overline{\text{LOCAL}}$	IN	Power feeding mode setting "H": phantom power feeding mode "L": local power fedding mode	with pull-up resistor
45	LPSEL	IN	LPSW signal setting "H": call only extended loopback 2A "L": normal call, call by extended loopback 2A (loop control signal at local power feeding mode)	with pull-up resistor
66	EXID	IN	Loopback setting "H": transmit ID1 = "1" (correspond to extended loopback 2) "L": transmit ID1 = "0" (loopback 2A operates at AP = "1")	with pull-up resistor
82	CLKSEL	IN	Clock output setting "H": do not output clock "L": output clock	with pull-up resistor

Note 1 When not using TTL interface, set HTD, LTD pins as bellow.
When TDP = “H”, set HTD, LTD = “L”
When TDP = “L”, set HTD, LTD = “H”

Note 2 When using the YTD428 on a terminal with built-in DSU, it is recommended that fixed timing be selected for the sample timing of T reference point receive data (TSMPSEL=“H” and TSMPAUT=“H”). This is because the bus distribution form becomes a short passive bus in this case.

Note 3 When using NTSEL, external terminating resistor setting is required.
When NTSEL = “H”, terminating resistor is required.
When NTSEL = “L”, remove terminating resistor as necessary.

Note 4 Set $\overline{\text{LOCAL}}$ = “L” when LPSEL = “L” or CLKSEL = “L”.

■ T Reference Point Section

Pin No.	Pin Name	I/O	Function	Remarks
15	LI1	IN	S/T line input	
16	LICT	OUT	S/T line reference source output	
17	CX2	-	Connecting external capacitor and resistor 0.1 µF capacitor and 1 MΩ resistor are to be connected across the CX2 pin and the AVss2 pin.	
18	LI2	IN	S/T line input	
20	CX1	-	Connecting external capacitor 22 µF capacitor is to be connected across the CX1 pin and the AVss2 pin.	
21	LO1	OUT	S/T line output	
23	LO2	OUT	S/T line output	
24	RX	-	Connecting external resistor 33 kΩ resistor is to be connected across the RX pin and the AVss2 pin .	

Note 1 When not using T ref. pt. analog interface, set these pins as bellow.
The LI1, LI2 and LICT pins are to be connected each other (short).
0.1 µF capacitor is to be connected across the LICT pin and the AVss2 pin.

Note 2 About how to connect external capacitor and resistor, refer to “REFERENCE CIRCUIT” .

Pin No.	Pin Name	I/O	Function	Remarks
27	HRD	OUT	NTSEL = "H": DSU transmit data (+) NTSEL = "L": TE receive data (+)	
28	LRD	OUT	NTSEL = "H": DSU transmit data (–) NTSEL = "L": TE receive data (–)	
29	HTD	IN	NTSEL = "H": DSU receive data (+) NTSEL = "L": TE transmit data (+)	
30	LTD	IN	NTSEL = "H": DSU receive data (–) NTSEL = "L": TE transmit data (–)	

Note When not using TTL interface, set HTD, LTD pins as bellow.
When TDP = “H”, set HTD, LTD = “L”
When TDP = “L”, set HTD, LTD = “H”

■ U Reference Point Section

Pin No.	Pin Name	I/O	Function	Remarks
2	RXU1	IN	Receive signal input 1	
4	SGR	OUT	Analog signal reference output	
5	RXU2	IN	Receive signal input 2	
6	RUC	-	0.1 µF capacitor is to be connected across the RUC pin and the AVss1 pin.	
7	SGA	-	0.0047 µF (10%) capacitor is to be connected across the SGA pin and the SGR pin.	
9	RXS	-	0.0022 µF (10%) capacitor is to be connected across the RXS pin and the SGR pin.	
10	SGB	-	0.015 µF (10%) capacitor is to be connected across the SGB pin and the SGR pin.	
11	SGBP	-	0.15 µF (10%) capacitor is to be connected across the SGBP pin and the SGR pin.	
12	SXA	-	This pin must be left unconnected.	
97	VRB	OUT	ADC reference power supply (low voltage) 0.1 µF capacitor is to be connected across the VRB pin and the AVss1 pin.	
98	VRT	OUT	ADC reference power supply (high voltage) 0.1 µF capacitor is to be connected across the VRT pin and the AVss1 pin.	

Pin No.	Pin Name	I/O	Function	Remarks
84	UDM0	OUT	Negative pulse driving signal	
85	UDM1	OUT	Negative pulse driving signal	
86	UDP0	OUT	Positive pulse driving signal	
87	UDP1	OUT	Positive pulse driving signal	

Pin No.	Pin Name	I/O	Function	Remarks
40	REV	IN	U ref. pt. polarity When LPSEL = "H", set this pin to "H". When LPSEL = "L", set this pin as bellow. "L": positive polarity "H": reverse polatity	
55	LOOP2A	OUT	"L": normal operation "H": indicating loopbak 2	
56	LPSW	OUT	Call control signal "L": normal operation "H": call initiate request	

■ Clock Output Pins

Pin No.	Pin Name	I/O	Function	Remarks
32	CLK192K	OUT	192 kHz clock (usually fixed to "L") Output clock when CLKSEL = "L" and LOCAL = "L".	**Note 1, 2**
61	CLK4K	OUT	4 kHz clock (usually fixed to "L") Output clock when CLKSEL = "L" and LOCAL = "L".	**Note 1, 2**
62	CLK256K	OUT	256 kHz clock (usually fixed to "L") Output clock when CLKSEL = "L" and LOCAL = "L".	**Note 1**
63	CLK200	OUT	200 Hz clock (usually fixed to "L") Output clock when CLKSEL = "L".	**Note 1, 2**
64	CLK400	OUT	400 Hz clock (usually fixed to "L") Output clock when CLKSEL = "L".	**Note 1, 2**

Note 1 Outputs “L” when the YTD428 is set to not output the clock. In addition, if the YTD428 is not synchronized to the network, the frequency of the output clock is not guaranteed.

Note 2 Clock is output when REV = “H.”

■ Test Pins

These are for LSI examinations, and not used in normal operation.

Be sure that each pin is set as bellow.

Pin No.	Pin Name	I/O	Function	Remarks
46, 48, 49, 51 ~ 54, 57, 67, 80, 81	TEST0, 2 ~ 9, 21, 22	IN	Test pin Usually fixed to "H".	with pull-up resistor
89, 91 ~ 93	TEST 23, 25 ~ 27	IN	Test pin Usually fixed to "L".	
94	TEST28	IN	Test pin Usually fixed to "H".	
47, 75 ~ 78	TEST1, 16 ~ 19	I/O	Test pin Usually pull up to "H".	with pull-up resistor
68, 69, 90	TEST10, 11, 24	I/O	Test pin Usually pull up to "H".	
70 ~ 73	TEST 12 ~ 15	I/O	Test pin Usually fixed to "L".	
79	TEST20	OUT	Test pin This pin must be left unconnected.	
100	ATEI	IN	Test pin Usually fixed to "L".	
1	ATEO	I/O	Test pin Usually pulled up to "H".	

4. DETAILS OF FUNCTIONS

4.1 U Reference Point Section

■ Variable Amplifier

This block amplifies the receive signal amplitude to the maximum dynamic range.

■ ADC

This block makes an A/D conversion of the received signal and transfers it to the line termination block.

■ Peak Hold

This block is performed during the initial training so that the gain of the Variable amplifier block is set to make best communication condition.

4.2 Circuit Termination / Line Termination Section

■ Circuit Termination Block

The following functions provide the necessary functions for TTC Standard JT-G961 (TCM operation) and the NT function described in TTC Standard JT-I430.

- Rate adaptation and frame assembly / disassembly at the U and T reference points
- State transition control
- U reference point drive control
- T reference point receive timing control
- Loopback control

  YTD428 supports loopback 2 and loopback C for testing and maintenance.

  These loopback tests are under local switch control.

■ Line Termination Block

The line termination provides the f equalization which compensates the DLL (Digital Local Line) loss and the amplitude distortion, and the BT equalization which compensates the waveform distortion caused by the bridged tap.

4.3 Interface Switch Section

Normally, this section connects T I/F section with CT/LT section to provide DSU function (NTSEL = “H”). By setting this section, the driver/receiver function of the T I/F section can be separated from the CT/LT section and be used independently (NTSEL = “L”).

For example, it is useful under such a situation that there are some terminals which have DSU function on the same S/T line.

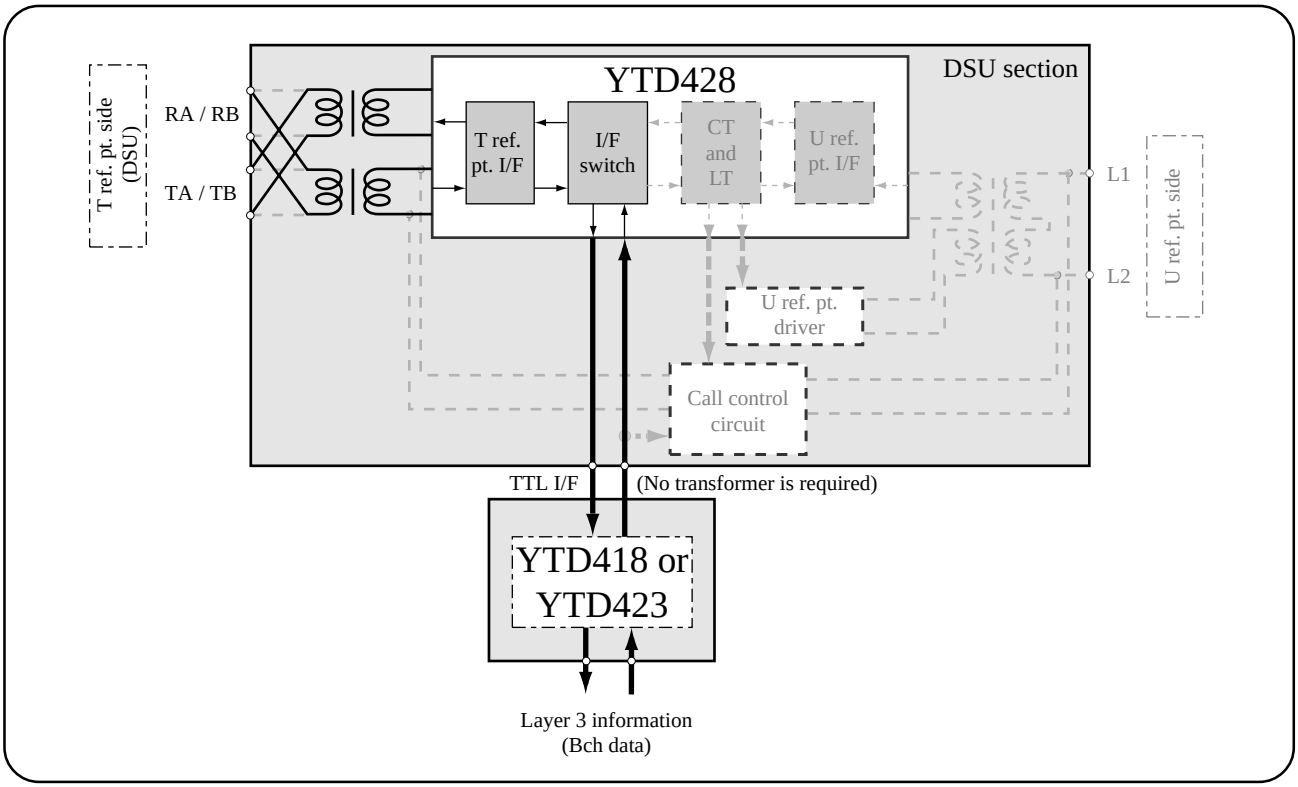


Figure 4.1 Image Of Using T Ref. Pt. I/F Drive/Receiver Independently

In case of using NTSEL = "L" (TE mode), the signals of TA/TB and RA/RB should be reversed by switches or other devices. Because S/T bus signals that are connected to TA, TB, RA and RB pin are different between using YTD428 as DSU (NTSEL = "H") and S/T terminal (NTSEL = "L").

Generally speaking, the terminal resistors are only mounted on the nearest terminal from DSU and other terminals that are connected with the same bus don't require the terminal resistors. Therefore, it is useful that switches which can control ON/OFF of the terminal resistors are provided on the equipment.

4.4 T Reference Interface Section

■ Reference Power Supply Block

This block provides the electric power to supply for the receiver block and the driver block.

■ Receiver Block

The receiver block receives signal from the S/T bus through the external pulse transformer and converts it to the logic level signal.
The voltage threshold level for he receiver is properly adapted automatically according to the receiving signal level.

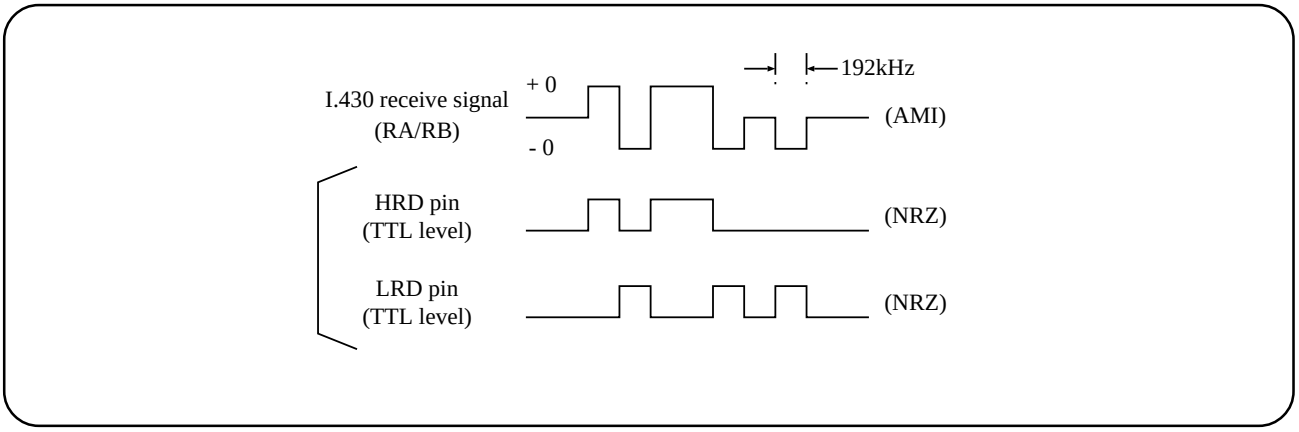


Figure 4.2 Receive Signal Logic (RDP = “H”, NTSEL = “L”)

■ Driver Block

The driver block drives the 2:1 turn ratio transformer according to the logic level transmitting signal.

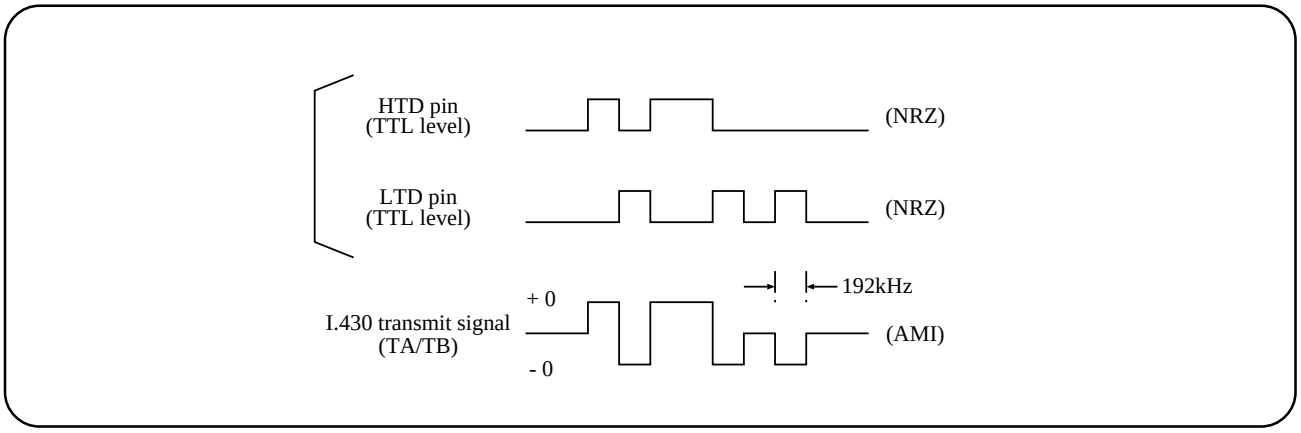


Figure 4.3 Transmit Signal Logic (TDP = “H”, NTSEL = “L”)

5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Parameter	Symbol	Min.	Max	Units
Supply Voltage	V_{DD}	V_{SS} - 0.3	V_{SS} + 7.0	V
Input Voltage	V_I	V_{SS} - 0.3	V_{DD} + 0.3	V
Storage Temperature	T_{stg}	- 50	+ 125	° C

5.2 Recommended Operating Conditions

Parameter	Symbol	Range
Supply Voltage	V_{DD}	5.0 V ± 5 %
Operating Temperature	T_{op}	-20 ~ +70 ° C

5.3 DC Characteristics

(DV_{DD} = AV_{DD} = 5 .0V, DV_{SS} = AV_{SS} = 0.0 V, Operating Temperature: T_{op} = 25 ºC)

Parameter		Symbol	Condition	Min.	Typ.	Max.	Units
Analog Output Allowable Load Impedance		Z_O	**Note 1**	30			kΩ
Analog Receive Buffer Input Impedance		Z_{i1}	**Note 2**	10			MΩ
Analog Signal Reference Voltage		V_{SG}	**Note 3**	2.45	2.50	2.55	V
ADC	Self-Bias VRT	V_{RT}	**Note 4**	0.7AV_{DD} - 0.1	0.7AV_{DD}	0.7AV_{DD} + 0.1	V
	Self-Bias VRB	V_{RB}	**Note 5**	0.3AV_{DD} - 0.1	0.3AV_{DD}	0.3AV_{DD} + 0.1	V

Note 1 With respect to SGR, SXA pins.
Note 2 With respect to RXU1 and RXU2 pins.
Note 3 Set SGR pin to open.
Note 4 With respect to VRT pin.
Note 5 With respect to VRB pin.

(DV_{DD} = AV_{DD} = 5.0 ± 5% V, T_{op} = -20 ~ 70 ºC)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
High Level Input Voltage (TTL)	V_{IH}	(**Note 1**)	2.2			V
	V_{IH}	(**Note 2**)	3.0			V
Low level Input Voltage (TTL)	V_{IL}	(**Note 1**)			0.8	V
	V_{IL}	(**Note 2**)			0.8	V
High Level Input Voltage (CMOS)	V_{IH}	(**Note 3**)	3.5			V
Low Level Input Voltage (COMS)	V_{IL}	(**Note 3**)			1.0	V
High Level Output Voltage (TTL)	V_{OH}	(**Note 4**)	DV_{DD} - 1.0			V
		(**Note 5**)	DV_{DD} - 1.0			V
Low Level Output Voltage (TTL)	V_{OL}	(**Note 4**)			DV_{SS} + 0.4	V
		(**Note 5**)			DV_{SS} + 0.4	V
Low Level Output Voltage (Open-D)	V_{OL}	(**Note 6**)			DV_{SS} + 0.4	V
Leak Current	I_L		-10		10	µA
Idle Condition Leak Current	I_{LZ}		-10		10	µA
Power Supply Current	I_{DD}	(**Note 7**)		36		mA

Note 1 With respect to the digital pins other than $\overline{\text{RESET}}$, POWDET, CLK1536 and TEST23 ~ 28 pins
Note 2 With respect to $\overline{\text{RESET}}$, POWDET pins
Note 3 With respect to CLK1536, TEST23 ~ 28 pins
Note 4 With respect to the pin other than HRD, LRD pins
Test condition: Output Current "H" level (I_{OH}) = -0.2 mA, Output Current "L" level (I_{OL}) = 1.2 mA
Note 5 With respect to HRD, LRD pins (when $\overline{\text{ODSEL}}$ = "H"), Test condition: I_{OH} = -0.2 mA, I_{OL} = 1.2 mA
Note 6 With respect to HRD, LRD pins (when $\overline{\text{ODSEL}}$ = "L"), Test condition: I_{OL} = 1.2 mA
Note 7 When using T ref. pt. analog interface

5.4 AC Characteristics

■ T Reference Point Receive Characteristic (NT mode)

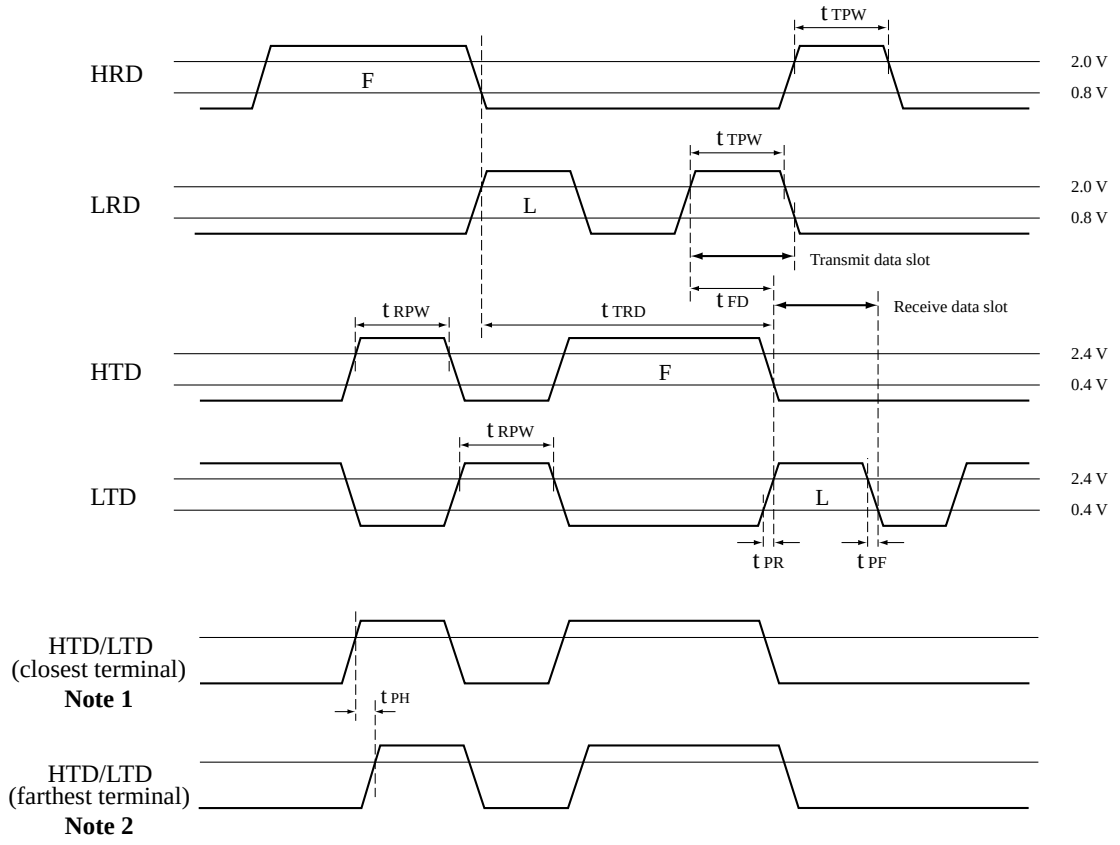
(V_{DD} = 5.0 ± 5% V , T_{op} = -20 ~ 70 °C, Load Capacity: C_L = 50 pF)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Transmit Pulse Width	t_{TPW}		5.00	5.208	5.40	µs
Receive Pulse Width	t_{RPW}			5.208		µs
Rise Time	t_{PR}				260	ns
Fall Time	t_{PF}				30	ns
Phase Diffierence between Tx and Rx signals	t_{TRD}	**Note 1**	10.0		14.0	µs
	t_{TRD}	**Note 2**	10.0		42.0	µs
Phase Difference between Rx signals	t_{PH}	**Note 2**, **Note 3**			2.0	µs

Note 1 With respect to using the Fixed timing

Note 2 With respect to using the Adaptive timing

Note 3 This value shows the difference between two terminals which are connected with bus system.



Note 1 Indicates the terminal that is connected closest from the DSU. The signal from this terminal reaches the DSU the fastest.

Note 2 Indicates the terminal that is connected farthest from the DSU. The signal from this terminal reaches the DSU the slowest.

Figure 5.1 Timing At T Ref. Pt. Interface

■ T Reference Point Receive Characteristic (TE mode)

(V_{DD} = 5.0 ± 5% V, T_{op} = -20 ~ 70 °C, C_L = 50 pF)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Delay Time	t_{RDR}				700	ns
	t_{RDL}				200	ns
	t_{RDH}				700	ns
	t_{RDF}				700	ns
Rise Time	t_{RR}	**Note 1**			30	ns
Fall Time	t_{RF}	**Note 2**			30	ns

Note 1 With respect to HRD, LRD pins ($\overline{ODSEL}$ = “H”)

Note 2 With respect to HRD, LRD pins

Note 3 Figure 5.2 shows the timing when RDP = “H”. When RDP = “L”, the output signal polarity from HRD and LRD pins are inverted.

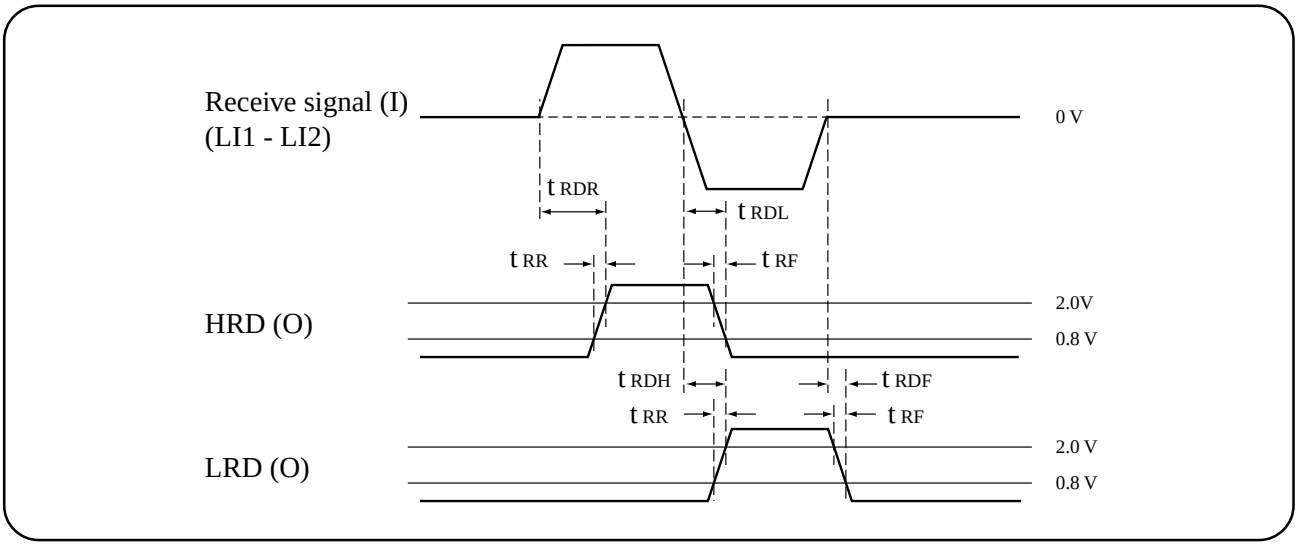


Figure 5.2 Receive Timing

■ T Reference Point Transmit Characteristic (TE mode)

(V_{DD} = 5.0 ± 5% V, T_{op} = -20 ~ 70 °C, C_L = 50 pF)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
HTD, LTD Pulse Period	t_{SW}		4.95		5.45	µs
HTD, LTD Pulse Gap	t_{GAP}		0		260	ns
HTD, LTD Rise Time	t_{SR}				260	ns
HTD, LTD Fall Time	t_{SF}				30	ns
Transmit Signal Delay Time	t_{SRL}	**Note 1**			490	ns
	t_{SRH}	**Note 1**			1010	ns
	t_{SFH}	**Note 1**			165	ns
	t_{SFL}	**Note 1**			685	ns
Zero Cross Delay Time	t_{SDZ}	**Note 1**			1010	ns

Note 1 Measuring with R_L voltage drop as shown in Figure 5.4

Note 2 Figure 5.3 shows the timing when TDP = "H". When TDP = "L", the output signal polarity from HRD and LRD pins are inverted.

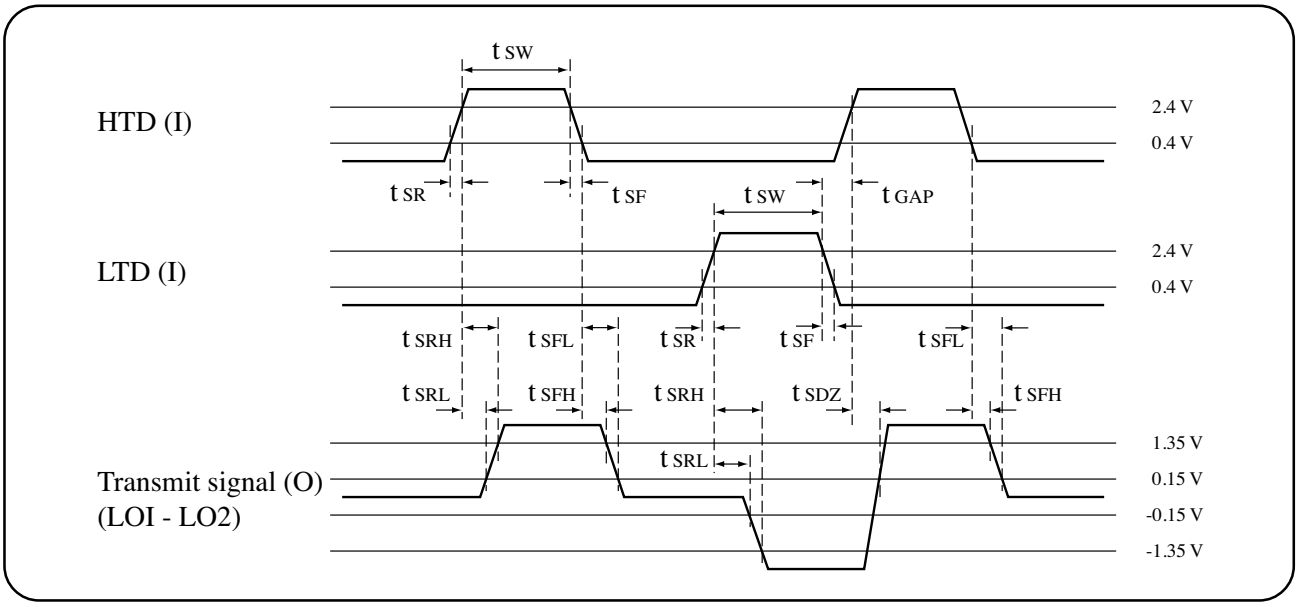


Figure 5.3 Transmit Timing

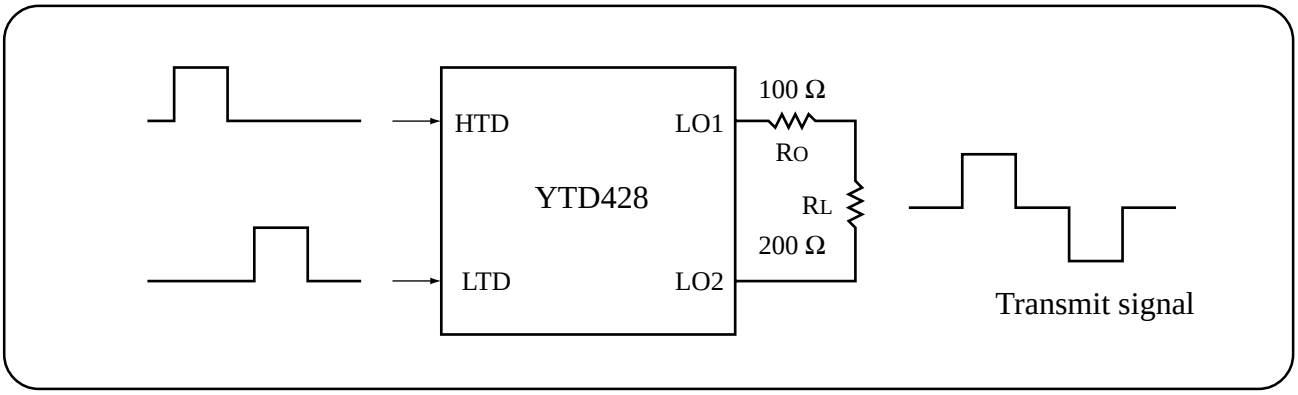


Figure 5.4 Transmit Block Test Circuit

■ Driver, Receiver I/O Impedance

Parameters	Symbol	Condition	Min.	Typ.	Max.	Units
Receiver Input Impedance	Z_{LI}	LI1 - LI2	50			kΩ
Driver Ouput Impedance	Z_{LO1}	LO1 - LO2 (Note1)	50			kΩ
Driver Ouput Impedance	Z_{LO0}	LO1 - LO2 (Note2)		15		Ω

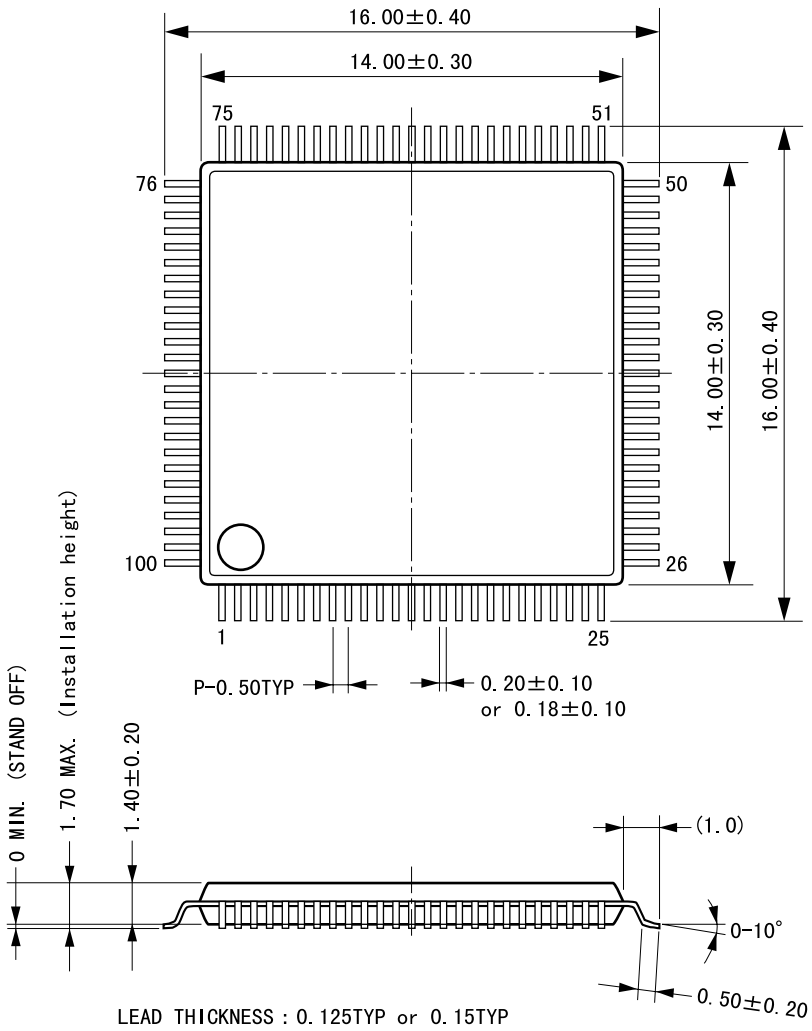
Note 1 When no pulse is output.

Note 2 When pulse is output.

◄

6. PIN DESCRIPTIONS

C-PK100SP-1



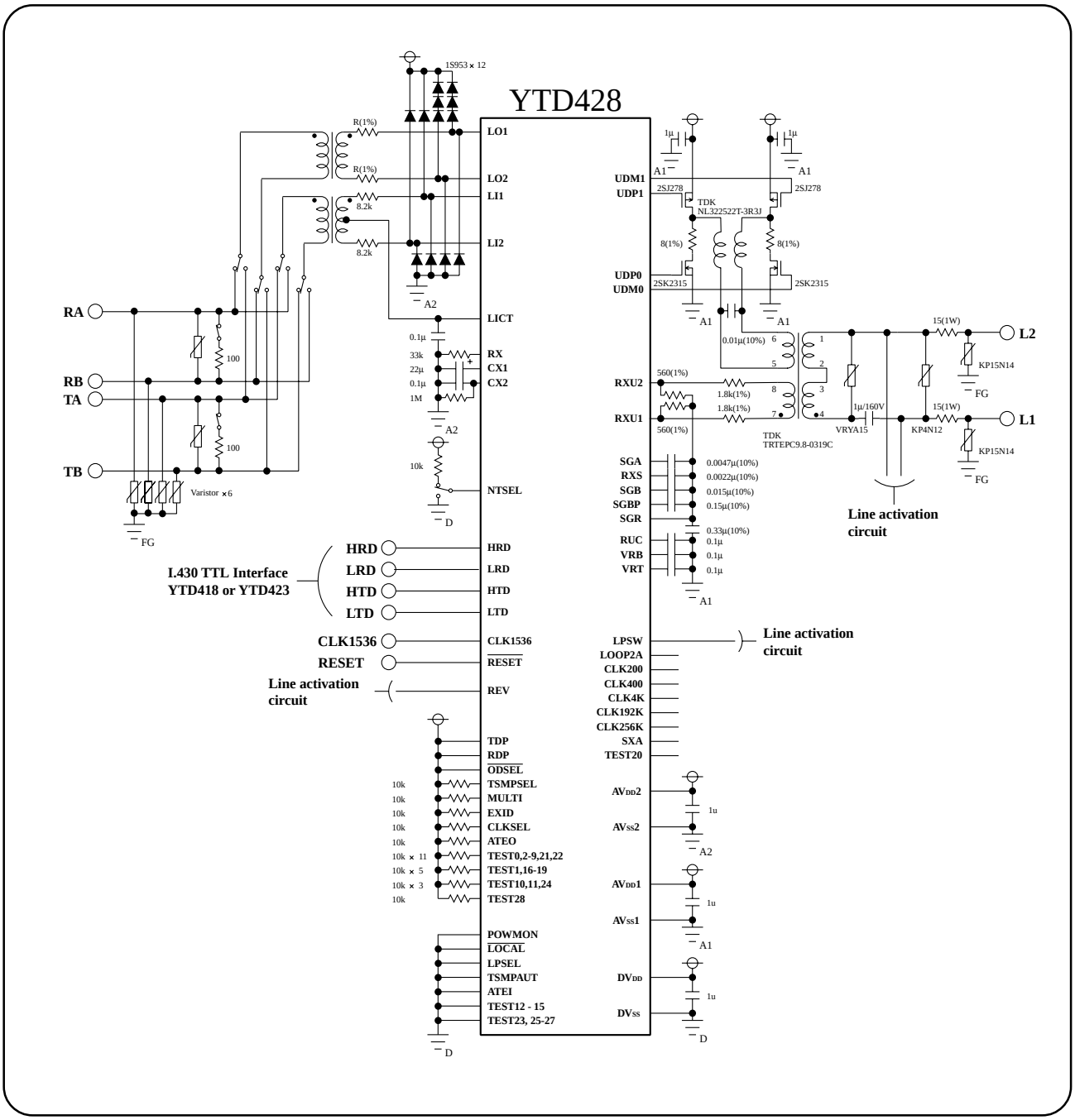
(UNIT) : mm (millimeters)

The shape of the molded corner may slightly different from the shape in this diagram.

The figure in the parenthesis ( ) should be used as a reference.
Plastic body dimensions do not include burr of resin.
UNIT: mm

REFERENCE CIRCUIT

The reference circuit using YTD428 is shown as bellow.



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Notice The specifications of this product are subject to improvement changes without prior notice.

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YAMAHA CORPORATION

Address inquiries to:
Semiconductor Sales & Marketing Department

■ Head Office 203, Matsunokijima, Toyooka-mura
Iwata-gun, Shizuoka-ken, 438-0192, Japan
Tel. +81-539-62-4918 Fax. +81-539-62-5054

■ Tokyo Office 2-17-11, Takanawa, Minato-ku,
Tokyo, 108-8568, Japan
Tel. +81-3-5488-5431 Fax. +81-3-5488-5088

■ Osaka Office 3-12-12, Minami Senba, Chuo-ku,
Osaka City, Osaka, 542-0081, Japan
Tel. +81-6-6252-6221 Fax. +81-6-6252-6229

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