YAMAHA LSI

YTD428

IDSU

DSU LSI for the ISDN Terminal Equipment

INTRODUCTION

YTD428 is a LSI which provides the ISDN subscriber interface (two-wire time compression multiplexing operation) and the NT side of the ISDN Basic Rate user-network interface function (digital four-wire time-division full-duplex operation). It is capable of providing the electric characteristics conforming to TTC Standard JT-I430 and JT-G961.

YTD428 incorporates the circuit termination and line termination functions on a single chip allowing the user to easily configure a DSU (Digital Service Unit) that consumes small amount of power at a minimal cost.

In addition, a TTL interface is provided at the T reference point (layer 1 level). This feature is especially effective when combined with YAMAHA's ISDN LSI for S/T reference point interface, YTD423 or YTD418. It allows considerable cost reduction on parts around the pulse transformer when constructing a device with a built-in DSU.

The driver/receiver section of the T reference point interface can be separated from the DSU section and be used independently. The user can enable or disable this feature as necessary.

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YTD428 CATALOG
CATALOG No.:4TD428A2
2001.1

❒ Features

■ Circuit Termination Section

- ■ Conforms to TTC Standard JT-I430 and JT-G961
- • Digital four-wire time-division full-duplex operation
- • Two-wire time compression multiplexing operation
- • Transmission rate at U reference point: 320 kbit/s, at T reference point: 192 kbit/s
- • Frame assembling and disassembling function
- • State transition control
- • Loopback function
- • T reference point timing control
  (switch between short passive bus / extended passive bus, point-to-point)
- • U reference point driver control

■ Line Termination Section

- ■ Conforms to TTC Standard JT-G961
- • $\sqrt{f}$ equalizer
- • Bridged tap equalizer

■ T Reference Point Interface Section

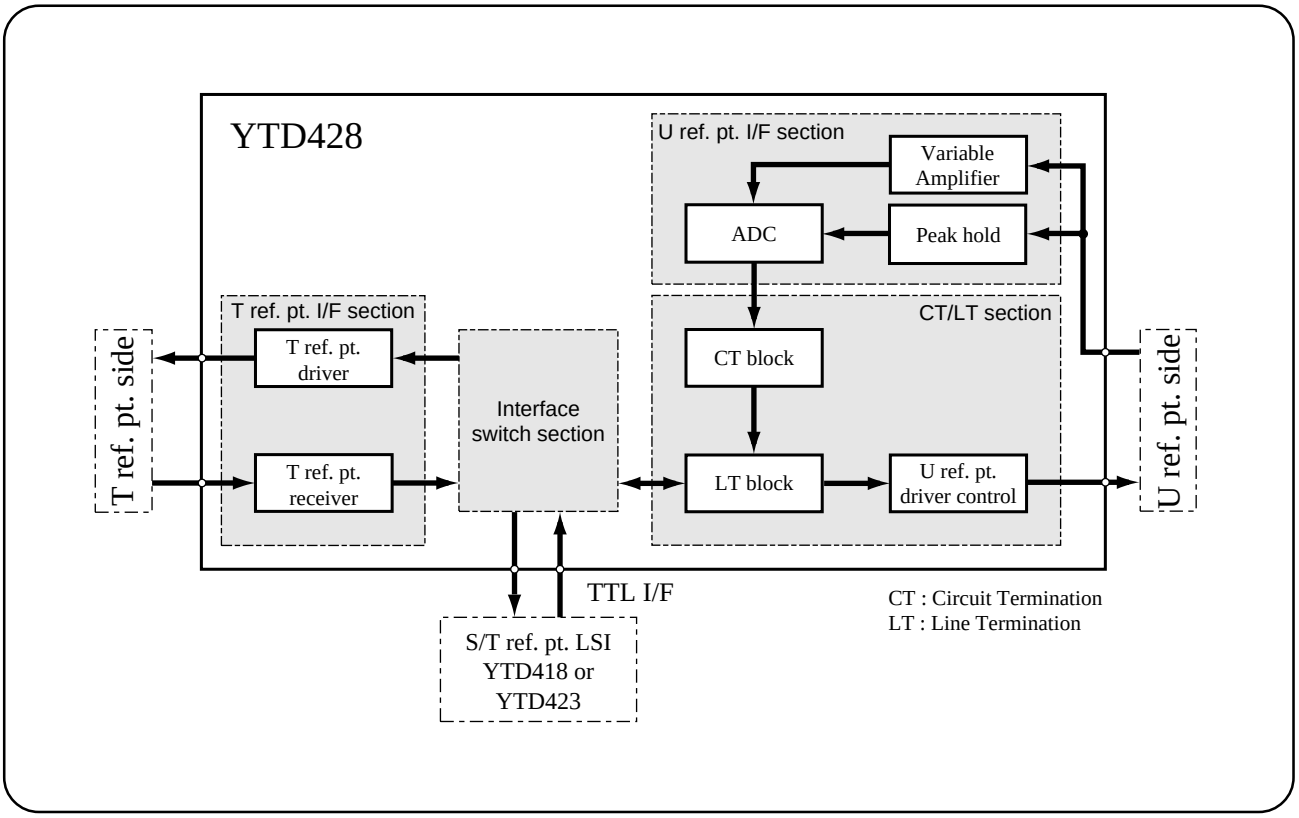
- • The T reference point driver / receiver section can be separated from DSU section, and use independently (TE mode). The user can enable or disable this feature as necessary.

■ Others

- • +5 V single power supply
- • 100 pin SQFP

BLOCK DIAGRAM

❒ Internal Block Diagram

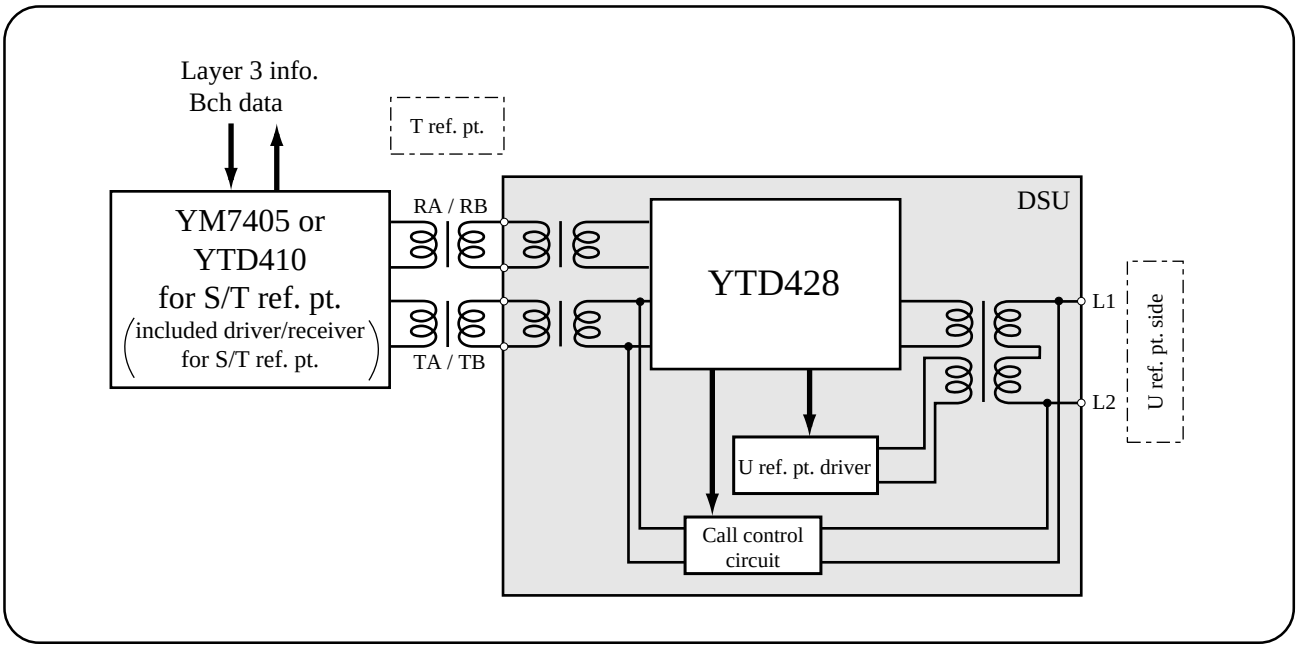


❒ DSU Configuration Example

YTD428 incorporates the circuit termination, line termination, T reference point interface and U reference point interface functions on a single chip allowing the user to easily configure a DSU that consumes small amount of power at a minimal cost. The user can select from the two types of configurations. One is the general configuration in which a transformer is used at the T reference point interface. The other is a configuration in which a TTL interface is used to directly connect to the T reference point LSI.

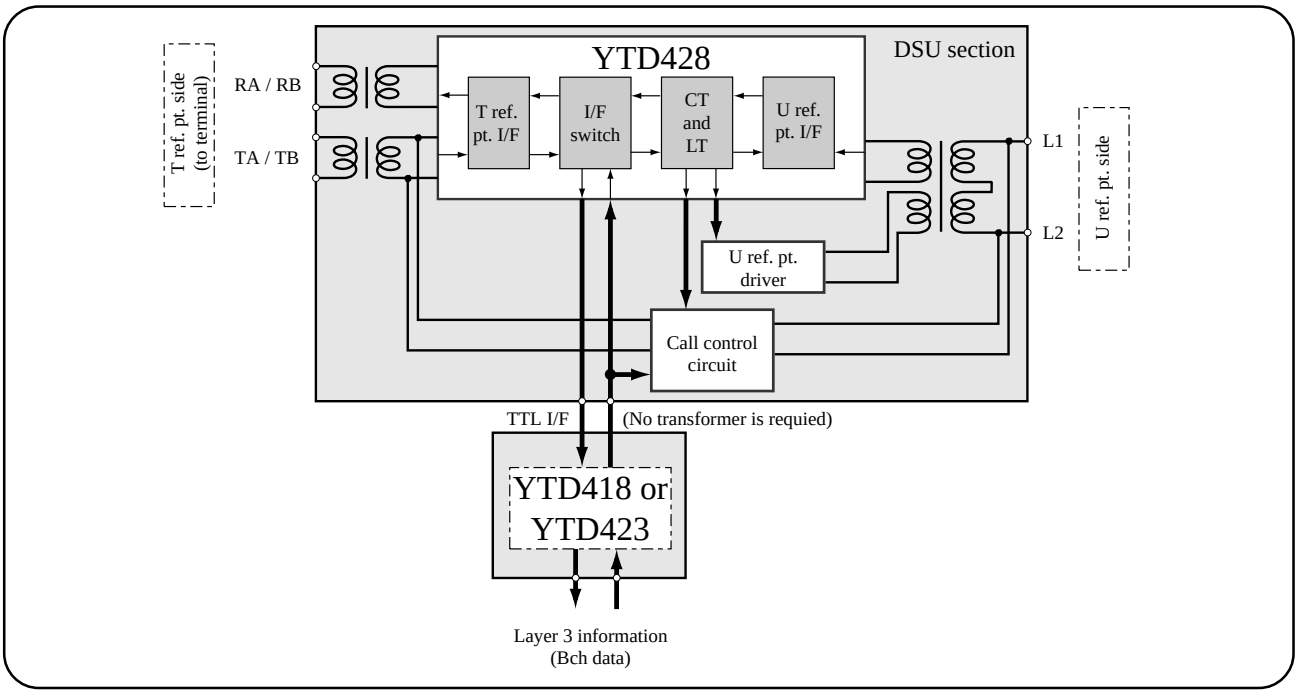
■ Configuration example of a general DSU

Various functions are incorporated on a single chip allowing the user to create a low power-consuming product at a low cost.



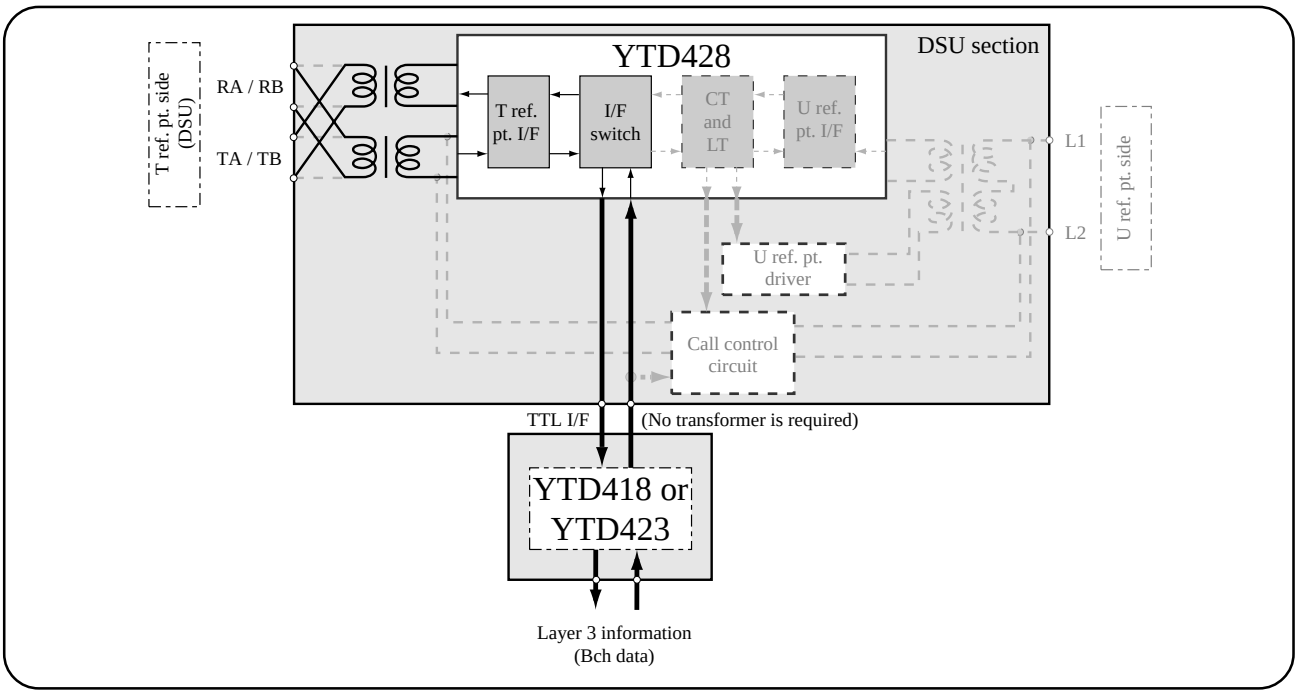
■ Configuration example of a device with a built-in DSU that uses a TTL interface at the T ref. pt.

When using YTD428 with YAMAHA'S S/T reference point interface LSI to create a device with a built-in DSU, they can be connected directly through the TTL interface. This results in a reduction of pulse transformer parts.

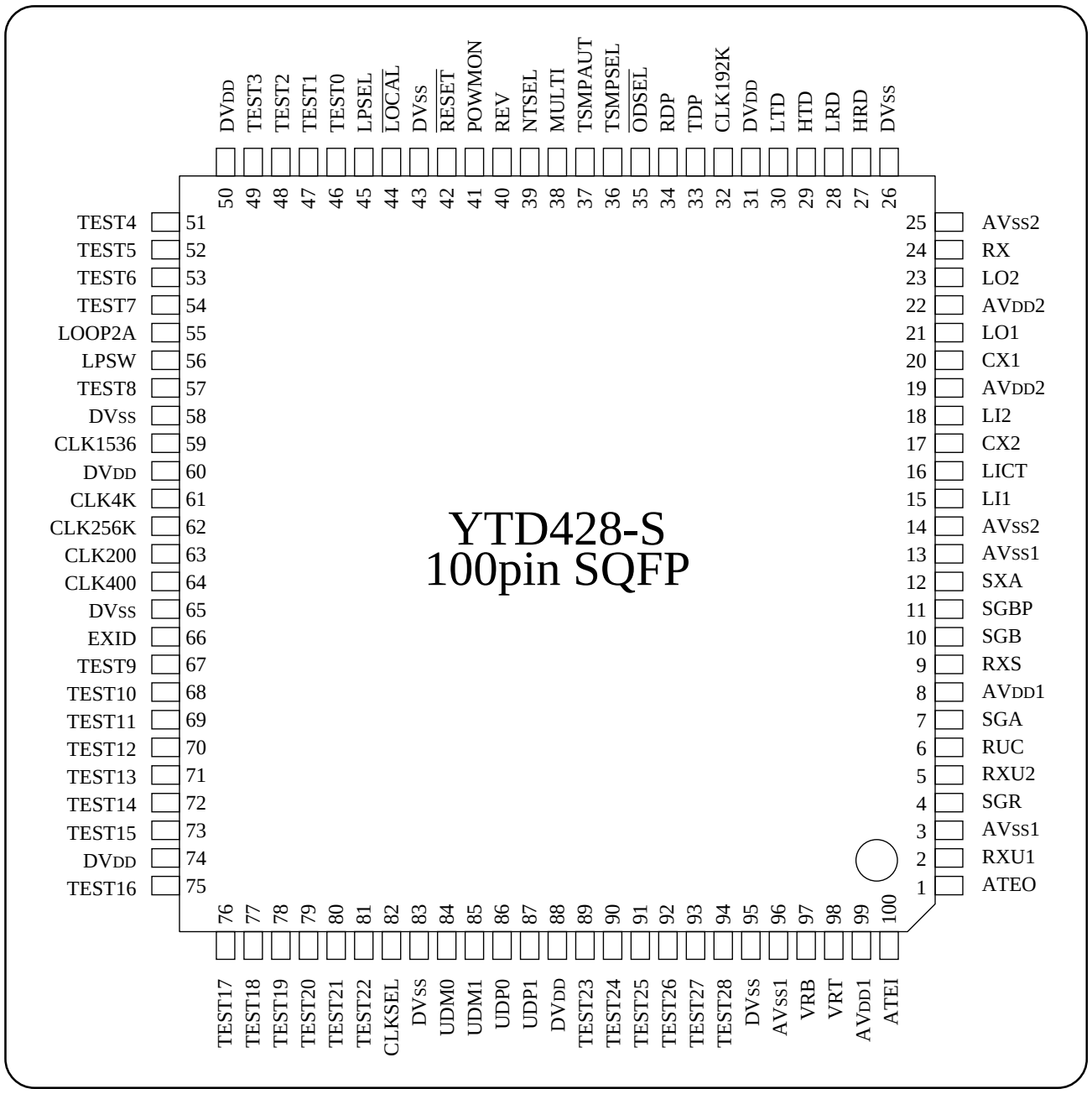


■ Example of using T reference point driver / receiver section independently

By setting the Interface switch, the drive / receiver of the T reference point interface section can be separated from the circuit termination (CT) and line termination (LT) section and be used independently.
The user can enable or disable this feature as necessary.



Pin Assignments



ELECTRICAL CHARACTERISTICS

❒ Absolute Maximum Ratings

Parameter	Symbol	Min.	Max	Units
Supply Voltage	V_{DD}	V_{SS} - 0.3	V_{SS} + 7.0	V
Input Voltage	V_I	V_{SS} - 0.3	V_{DD} + 0.3	V
Storage Temperature	T_{stg}	- 50	+ 125	° C

❒ Recommended Operating Conditions

Parameter	Symbol	Range
Supply Voltage	V_{DD}	5.0 V ± 5 %
Operating Temperature	T_{op}	-20 ~ +70 ° C

◄

❒ DC Characteristics

(DV_{DD} = AV_{DD} = 5 .0V, DV_{SS} = AV_{SS} = 0.0 V, Operating Temperature: T_{op} = 25 ºC)

Parameter		Symbol	Condition	Min.	Typ.	Max.	Units
Analog Output Allowable Load Impedance		Z_O	Note 1	30			kΩ
Analog Receive Buffer Input Impedance		Z_{i1}	Note 2	10			MΩ
Analog Signal Reference Voltage		V_{SG}	Note 3	2.45	2.50	2.55	V
ADC	Self-Bias VRT	V_{RT}	Note 4	0.7AV_{DD} - 0.1	0.7AV_{DD}	0.7AV_{DD} + 0.1	V
	Self-Bias VRB	V_{RB}	Note 5	0.3AV_{DD} - 0.1	0.3AV_{DD}	0.3AV_{DD} + 0.1	V

Note 1 With respect to SGR, SXA pins.
Note 2 With respect to RXU1 and RXU2 pins.
Note 3 Set SGR pin to open.
Note 4 With respect to VRT pin.
Note 5 With respect to VRB pin.

(DV_{DD} = AV_{DD} = 5.0 V, T_{op} = -20 ~ 70 ºC)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
High Level Input Voltage (TTL)	V_{IH}	(Note 1)	2.2			V
	V_{IH}	(Note 2)	3.0			V
Low level Input Voltage (TTL)	V_{IL}	(Note 1)			0.8	V
	V_{IL}	(Note 2)			0.8	V
High Level Input Voltage (CMOS)	V_{IH}	(Note 3)	3.5			V
Low Level Input Voltage (COMS)	V_{IL}	(Note 3)			1.0	V
High Level Output Voltage (TTL)	V_{OH}	(Note 4)	DV_{DD} - 1.0			V
		(Note 5)	DV_{DD} - 1.0			V
Low Level Output Voltage (TTL)	V_{OL}	(Note 4)			DV_{SS} + 0.4	V
		(Note 5)			DV_{SS} + 0.4	V
Low Level Output Voltage (Open-D)	V_{OL}	(Note 6)			DV_{SS} + 0.4	V
Leak Current	I_L		-10		10	µA
Idle Condition Leak Current	I_{LZ}		-10		10	µA
Power Supply Current	I_{DD}	(Note 7)		36		mA

Note 1 With respect to the digital pins other than $\overline{\text{RESET}}$, POWMON, CLK1536 and TEST23 ~ 28 pins
Note 2 With respect to $\overline{\text{RESET}}$, POWMON pins
Note 3 With respect to CLK1536, TEST23 ~ 28 pins
Note 4 With respect to the pin other than HRD, LRD pins
Test condition: Output Current "H" level (I_{OH}) = -0.2 mA, Output Current "L" level (I_{OL}) = 1.2 mA
Note 5 With respect to HRD, LRD pins (when $\overline{\text{ODSEL}}$ = "H"), Test condition: I_{OH} = -0.2 mA, I_{OL} = 1.2 mA
Note 6 With respect to HRD, LRD pins (when $\overline{\text{ODSEL}}$ = "L"), Test condition: I_{OL} = 1.2 mA
Note 7 With using T ref. pt. analog interface

❒ AC Characteristics

■ T Reference Point Receive Characteristic (NT mode)

(V_{DD} = 5.0 V, T_{op} = -20 ~ 70 °C, Load Capacity: C_L = 50 pF)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Transmit Pulse Width	t_{TPW}		5.00	5.208	5.40	µs
Receive Pulse Width	t_{RPW}			5.208		µs
Rise Time	t_{PR}				260	ns
Fall Time	t_{PF}				30	ns
Phase Diffierence between Tx and Rx signals	t_{TRD}	Note 1	10.0		14.0	µs
	t_{TRD}	Note 2	10.0		42.0	µs
Phase Difference between Rx signals	t_{PH}	Note 1, Note 3			4.0	µs
	t_{PH}	Note 2, Note 3			2.0	µs

Note 1 With respect to using the Fixed timing

Note 2 With respect to using the Adaptive timing

Note 3 This value shows the difference between two terminals which are connected with bus system.

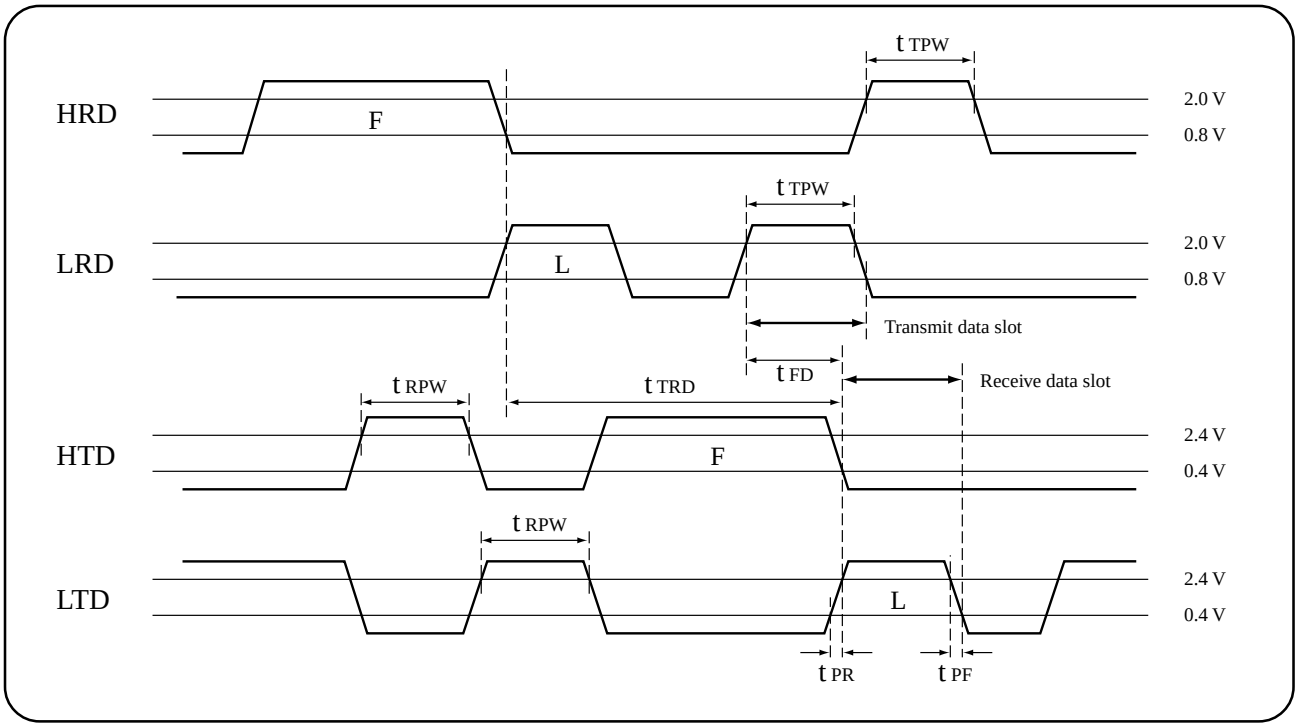


Figure 1 Timing At T Ref. Pt. Interface

■ T Reference Point Receive Characteristic (TE mode)

(V_{DD} = 5.0 V, T_{op} = -20 ~ 70 °C, C_L = 50 pF)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
Delay Time	t_{RDR}				700	ns
	t_{RDL}				200	ns
	t_{RDH}				700	ns
	t_{RDF}				700	ns
Rise Time	t_{RR}	Note 1			30	ns
Fall Time	t_{RF}	Note 2			30	ns

Note 1 With respect to HRD, LRD pins ($\overline{\text{ODSEL}}$ = “H”)

Note 2 With respect to HRD, LRD pins

Note 3 Figure 2 shows the timing when RDP = “H”. When RDP = “L”, the output signal polarity from HRD and LRD pins are inverted.

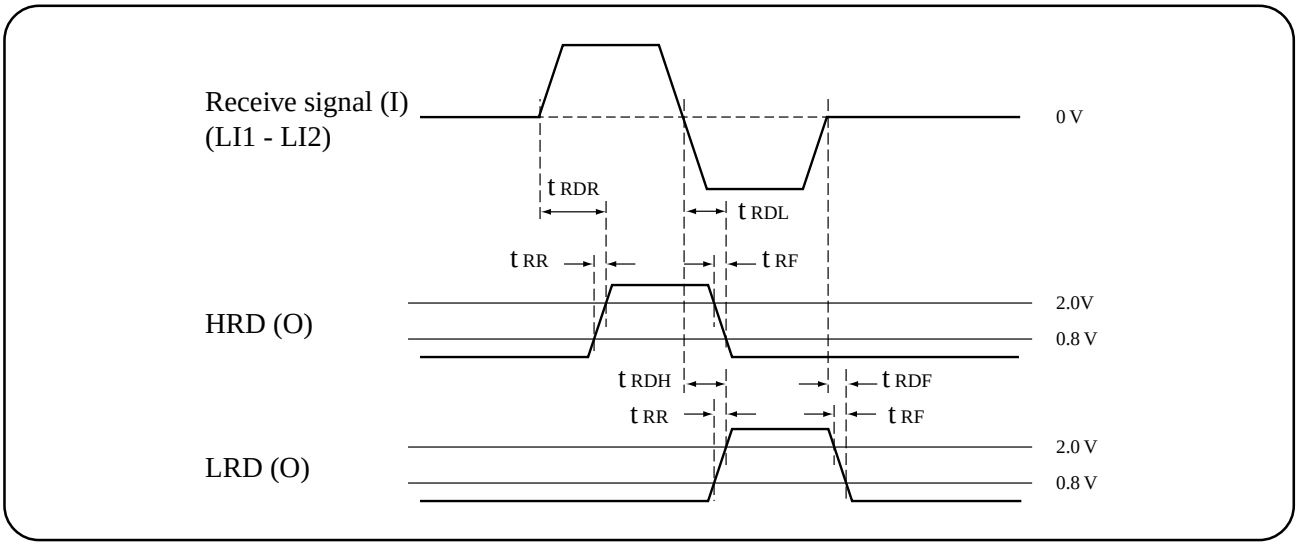


Figure 2 Receive Timing

■ T Reference Point Transmit Characteristic (TE mode)

(V_{DD} = 5.0 V, T_{op} = -20 ~ 70 °C, C_L = 50 pF)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Units
HTD, LTD Pulse Period	t_{SW}		4.95		5.45	µs
HTD, LTD Pulse Gap	t_{GAP}		0		260	ns
HTD, LTD Rise Time	t_{SR}				260	ns
HTD, LTD Fall Time	t_{SF}				30	ns
Transmit Signal Delay Time	t_{SRL}	Note 1	0		490	ns
	t_{SRH}	Note 1	490		1010	ns
	t_{SFH}	Note 1	0		165	ns
	t_{SFL}	Note 1	165		685	ns
Zero Cross Delay Time	t_{SDZ}	Note 1	490		1010	ns

Note 1 Measuring with R_L voltage drop as shown in Figure 4.

Note 2 Figure 3 shows the timing when TDP = “H”. When TDP = “L”, the output signal polarity from HRD and LRD pins are inverted.

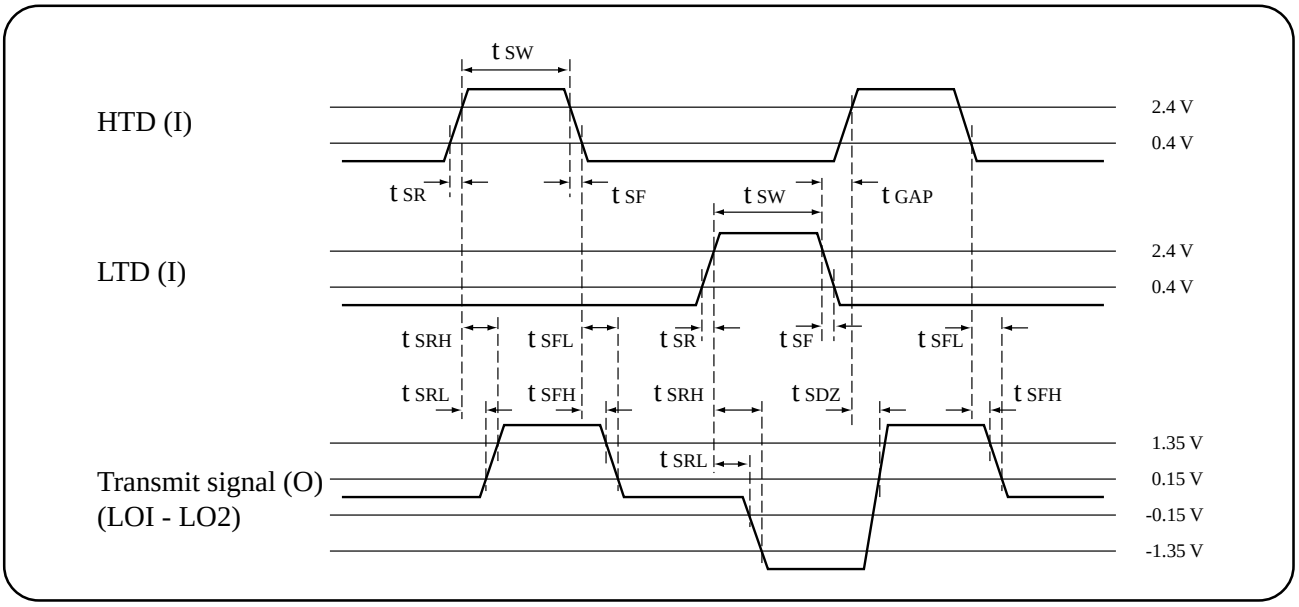


Figure 3 Transmit Timing

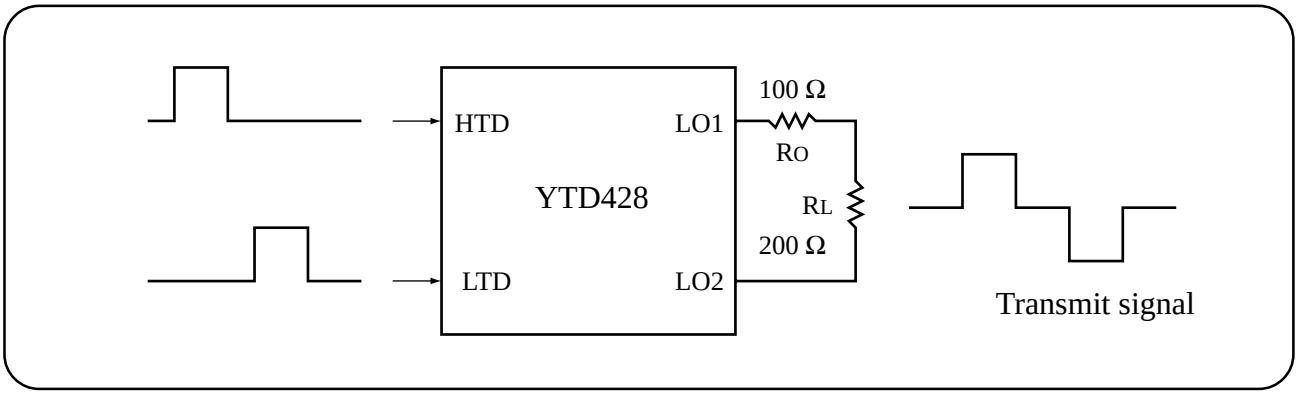


Figure 4 Transmit Block Test Circuit

■ Driver, Receiver I/O Impedance

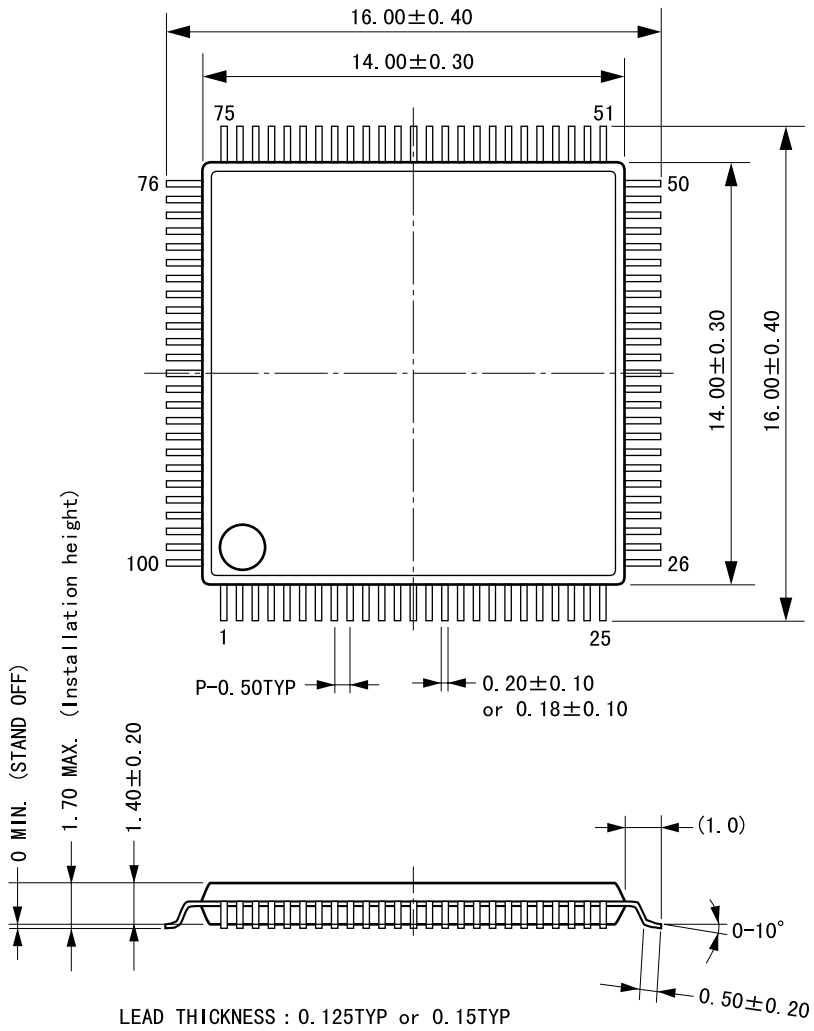
Parameters	Symbol	Condition	Min.	Typ.	Max.	Units
Receiver Input Impedance	Z_{LI}	LI1 - LI2	50			kΩ
Driver Ouput Impedance	Z_{LO1}	LO1 - LO2 (Note1)	50			kΩ
Driver Ouput Impedance	Z_{LO0}	LO1 - LO2 (Note2)		15		Ω

Note 1 When no pulse is output.

Note 2 When pulse is output.

PIN DESCRIPTIONS

C-PK100SP-1



(UNIT) : mm (millimeters)

The shape of the molded corner may slightly different from the shape in this diagram.

The figure in the parenthesis ( ) should be used as a reference.
Plastic body dimensions do not include burr of resin.
UNIT: mm

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