YAMAHA

YSS944/943/940

ADAMB

Advanced Digital Audio Multi channel decode processor

■ Outline

The YSS944 (ADAMB-f)/YSS943 (ADAMB-b)/YSS940 (ADAMB-nd) is an audio decoding digital signal processor that integrates onto a single chip the various digital signal processing functions required for AV amplifiers, etc. It includes an advanced 32-bit floating-point DSP and is able to decode a variety of audio formats.

[Note]

- The contents described in this manual are implemented by downloading boot firmware.
  For detailed information about the boot firmware, please contact YAMAHA.
- The YSS943 cannot execute DTS-ES and DTS Neo:6 decoding.
- The YSS940 cannot execute any decoding related to DTS (DTS, DTS-ES, DTS 96/24, and DTS Neo:6).

■ Features

- Supports various types of decoding up to 7.1 channels (5.1/6.1/7.1 channels selectable).
- 5.1-channel decoding of Dolby Digital (AC-3), DTS, AAC.
- 6.1-channel decoding of Dolby Digital EX, DTS-ES.
- DTS 96/24 decoding and audio interface clock division/switching functions.
- Dolby Pro Logic IIx and DTS Neo:6 decoding
- Tone control and bass management functions
- Function modification/expansion by downloading firmware to on-chip memory
- Lip-sync function that enables synchronization of voice and video with variable voice delay
- Supports sampling frequencies up to 192 kHz during PCM playback.
- 1/2 down sampling function when two PCM channels are played back
- Dolby Digital/DTS/AAC decode information output function (can be read by microprocessor)
- High-speed/high-accuracy operation by 32-bit floating-point DSP
  Operating frequency: 180 MHz (178.176 MHz)
  Data bus width: 32 bits (24-bit mantissa and 8-bit exponent)
  Multiplier/adder: 32 bits × 32 bits + 55 bits → 55 bits (47-bit mantissa and 8-bit exponent)
- No external memory needed (external memory is used when delay is increased.)
- Eight general I/O ports
- On-chip PLL for generation of high-speed internal operating clock
- Supply voltage: 1.2 V (core block) and 3.3 V (pin block)
- Low power consumption: about 210 mW (standard value during Dolby Digital decoding)
- Si-gate CMOS process
- Lead-free plating LQFP144 package (YSS944-VZ, YSS943-VZ, and YSS940-VZ)

[Note]

"Dolby," "Dolby Pro Logic IIx," and "AC-3" are trademarks of Dolby Laboratories.
"DTS," "DTS-ES," "DTS 96/24," and "DTS Neo:6" are trademarks of Digital Theater Systems, Inc.

■ Applications

- AV amplifiers for home theaters
- Car audio systems

YAMAHA CORPORATION

YSS944/943/940 CATALOG
CATALOG No.: LSI-4SS944A31
2005.6

YSS944/943/940 functional comparison

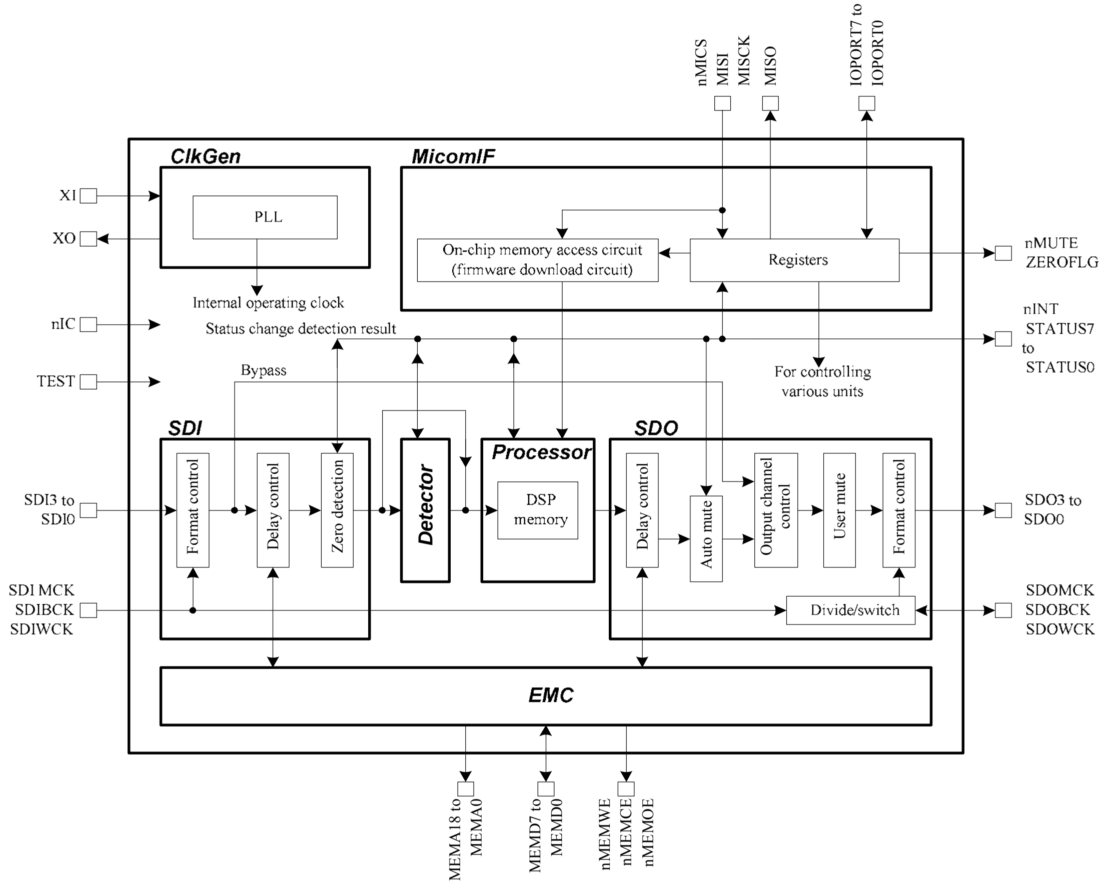
Decoder functional comparison

function \ devise	YSS944	YSS943	YSS940
Dolby Digital	YES	YES	YES
Dolby Digital EX	YES	YES	YES
Dolby Pro Logic IIx	YES	YES	YES
AAC	YES	YES	YES
DTS	YES	YES	NO
DTS 96/24	YES	YES	NO
DTS-ES	YES	NO	NO
DTS Neo:6	YES	NO	NO

YSS944/943/940 common functions

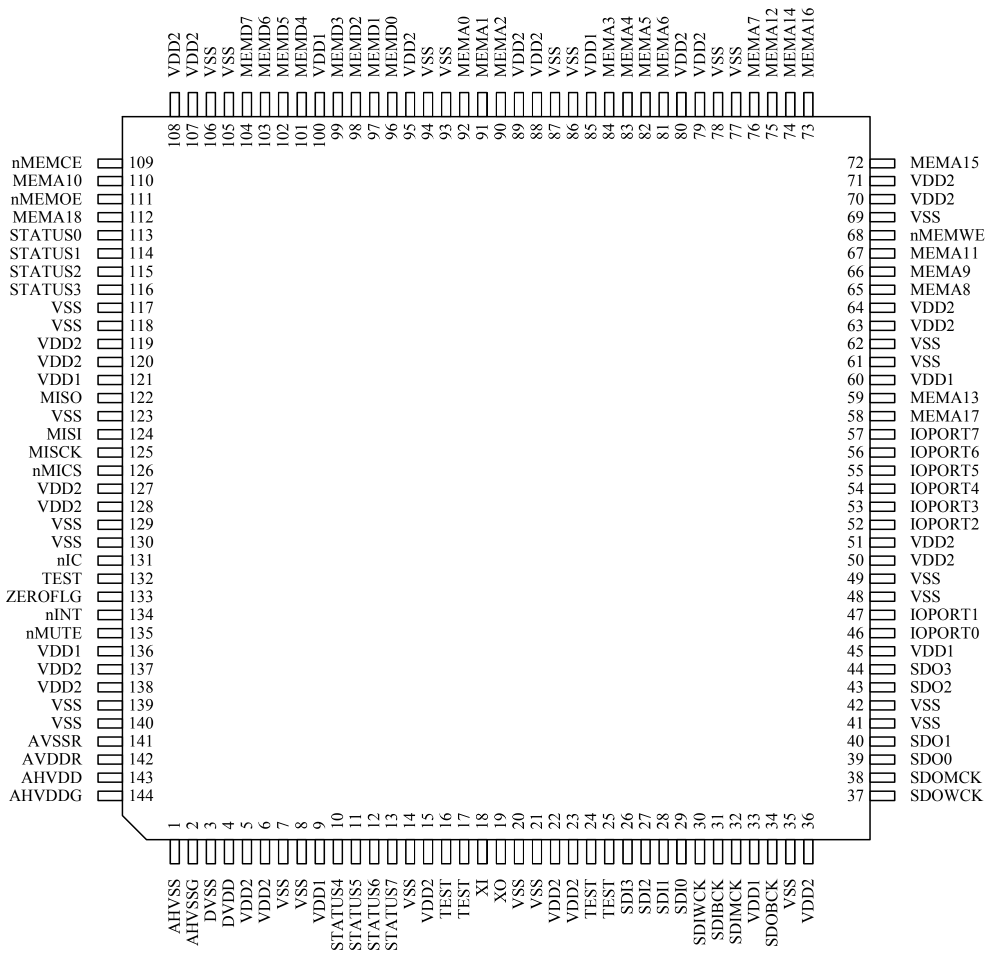
Input channel selection
Volume adjustment
Tone Control
Bass Management
User mute
Auto mute
Input delay
Output delay
Stream detection
Noise generation
Impulse generation
General purpose I/O port

■ Block Diagram



Block Name	Function
ClkGen	This is the internal operating clock generation block. This block provides the PLL and supplies the clock to each block.
MicomIF	This is an interface block to connect to a microprocessor. This block controls access to the registers/memory in this LSI.
SDI	This is the audio interface block for DIR, ADC, etc. This block controls the input data format/delay, etc.
SDO	This is the audio interface block for DIT, DAC, etc. This block controls the output data format/delay, etc.
Detector	This is the stream detection block. This block detects the input data encoding format.
EMC	This is an interface block to read from and write to external memory. This block implements delay functions using external memory.
Processor	This is an operation processing block. This decoder includes a 32-bit floating-point DSP and memory (ROM or RAM). Various functions can be implemented. Function modification/expansion by downloading firmware is also supported.

■ Pin Configuration



< LQFP 144 TOP VIEW >

■ Pin Functions

Type	Pin No.	Pin Name	I/O Note 1)	Function
Power supply	9	VDD1	-	Power supply pins for pin block (Typ. 3.3 V).
	33			
	45			
	60			
	85			
	100			
	121			
	136			
	5	VDD2	-	Power supply pins for core block (Typ. 1.2 V).
	6			
	15			
	22			
	23			
	36			
	50			
	51			
	63			
	64			
	70			
	71			
	79			
	80			
	88			
	89			
	95			
	107			
	108			
	119			
	120			
	127			
	128			
	137			
	138			
	142	AVDDR	-	Power supply pin 1 for PLL analog block (Typ. 3.3 V). Be sure to insert a 0.1 μF capacitor between the AVDDR and AVSSR pins.
	143	AHVDD	-	Power supply pin 2 for PLL analog block (Typ. 3.3 V). Be sure to insert a 0.1 μF capacitor between the AHVDD and AHVSS pins.
	144	AHVDDG	-	Power supply pin 3 for PLL analog block (Typ. 3.3 V). Be sure to insert a 0.1 μF capacitor between the AHVDDG and AHVSSG pins.
	4	DVDD	-	Power supply pin for PLL digital block (Typ. 1.2 V). Be sure to insert a 0.1 μF capacitor between the DVDD and DVSS pins.
	7	VSS	-	Ground pins
	8			
	14			
	20			
	21			
	35			
	41			
	42			
	48			
	49			

Type	Pin No.	Pin Name	I/O **Note 1)**	Function
	61			
	62			
	69			
	77			
	78			
	86			
	87			
	93			
	94			
	105			
	106			
	117			
	118			
	123			
	129			
	130			
	139			
	140			
	1	AHVSS		Ground pin 2 for PLL analog block. Be sure to insert a 0.1 μF capacitor between the AHVDD and AHVSS pins.
	2	AHVSSG		Ground pin 3 for PLL analog block. Be sure to insert a 0.1 μF capacitor between the AHVDDG and AHVSSG pins.
	3	DVSS		Ground pin for PLL digital block. Be sure to insert a 0.1 μF capacitor between the DVDD and DVSS pins.
	141	AVSSR		Ground pin 1 for PLL analog block. Be sure to insert a 0.1 μF capacitor between the AVDDR and AVSSR pins.
Initial clear	131	nIC	Is	Hardware reset input pin The LSI is initialized when this pin is at low level.
Clock	18	XI	I	Clock input pin. Connect this pin as shown in the circuit example **Note 2)** of the 12.288 MHz crystal oscillator. If not connected to a crystal oscillator, input a 12.288 MHz clock to this pin.
	19	XO	O	This is the output pin for the crystal oscillator. Connect this pin as shown in the circuit example **Note 2)**. If not connected to a crystal oscillator and inputting directly to the XI pin, do not connect anything to this pin. Do not use this pin for any purpose other than clock oscillation.
Microprocessor interface	126	nMICS	Is	This is the microprocessor interface's chip select input pin. Input to the MISCK and MISI pins becomes valid when this pin is at low level.
	125	MISCK	Is	This is the microprocessor interface's clock input pin.
	124	MISI	I	This is the microprocessor interface's address read/write control and data input pin.
	122	MISO	Ot	This is the microprocessor interface's data output pin. Connect a pull-up resistor.
Audio interface	32	SDIMCK	Is	This is the master clock input pin for the audio interface's input side. The master clock is input from DIR, ADC, etc. The highest clock frequency that can be input is 25 MHz. (The clock rate is 512 fs when the input sampling frequency is 48 kHz or less, 256 fs when the frequency is 96 kHz, and 128 fs when the frequency is up to 192 kHz.)
	31	SDIBCK	Is	This is the bit clock I/O pin for the audio interface's input side.

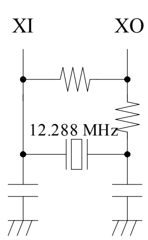
Type	Pin No.	Pin Name	I/O **Note 1)**	Function
				It inputs a 64 fs bit clock.
	30	SDIWCK	I	This is the word clock pin for the audio interface's input side.
	26	SDI3	I	This is the audio interface's serial data input pin 3. If this pin is not used, connect it to a ground.
	27	SDI2	I	This is the audio interface's serial data input pin 2. If this pin is not used, connect it to a ground.
	28	SDI1	I	This is the audio interface's serial data input pin 1. If this pin is not used, connect it to a ground.
	29	SDI0	I	This is the audio interface's serial data input pin 0. Connect digital audio data (various streams or PCM) via IEC60958 to this pin.
Audio interface	38	SDOMCK	Ot	This is the master clock output pin for the audio interface's output side. It outputs the master clock to DIT, DAC, etc. The highest clock frequency that can be output is 25 MHz.
	34	SDOBCK	Is/O	This is the bit clock I/O pin for the audio interface's output side. It inputs or outputs a 64 fs bit clock.
	37	SDOWCK	I/O	This is the word clock pin for the audio interface's output side.
	44	SDO3	O	This is the audio interface's serial data output pin 3.
	43	SDO2	O	This is the audio interface's serial data output pin 2.
	40	SDO1	O	This is the audio interface's serial data output pin 1.
	39	SDO0	O	This is the audio interface's serial data output pin 0.
External memory interface	112	MEMA18	O	These are external memory address output pins 18 to 0. If external memory is not used, these pins should be left unconnected.
	58	MEMA17		
	73	MEMA16		
	72	MEMA15		
	74	MEMA14		
	59	MEMA13		
	75	MEMA12		
	67	MEMA11		
	110	MEMA10		
	66	MEMA9		
	65	MEMA8		
	76	MEMA7		
	81	MEMA6		
	82	MEMA5		
	83	MEMA4		
	84	MEMA3		
	90	MEMA2		
	91	MEMA1		
	92	MEMA0		
	104	MEMD7	I/O	These are external memory data I/O pins 7 to 0. If external memory is not used, these pins should be left unconnected.
	103	MEMD6		
	102	MEMD5		
	101	MEMD4		
	99	MEMD3		
	98	MEMD2		
	97	MEMD1		
	96	MEMD0		
	109	nMEMCE	O	This is the external memory chip select output pin. If external memory is not used, this pin should be left unconnected.
	111	nMEMOE	O	This is the external memory output enable output pin. If external memory is not used, this pin should be left unconnected.
	68	nMEMWE	O	This is the external memory write enable output pin. If external memory is not used, this pin should be left unconnected.
Status ports	134	nINT	O	This is the interrupt request output pin.

Type	Pin No.	Pin Name	I/O **Note 1)**	Function
	135	nMUTE	O	This is the output pin during auto mute periods.
	133	ZEROFLG	O	This is the consecutive zero data input detection pin.
	13	STATUS7	O	These are status output pins 7 to 0. They are used to confirm firmware operations. Normally, they should be left unconnected.
	12	STATUS6		
	11	STATUS5		
	10	STATUS4		
	116	STATUS3		
	115	STATUS2		
	114	STATUS1		
	113	STATUS0		
General-purpose I/O ports	57	IOPORT7	I(+)/O	These are general I/O port pins 7 to 0. Their I/O status can be set via register settings.
	56	IOPORT6		
General-purpose I/O ports	55	IOPORT5	I(+)/O	These are general I/O port pins 7 to 0. Their I/O status can be set via register settings.
	54	IOPORT4		
	53	IOPORT3		
	52	IOPORT2		
	47	IOPORT1		
	46	IOPORT0		
Test	16	TEST	Is	Test pins Connect these pins to a ground.
	17			
	24			
	25			
	132			

Note 1) I/O symbols

- I: Input
- Is: Schmitt trigger input
- O: Output
- Ot: Tri-state output
- I/O: I/O
- I(+)/O: Pull-up during input, no pull-up during output

Note 2) Example of circuit connected to crystal oscillator



* The above resistor and capacitor vary depending on the crystal oscillator. Be sure to comply with the specifications of the crystal oscillator used.

■ Function Description

Functions of the YSS944/943/940 are follows.

(1) Main Decoder Functions

- Dolby Digital decoding
  - Firmware AC3 decoder is included.
  - Supports Annex D.
  - Supports sampling frequencies of 32 kHz, 44.1 kHz, and 48 kHz.
  - 5.1-channel decoding.

- DTS decoding
  - Firmware DTS decoder is included.
  - Supports DTS-ES Discrete 6.1 decoding. (Sampling frequencies of 44.1 kHz and 48 kHz.)
  - Supports DTS 96/24 decoding. (Output sampling frequencies of 88.2 kHz and 96 kHz.)

  [Note]
  - The YSS943 does not support DTS-ES Discrete 6.1 decoding.
  - The YSS940 does not support any DTS decoding.

- AAC decoding
  - Firmware AAC decoder is included.
  - Complies with ARIB digital broadcast standard.
  - Supports ADTS.
  - Supports LC profile.
  - Supported sampling frequencies are 32 kHz, 44.1 kHz, and 48 kHz.
  - 5.1-channel decoding

- PCM 2-channel input playback
  - Firmware PCM2 player is included.
  - Supported sampling frequencies are 32 kHz, 44.1 kHz, 48 kHz, 64 kHz, 88.2 kHz, 96 kHz, 128 kHz, 176.4 kHz, and 192 kHz.
  - Supports 24-bit word length.
  - De-emphasis function.
  - Input DC cutoff function.
  - 1/2 down sampling function.

- PCM 6-/7-/8-channel input playback
  - Firmware PCM8 player is included.
  - Supported sampling frequencies are 32 kHz, 44.1 kHz, 48 kHz, 64 kHz, 88.2 kHz, 96 kHz, 128 kHz, 176.4 kHz, and 192 kHz.
  - Supports 24-bit word length.
  - De-emphasis function.
  - Input DC cutoff function.
  - Audio data input channel control function.

(2) Post Decoder Functions

The following post-decoder function can be applied to the results of main decoder described above.

- Dolby Pro Logic IIx decoding
  - Firmware PL2 decoder is included.
  - Expands to up to 7 channels from 2 channels of L and R.
  - Expands to up to 4 channel from 2 channels of LS and RS (supports Dolby Digital EX with the combination of Dolby Digital decoding function)
  - Supported sampling frequencies are 32 kHz, 44.1 kHz, 48 kHz, 64 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, and 192 kHz.

- DTS Neo:6 decoding
  - Firmware Neo:6 decoder is included.
  - Expands to up to 6 channels from 2 channels of L and R.

- Expands to 3 channels from 2 channels of LS and RS (supports ES Matrix processing when combined with DTS decoding function).
- Supported sampling frequencies are 32 kHz, 44.1 kHz, 48 kHz, 64 kHz, 88.2 kHz, and 96 kHz.

[Note]
- The YSS943 and YSS940 do not support DTS Neo:6 decoding.

(3) Post Processor Functions

The following post-processing function can be applied to the results of main decoder or post decoder.

- Post-processing input channel selection
  - Firmware Switcher is included.
  - Supports 8 channels.

- Tone control
  - Firmware Tone controller is included.
  - Adjustable bass and treble for left and right channels
  - Supported sampling frequencies are 32 kHz, 44.1 kHz, 48 kHz, 64 kHz, 88.2 kHz, 96 kHz, 128 kHz, 176.4 kHz, and 192 kHz.

- Bass Management
  - Firmware Bass manager is included.
  - Characteristics can be changed by changing the coefficient.
  - Up to 7.1-channel input/output.
  - Supported sampling frequencies are 32 kHz, 44.1 kHz, 48 kHz, 64 kHz, 88.2 kHz, 96 kHz, 128 kHz, 176.4 kHz, and 192 kHz.

- Volume adjustment
  - Firmware Scaler is included.
  - Adjustable master volume (setting range: -127 dB to +31 dB, in 1 dB units).
  - Adjustable volume for up to eight channels ($-\infty$ dB to +12 dB, phase inversion enabled).

(4) Generator Functions

- Noise generation
  - Firmware noise generator is included.
  - Enables generation of pink noise ("shaped noise" in the Dolby standard) and white noise.
  - Supported sampling frequencies are 32 kHz, 44.1 kHz, and 48 kHz.

- Impulse generation
  - Firmware impulse generator is included.
  - Impulses can be generated.
  - Supported sampling frequencies are 32 kHz, 44.1 kHz, and 48 kHz.

(5) Other Functions

- Microprocessor interface
  - This is a four-wire serial interface.
  - Enables register access and on-chip memory access (firmware download).

- Firmware download
  - Instruction code from the microprocessor to this LSI and coefficient data can be downloaded.
  - The amount of 6-/7-/8-channel output delay can be changed.
  - The filter characteristics of the bass management function can be changed.
  - Functions can be expanded for future use.

[Note]
- The boot firmware must be downloaded at initialization.

- Audio interface
  - Master clock, bit clock, word clock, and four serial data (8ch) for input and output are provided respectively.
  - Various audio interface formats are supported.
  - The bit clock rate is fixed to 64 fs.
  - Supported sampling frequencies are 32 kHz, 44.1 kHz, 48 kHz, 64 kHz, 88.2 kHz, 96 kHz, 128 kHz, 176.4 kHz, and 192 kHz.
  - The bit clock and word clock on the output side have switchable input/output, and can therefore be used as either master or slave.
  - A clock divider/switching function is included to enable adjustment of the input/output sampling frequency for DTS 96/24, etc.

- Audio data output channel control
  - Audio output data can be output to any of the channels for the SDO3 to SDO0 pins.

- Bypass
  - Output of SDI data to SDO can bypass the internal core logic.

- User mute
  - Output channels can be muted via the microprocessor interface.

- External memory interface
  - Up to 4 Mb of SRAM can be connected for input delay and/or output delay.
  - Access time can be adjusted via register settings.

- Input delay (lip sync)
  - Input delay for adjusting synchronization between video and audio can be implemented when using external memory.

- Output delay
  - 3-/4-/5-/6-/7-/8-channel output delay with an output sampling frequency of up to 192 kHz can be implemented without using external memory (some exceptions).
  - 3-/4-/5-/6-/7-/8-channel output delay with an output sampling frequency of up to 96 kHz can be implemented using external memory.

- Stream detection
  - Encoding format detection
  - Zero detection
  - Input sampling frequency detection

- Auto mute
  - All channels are muted automatically by detection of noise generation factor.

- Status ports
  - Consecutive-zero data input detection: 1 pin.
  - Auto mute period output: 1 pin.
  - Interrupt request output: 1 pin.

- General purpose I/O port
  - 8 general purpose I/O ports are available.
  - Input and output mode can be switched by register setting.

- Internal operating clock generation
  - Generates the high-speed internal operating clock by on-chip PLL.

- Power-up/power-down
  - Enables power-up/power-down control of the LSI via register settings.

■ Microprocessor Interface

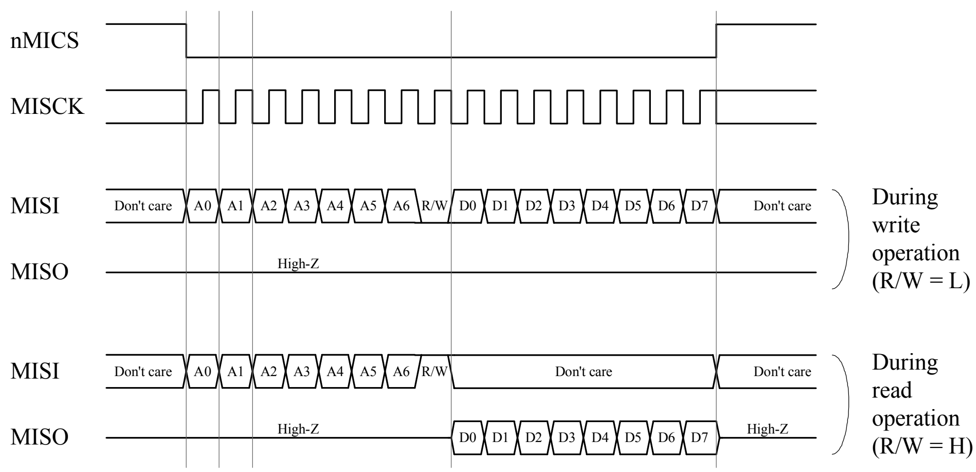
External microprocessor or similar devices use this microprocessor interface (4-wire serial interface) to perform the following tasks.

- Access to registers
- Firmware download to on-chip memory

(1) Register access

Registers are accessed in 16-bit units via the microprocessor interface. MISI is used to specify the register's address (7 bits: A6 to A0) and the read/write option (1 bit:R/W). During a write operation (R/W=L), data (8 bits: D7 to D0) is input to MISI and during a read operation (R/W=H) 8-bit data is output from the MISO pin. The data to be written is stored in the register at the rising edge of MISCK during the last data bit (D7 in figure).

The microprocessor interface's sequence when accessing registers is shown below.



[Note]

- MISO is in output mode only when nMICS is at low level and during the data (8 bits) output timing. Otherwise, it is in high impedance (High-Z) mode and MISCK, MISI, and MISO can be shared for devices that have a similar interface.
- Registers can be accessed continuously while nMICS remains at low level. There is no need to repeatedly set nMICS to high level.
- Certain register settings enable nMICS to be shared by multiple LSIs.
- Access to on-chip memory (firmware download) is performed by combining with control of writing to a register
- Operation during a hardware reset (when nIC is at low level):
  During a hardware reset, the microprocessor interface does not function. Also, MISO is fixed at high impedance (High-Z). When nIC is at low level, nMICS should be initialized to high level.
- Interruption of access:
  Access can be interrupted by setting nMICS to high level. The write operation prior to the 16th rising edge of MISCK (MISI's D7 data capture clock) described above becomes invalid. The MISO pin is set to high impedance (High-Z).

(2) On-chip memory access (firmware download)

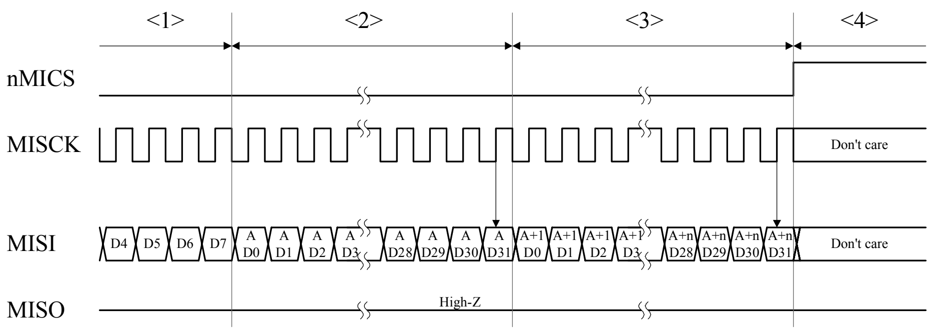
Access to on-chip memory is performed in 32-bit units via the microprocessor interface. Also, on-chip memory access can be performed concurrently with register access. The two firmware downloading methods prepared for this LSI are explained below.

(a) Burst transfer mode

When the IA carrier (PRGMOD[1:0] = 11) is used, instruction code/coefficient data firmware can be downloaded in this mode. By using this mode, a large amount of data can be downloaded at high speeds when initialization is executed or when the sampling frequency is changed. The features of the burst transfer mode are as follows.

- During the transfer period, decoding is aborted and data is transferred at high speeds. Muting is automatically effected during the transfer period.
- Data transferred from the microprocessor can be received without handshaking.
- Both instruction code firmware and coefficient data firmware can be downloaded.

The microprocessor interface’s sequence in firmware downloading burst transfer mode is shown below.



[Access steps and statuses]

<1> Register setting:

The microprocessor interface function change for the on-chip memory access start address (A in figure) and on-chip memory access is set by register as shown below.

- Set the instruction code firmware download mode (IACNFG = 1)
- Change the firmware program mode to IA carrier (PRGMOD[1:0] = 11).
- Set the on-chip memory access start address IAA[20:0].
- Change the function of the microprocessor interface pin from register access to on-chip memory access (IA = 1).
  Once this setting is made, the microprocessor interface functions in firmware downloading burst transfer mode until the nMICS pin is set to high level.

<2> Start firmware download:

- The nMICS pin is fixed at low level.
- Data is transferred LSB first, in 32-bit units.
- Data is written to on-chip memory when the rising edge of MISCK occurs for the 32nd bit of data (D31 in the figure).

<3> Continuation and termination of firmware download:

- Each time 32 bits of data are written, IAA[20:0] is automatically incremented. Accordingly, when writing to consecutive addresses, only the data is transferred.
- When nMICS changes from low level to high level, firmware download ends and the microprocessor interface returns to accessing registers.
- When accessing non-consecutive on-chip memory addresses or when resuming firmware downloading after an access interruption, be sure to set IAA[20:0] as described in <1> above.

<4> When this LSI has not been selected:

<5> Register setting:

After completing a firmware download, perform the following processing.

- Set the instruction code firmware execution mode (IACNFG = 0).
- Report the existence of boot firmware to this LSI (DL = 1).
- Change the firmware program mode PRGMOD[1:0] from “IA carrier” to another mode.

[Note]

Interruption of burst transfer:

- Burst transfer can be interrupted by setting nMICS to high level.
- The write operation becomes invalid when the rising edge of MISCK occurs for the 32nd bit of data (D31 in the figure).
- The MISO pin is set to high impedance (High-Z).

(b) Runtime transfer mode

When the main decoder, noise generator, or impulse generator is used (PRGMOD[1:0] = 00, 01, or 10), the coefficient data firmware can be downloaded in this mode. By using this mode, coefficients such as the amount of 6-/7-/8-channel output delay can be changed without disruption of sound. The features of the runtime transfer mode are as follows.

- Transfer is executed while decoding continues. Muting is not automatically effected during the transfer period.
- One word is transferred at a time while the device is handshaking with the microprocessor.
- Up to 32 words of transfer data are buffered and written all at once to the on-chip memory.
- Downloading coefficient firmware is supported.

[Access steps and statuses]

<1> Start firmware download:
Set the runtime transfer mode and transfer start address by using registers.
- Initialize the handshake-related registers (RDLFLG = RDLEND = RDLCNT[4:0] = 0).
- Set the runtime transfer mode (RDLMODE = 1).
- Set the on-chip memory access start address IAA[20:0].

<2> Execute firmware download:
One word (32 bits) is downloaded at a time.
- Change the microprocessor interface pin function from register access to on-chip memory access (IA = 1). IAA[20:16] in this byte is valid only when it is set for the first time (for the second and subsequent time, any value may be written).
- Fix nMICS to L.
- Transfer data with the LSB first and in 32-bit units.
- Raise nMICS from L to H.
- Read RDLCNT[4:0].
- Specify starting data transfer (RDLFLG = 1).
  Set RDLEND to 1 if the transferred data is the last word in successive address transfer; otherwise, clear RDLEND to 0. At this time, write back the value that is read, to RDLCNT[4:0].

<3> Continuation of firmware download (if RDLEND = 0 in <2>):
- Confirm the termination of data transfer (RDLFLG = 0).
- Return to step <2> above.

<4> Termination of firmware download (if RDLEND = 1 in <2>):
- Confirm the termination of data transfer/successive address transfer (RDLFLG = RDLEND = 0).
- Cancel the runtime transfer mode (RDLMODE = 0).

[Note]

- Runtime transfer can be stopped by making nMICS high and clearing RDLMODE to 0.
- Start from <1> if non-successive addresses are transferred or when execution is started again after stopping downloading.
- When the transfer data is captured in the internal buffer, the value of RDLFLG automatically changes from 1 to 0.
  If RDLEND = 0 at this time, the transfer data is written only to the internal buffer and not to the transfer destination address.
  If RDLEND = 1, the transfer data, along with the data in the internal buffer, is sequentially written from the transfer start address. If data of two or more words, such as filter coefficients, are changed at the same time, transfer them as successive address data.
- Transfer successive address data in the order of the address data that has been incremented starting from the data of the transfer start address.
- Up to 32 words can be transferred as successive address data.
  If more than 32 words are transferred to successive addresses, start the next transfer from <1> after the first 32 words have been transferred.
- The time until RDLFLG is automatically cleared to 0 after it has been set to 1 varies from 0 to 4 ms.
- Unlike the burst transfer mode, it is not necessary to change IACNFG and PRGMOD[1:0].

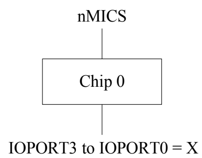
(3) Microprocessor interface connection example

When microprocessor interface pins are shared by several LSIs, the target LSI can be selected by either of the following two methods.

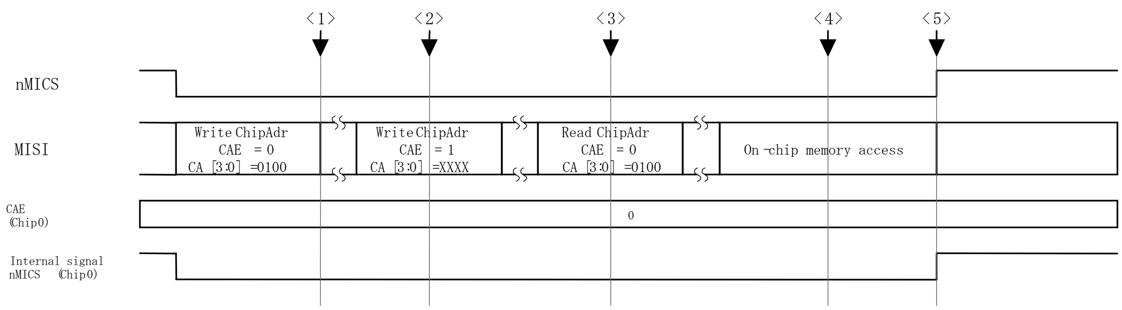
- Design nMICS pins dedicated to specific LSIs.
- When nMICS pins are shared by several LSIs, use the ChipAdr register to select the target LSI.

These two examples are described below.

(a) Microprocessor interface connection example 1 (single LSI)



Default value after hardware reset is CAE = 0, so there is no need to write to ChipAdr.



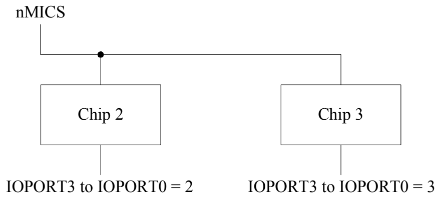
<1> A write operation to ChipAdr as the register access immediately after the falling edge of nMICS is valid.
In the above figure, an example of writing when CAE = 0 and CA[3:0] = 4 is illustrated.

<2> A write operation to ChipAdr as the register access immediately after the falling edge of nMICS is invalid.

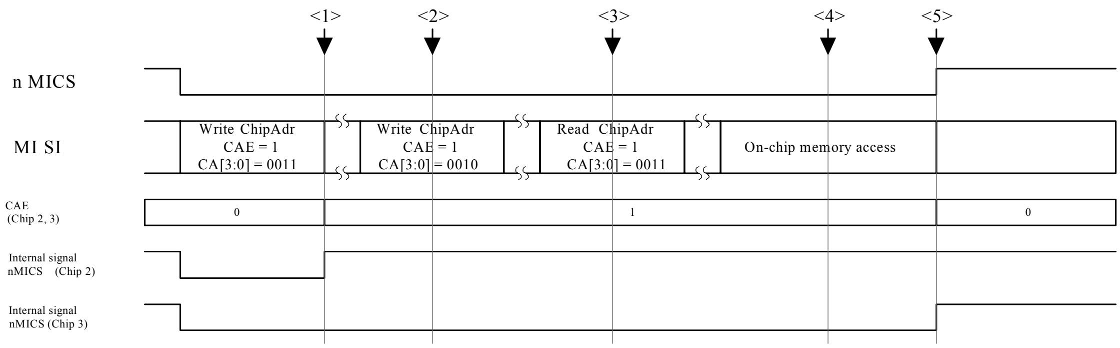
<3> ChipAdr can be read at any time.
In this case, the write operation (<2>) is disabled, so the write results from <1> are read.

<4> Registers cannot be accessed while accessing on-chip memory.

(b) Microprocessor interface connection example 2 (multiple LSIs)



When multiple LSIs are connected such as on the left, or when the device has a similar interface, access is performed using the register byte ChipAdr (CAE, CA[3:0]).



<1> A write operation to ChipAdr as the register access immediately after the falling edge of nMICS is valid to for all LSIs (chips 2 and 3 in this example) that share the nMICS pin. In this case, CAE = 1 and CA[3:0] = 3, so only the access only for chip 3 is valid.

<2> A write operation to ChipAdr not immediately after the falling edge of nMICS is also invalid for chip 3.
(Chip 2 is not affected by the register access itself.)

<3> The ChipAdr register can be read at any time. In this case, the write results from <1> are read from chip 3.
(Chip 2 is not affected by the register access itself.)

<4> During on-chip memory access, register access for chip 3 is invalid.
(Chip 2 is not affected by on-chip memory access.)

<5> CAE of all LSIs becomes zero at the rising edge of nMICS.

[Note]
The timing by which the chip selection is confirmed in <1> is determined by the value of IOPORT3 to IOPORT0 either at:

- the register access immediately after falling edge of nMICS, or
- a write operation to ChipAdr.

Once the chip selection is confirmed, the current value is retained until the next rising edge of nMICS. Accordingly, even if the selected chip's own IOPORT3 to IOPORT0 values change, the chip does not become deselected immediately.

When nMICS is shared by multiple chips:

- CAE = 0 at the register access immediately after the falling edge of nMICS or CAE = 1 is not written.
- CAE = 1 at the register access immediately after the falling edge of nMICS, but the values of IOPORT3 to IOPORT0 are the same for multiple LSIs.

In the above cases, the multiple LSIs that share nMICS become the selected devices. In such cases, multiple LSIs can be written to at once, but note with caution that a conflict can occur with the MISO output when they are read.

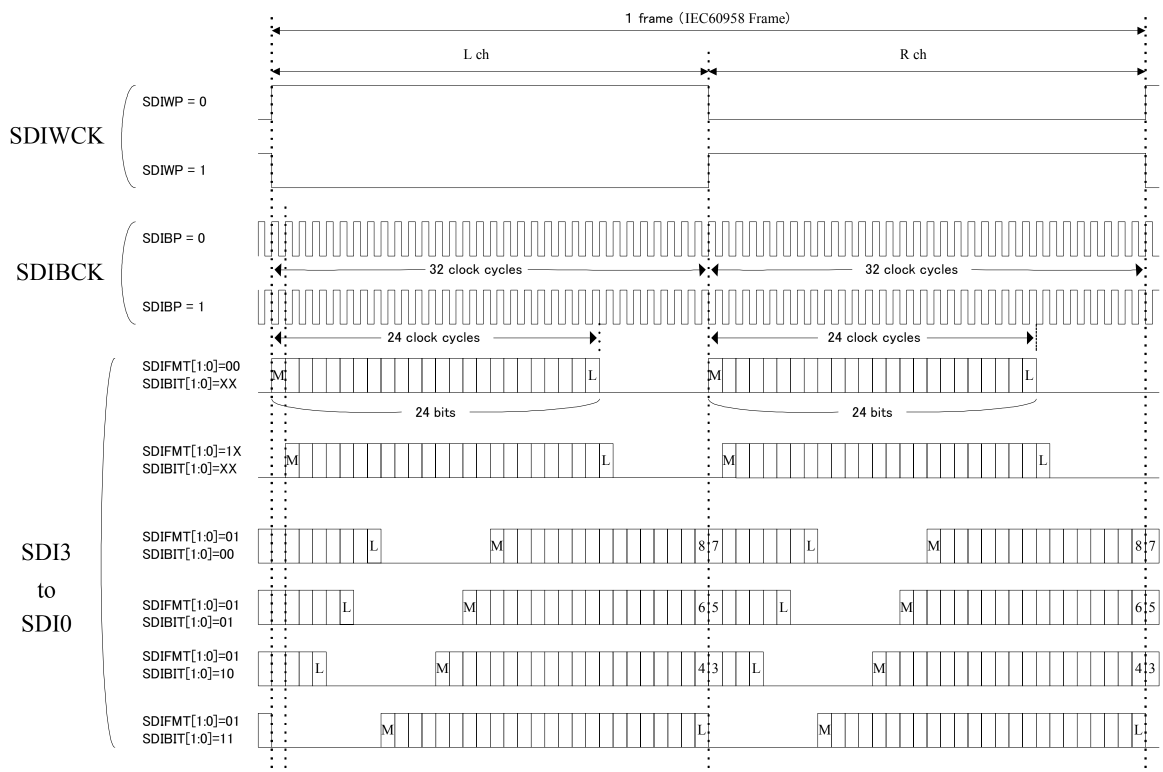
■ Audio Interface

Input and output of digital audio data is performed via two interfaces:

- SDI (serial data input) interface
- SDO (serial data output) interface

(1) SDI interface format

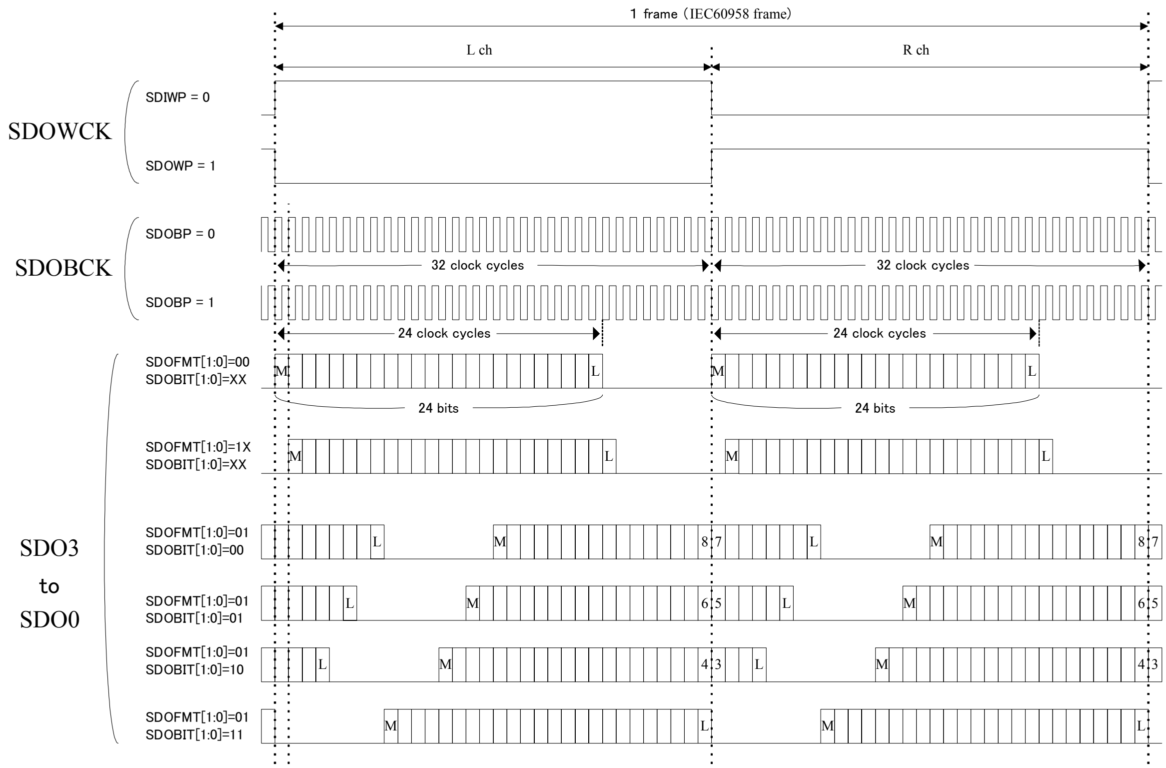
The following serial data input format is supported via register settings.
Regardless of the register setting, the input signals for SDI3 to SDI0 are always handled as fixed-point 24-bit data.



M : MSB DATA   L : LSB DATA

(2) SDO interface format

The following serial data output format is supported via register settings.
Regardless of the register setting, the output signals for SDO3 to SDO0 are always handled as fixed-point 24-bit data.



M : MSB DATA   L : LSB DATA

Interrupt Requests

This LSI's status changes by any of the following five factors are externally reported as interrupt requests via the nINT pin.

<1> When mute status is set by the auto mute function
<2> When mute status is canceled by the auto mute function
<3> When decode information is changed
<4> When the main decoder is changed (MAINMOD[7:0] are changed)
<5> When the post decoder is changed (POSTMOD[7:0] are changed)

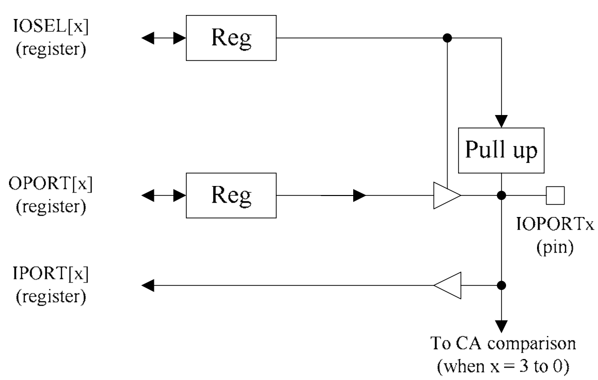
IM register can enable or disable generation of the interrupt of each interrupt factor, and IR register can check generation of and clear an interrupt factor. However, generation of an interrupt factor is not affected by the IM register setting. Changes in the status of this LSI are always detected and reported to IR register.

General Purpose I/O Ports

The general-purpose I/O ports IOPORT7 to IOPORT0 have the following functions. The functions are switched by IOSEL[7:0].

<1> Input port:
Pin statuses are read via IPORT[7:0].
<2> Output port:
Setting values in OPORT[7:0] are output from pins.
<3> CA comparison port:
IOPORT3 to IOPORT0 function as a CA comparison port that is used when nMICS is shared by several LSIs.

A functional outline of IOPORT7 to IOPORT0 is shown below.



■ Register List

The YSS422/421 is controlled by accessing the following registers via the microcomputer interface (nMICS, MISCK, MISI, and MISO).

Address	Byte Name	R/W	Default Value	D7	D6	D5	D4	D3	D2	D1	D0
0x00	ChipAdr	R/W	0x00	CAE	0	0	0	CA[3:0]			
0x01	IOsel	R/W	0x00	IOSEL[7:0]							
0x02	IPort	R	Undefined	IPORT[7:0]							
0x03	OPort	R/W	0x00	OPORT[7:0]							
0x04	Mute	R/W	0x00	nMUTE_3R	nMUTE_3L	nMUTE_2R	nMUTE_2L	nMUTE_1R	nMUTE_1L	nMUTE_0R	nMUTE_0L
0x05	SDIOClk	R/W	0x00	MCKOUT	0	MSEL[1:0]		WBCKOUT	WBSEL[2:0]		
0x06	SDI	R/W	0x00	SDISEL[1:0]		SDIFMT[1:0]		SDIBIT[1:0]		SDIWP	SDIBP
0x07	SDO	R/W	0x00	BYPASS	0	SDOFMT[1:0]		SDOBIT[1:0]		SDOWP	SDOBP
0x08	SDOsel0	R/W	0x10	0	SDOSEL_0R[2:0]			0	SDOSEL_0L[2:0]		
0x09	SDOsel1	R/W	0x32	0	SDOSEL_1R[2:0]			0	SDOSEL_1L[2:0]		
0x0A	SDOsel2	R/W	0x54	0	SDOSEL_2R[2:0]			0	SDOSEL_2L[2:0]		
0x0B	SDOsel3	R/W	0x76	0	SDOSEL_3R[2:0]			0	SDOSEL_3L[2:0]		
0x0C	EM0	R/W	0x00	EM_OEH[1:0]		EM_WEH[1:0]		EM_CYC[3:0]			
0x0D	EM1	R/W	0x00	EM_INCLR	0	0	EM_INSIZE[4:0]				
0x0E	EM2	R/W	0x00	EM_OUTCLR	0	0	EM_OUTSIZE[4:0]				
0x0F	Zero	R/W	0x00	ZERO[7:0]							
0x10	IA0	R/W	0x00	IA	0	0	IAA[20:16]				
0x11	IA1	R/W	0x00	IAA[15:8]							
0x12	IA2	R/W	0x00	IAA[7:0]							
0x13	IACnfg	R/W	0x00	IACNFG	0	0	0	0	0	0	0
0x14	IM	R/W	0x00	IMMUTE	IMUMUTE	IMBSCHG	IMMAINCHG	IMPOSTCHG	0	0	0
0x15	IR	R/W	0x00	IRMUTE	IRUMUTE	IRBSCHG	IRMAINCHG	IRPOSTCHG	0	0	0
0x16	State	R	0x00	nMUTE	0	0	0	IEC61937	DTSCD[1:0]		ZEROFLG
0x17	Pc0	R	0x00	PC[15:8]							
0x18	Pc1	R	0x00	PC[7:0]							
0x19	FsCnt	R	0x00	FSCNT[7:0]							
0x1A	MainMod	R	0x00	MAINMOD[7:0]							
0x1B	PostMod	R	0x00	POSTMOD[7:0]							
0x1C	Stream	R	0x00	STREAM[7:0]							
0x1D	PrgMod	R/W	0x00	PRGMOD[1:0]		0	DTSCDIGN	DSNIGN	DSNSEL[2:0]		
0x1E	Dly0	R/W	0x00	0	0	0	0	DELAY[11:8]			
0x1F	Dly1	R/W	0x00	DELAY[7:0]							
0x20	Download	R/W	0x00	RDLMODE	0	CHISEL[2:0]			CHCNFG[1:0]		DL
0x21	OutMode	R/W	0x00	VOLON	0	DUALMOD[1:0]		OUTMOD[3:0]			
0x22	NoiseMode	R/W	0x00	PNWN	0	0	0	0	0	NOISEFS[1:0]	
0x23	NoiseLevel	R/W	0x00	NOISELEV[7:0]							
0x24	SDly	R/W	0x00	0	0	0	SDELAY[4:0]				
0x25	CDly	R/W	0x00	0	0	0	0	0	CDELAY[2:0]		
0x26	BSDly	R/W	0x00	0	0	BSDELAY[5:0]					
0x27	Switch	R/W	0x00	RBOUTOFF	LFEOUTOFF	LBOUTOFF	COUTOFF	RSOUTOFF	LSOUTOFF	ROUTOFF	LOUTOFF
0x28	LVolume	R/W	0x00	LVOL[7:0]							
0x29	RVolume	R/W	0x00	RVOL[7:0]							
0x2A	LSVolume	R/W	0x00	LSVOL[7:0]							
0x2B	RSVolume	R/W	0x00	RSVOL[7:0]							
0x2C	CVolume	R/W	0x00	CVOL[7:0]							
0x2D	LSVolume	R/W	0x00	LBVOL[7:0]							
0x2E	LFEVolume	R/W	0x00	LFEVOL[7:0]							

0x2F	RBVolume	R/W	0x00	RBVOL[7:0]							
0x30	MasterVolume	R/W	0x00	MVOL[7:0]							
0x31	LScaleH	R/W	0x00	LSCALE[15:8]							
0x32	LScaleL	R/W	0x00	LSCALE[7:0]							
0x33	RScaleH	R/W	0x00	RSCALE[15:8]							
0x34	RScaleL	R/W	0x00	RSCALE[7:0]							
0x35	LSScaleH	R/W	0x00	LSSCALE[15:8]							
0x36	LSScaleL	R/W	0x00	LSSCALE[7:0]							
0x37	RSScaleH	R/W	0x00	RSSCALE[15:8]							
0x38	RSScaleL	R/W	0x00	RSSCALE[7:0]							
0x39	CScaleH	R/W	0x00	CSCALE[15:8]							
0x3A	CScaleL	R/W	0x00	CSCALE[7:0]							
0x3B	LBScaleH	R/W	0x00	LBSCALE[15:8]							
0x3C	LBScaleL	R/W	0x00	LBSCALE[7:0]							
0x3D	LFEScaleH	R/W	0x00	LFESCALE[15:8]							
0x3E	LFEScaleL	R/W	0x00	LFESCALE[7:0]							
0x3F	RBScaleH	R/W	0x00	RBSCALE[15:8]							
0x40	RBScaleL	R/W	0x00	RBSCALE[7:0]							
0x41	SimMode	R/W	0x00	ALLDELAY	DELAYOFF	0	0	0	0	0	0
0x42	TC	R/W	0x00	BASS[3:0]				TREBLE[3:0]			
0x43	BMMode	R/W	0x00	0	0	0	0	0	0	0	BMMODE
0x44	HDynrng	R/W	0x00	HDYNRNG[7:0]							
0x45	LDynrng	R/W	0x00	LDYNRNG[7:0]							
0x46	PCMMode0	R/W	0x00	PCMEMPON	PCMDLY	PCMDCCUTON	PCMIGN	PCMFS[3:0]			
0x47	PCMMode1	R/W	0x00	PCMDS	0	PCM20MOD[2:0]			0	0	0
0x48	AC3Mode0	R/W	0x00	AC3P11OFF	AC3DIALOFF	AC3DITHOFF	AC3CRCOFF	AC3KARAOKE	AC3STAUTO	AC3COMP[1:0]	
0x49	AC3Mode1	R/W	0x00	0	0	AC320MOD[2:0]			AC3S2MOD[2:0]		
0x4A	DTSMode0	R/W	0x00	DTSEXT[1:0]		DTSDITHOFF	0	0	0	DTSDIAL	DTSCOMP
0x4B	DTSMode1	R/W	0x00	0	0	DTS20MOD[2:0]			DTSS2MOD[2:0]		
0x4C	AACMode0	R/W	0x00	AACMIX	AACMIXSET	AACMIXLEV	AACCRCOFF	0	0	0	0
0x4D	AACMode1	R/W	0x00	0	0	AAC20MOD[2:0]			AACS2MOD[2:0]		
0x4E	Reserved	R/W	0x00	0	0	0	0	0	0	0	0
0x4F	Reserved	R/W	0x00	0	0	0	0	0	0	0	0
0x50	Reserved	R/W	0x00	0	0	0	0	0	0	0	0
0x51	PL2XMode0	R/W	0x00	PL2XDECMOD[1:0]		PL2XINVMAT	PL2XSPLIT	PL2XRSINV	PL2XAIBON	PL2XSRFIL[1:0]	
0x52	PL2XMode1	R/W	0x00	PL2XDIMCFG[3:0]				PL2XCWCFG[2:0]			0
0x53	Neo6Mode0	R/W	0x00	N6DECMOD	0	0	0	0	0	0	0
0x54	Neo6Mode1	R/W	0x00	N6CGAINON	N6CGAIN[6:0]						
0x55	Reserved	R/W	0x00	0	0	0	0	0	0	0	0
0x56	RunTime	R/W	0x00	RDLFLG	RDLEND	0	RDLCNT[4:0]				
0x57	Reserved	R/W	0x00	0	0	0	0	0	0	0	0
0x58	Bitstream0	R/W	0x00	Main decoder's decode information output							
0x59	Bitstream1	R/W	0x00	Main decoder's decode information output							
0x5A	Bitstream2	R/W	0x00	Main decoder's decode information output							
0x5B	Bitstream3	R/W	0x00	Main decoder's decode information output							
0x5C	Bitstream4	R/W	0x00	Main decoder's decode information output							
0x5D	Bitstream5	R/W	0x00	Main decoder's decode information output							
0x5E	Bitstream6	R/W	0x00	Main decoder's decode information output							
0x5F	Bitstream7	R/W	0x00	Main decoder's decode information output							
0x60	Bitstream8	R/W	0x00	Main decoder's decode information output							
0x61	Bitstream9	R/W	0x00	Main decoder's decode information output							
0x62	Bitstream10	R/W	0x00	Main decoder's decode information output							
0x63	Bitstream11	R/W	0x00	Main decoder's decode information output							
0x64	Bitstream12	R/W	0x00	Main decoder's decode information output							
0x65	Bitstream13	R/W	0x00	Main decoder's decode information output							

0x66	Bitstream14	R/W	0x00	Main decoder's decode information output							
0x67	Bitstream15	R/W	0x00	Main decoder's decode information output							
0x68	Bitstream16	R/W	0x00	Main decoder's decode information output							
0x69	Bitstream17	R/W	0x00	Main decoder's decode information output							
0x6A	Bitstream18	R/W	0x00	Main decoder's decode information output							
0x6B	Bitstream19	R/W	0x00	Main decoder's decode information output							
0x6C	Bitstream20	R/W	0x00	Main decoder's decode information output							
0x6D	Test			Access prohibited.							
0x6E	Test			Access prohibited.							
0x6F	Test			Access prohibited.							
0x70	Test			Access prohibited.							
0x71	Test			Access prohibited.							
0x72	Test			Access prohibited.							
0x73	Test			Access prohibited.							
0x74	Test			Access prohibited.							
0x75	Test			Access prohibited.							
0x76	Test			Access prohibited.							
0x77	Test			Access prohibited.							
0x78	Test			Access prohibited.							
0x79	Test			Access prohibited.							
0x7A	PLL0	R/W	0x1B	0	PLL_F[6:0]						
0x7B	PLL1	R/W	0x00	PLL_OD[1:0]		PLL_RDIV1	PLL_R[4:0]				
0x7C	nReset	R/W	0x00	nRESET	0	0	0	IC[3:0]			
0x7D	Power	R/W	0x80	PD[1:0]		0	0	0	0	UP	DOWN
0x7E	ADAMID	R	0x01 0x00	0	0	0	0	0	ADAM_ID[2:0]		
0x7F	DevID	R	0x03	DEV_ID = 0x03							

[Note]

Register addresses 0x6D to 0x79 comprise a test area. Writing of values to this area is prohibited and read values are undefined.

Access conditions for other addresses are shown below.

(Bold frame) indicates area that is accessible regardless of PD[1:0] value.

(Narrow frame) indicates area that is accessible only when PD[1:0] = 00. When PD[1:0] is not "00" values in this area are undefined when read or written.

0 (Shaded) indicates areas reserved for future expansion. Write zeros to these areas. Their output is undefined.

■ Electrical Characteristics

(1) Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit
Power supply voltage 1 (3.3 V)	VDD1 AVDDR AHVDD AHVDDG	-0.5	4.6	V
Power supply voltage 2 (1.2 V)	VDD2 DVDD	-0.5	1.68	V
Input voltage1 **Note 1)**	VI	-0.5	5.5	V
Input voltage2 **Note 2)**	V12	-0.5	4.6	V
Storage temperature	TSTG	-50	125	°C

Condition: All GND pins (VSS, AVSSR, AHVSS, AHVSSG, and DVSS) are 0 V.
Note 1) Applies to input pins other than the X1 pin.
Note 2) Applies to the X1 pin.

(2) Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage 1(3.3 V)	VDD1 AVDDR AHVDD AHVDDG	3.0	3.3	3.6	V
Power supply voltage 2(1.2 V)	VDD2 DVDD	1.14	1.2	1.26	V
Operating temperature	Top	-40	25	85	°C

Condition: All GND pins (VSS, AVSSR, AHVSS, AHVSSG, and DVSS) are 0 V.

(3) Current Consumption

Parameter	Condition	Min.	Typ.	Max.	Unit
Power consumption	**Notes 1 and 4)**		211	395	mW
3.3 V current consumption(normal operation mode)	**Notes 1, 2, and 4)**		13	21	mA
1.2 V current consumption(normal operation mode)	**Notes 1, 3, and 4)**		140	253	mA
3.3 V current consumption (power-down mode)	**Notes 1, 2, 5 and 6)**		35	90	µA
1.2 V current consumption (power-down mode)	**Notes 1, 3, 5, and 6)**		15	85	mA

Note 1) Typical values are typical under the recommended operating conditions. Maximum values are the maximum conditions under the recommended operating conditions.
Note 2) Total current of VDD1, AVDDR, AHVDD, and AHVDDG
Note 3) Total current of VDD2 and DVDD
Note 4) Typical value is at Dloby Digital. Maximum values are at PCM 2-chanel 192kHz+Dolby Pro Logic IIx+Bass Management.
Note 5) Value in power-down mode 3. XI input is at high level.
Note 6) The current consumption increases during power-down at higher temperatures.

(4) DC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High level input voltage (1)	V_{IH1}	XI pin	0.8VDD1		VDD1	V
Low level input voltage (1)	V_{IL1}	XI pin			0.2VDD1	V
High level input voltage (2)	V_{IH2}	Input pin other than XI **Note 1)**	2.2		5.25	V
Low level input voltage (2)	V_{IL2}	Input pin other than XI **Note 1)**			0.8	V
High level output voltage	V_{OH}	IOH = -1.0 mA, **Note 2)**	2.4			V
Low level output voltage	V_{OL}	IOL = 1.0 mA, **Note 2)**			0.4	V
High level output current	I_{OH}				-1.0	mA
Low level output current	I_{OL}				1.0	mA
Input leakage current	I_{LI}	Pin without pull-up resistor	-1		1	µA
Pull-up resistance	R_U		37		72	kΩ
Input pin's capacitance	C_I				7	pF

Note 1) All input pins other than XI are tolerant of 5 V.
Note 2) Applies to all output pins other than XO. No rating for the XO output voltage level.

(5) AC Characteristics

(a) Power up, Hardware Reset, and clock

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
1	nIC time 1	T_{IC1}	Figure 1) below	5			ms
2	nIC time 2	T_{IC2}	Figure 2) below	1			μs
3	XI clock frequency	f_{XIN}			12.288		MHz
4	XI clock duty	X_{DUTY}		40		60	%
5	Internal operating clock cycle	T_{CLK}	**Note 1)**		1000/178.176		ns
6	Power ON time	T_{V1V2}	**Note 2)**	0		1	s
			Note 3)	1		1	s

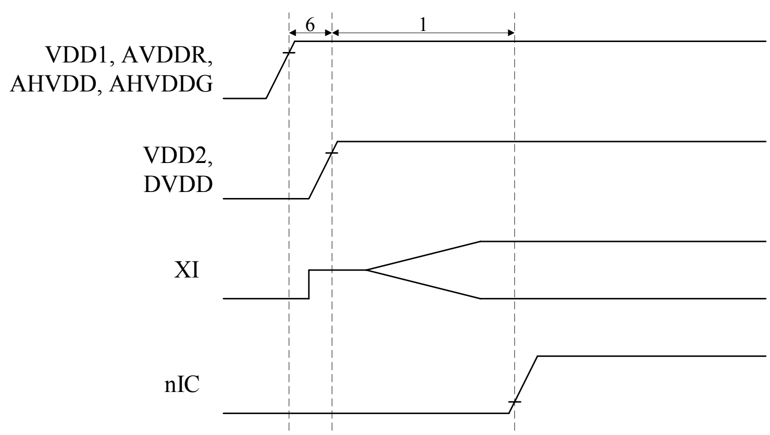
Note 1) When using recommended XI input and recommended PLL setting. The internal operating clock frequency is 178.176 MHz.

Note 2) When Shortcut key barrier diode is not connected
The 3.3 V power supply (VDD1, AVDDR, AHVDD, and AHVDDG) should be started before the 1.2 V power supply (VDD2 and DVDD).

Note 3) When Shortcut key barrier diode is connected
Insert a Shortcut key barrier diode with forward voltage of 0.4 V or less between the 3.3 V power supply (VDD1, AVDDR, AHVDD, and AHVDDG) and 1.2 V power supply (VDD2 and DVDD) (cathode is VDD1 and anode is VDD2).
The 3.3 V power supply and 1.2 V power supply can be started in either order.

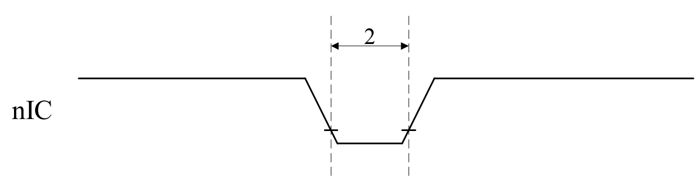
Note 4) The time interval of power ON or OFF between 3.3V power supply and 1.2V power supply must be within one second. Only one power keep on supplying, LSI would be damaged.

1) At power-on



- If a crystal oscillator is connected, this includes the time between power supply stabilization and oscillator stabilization.
- Turn on the power when nIC is at low level.

2) In normal operation mode

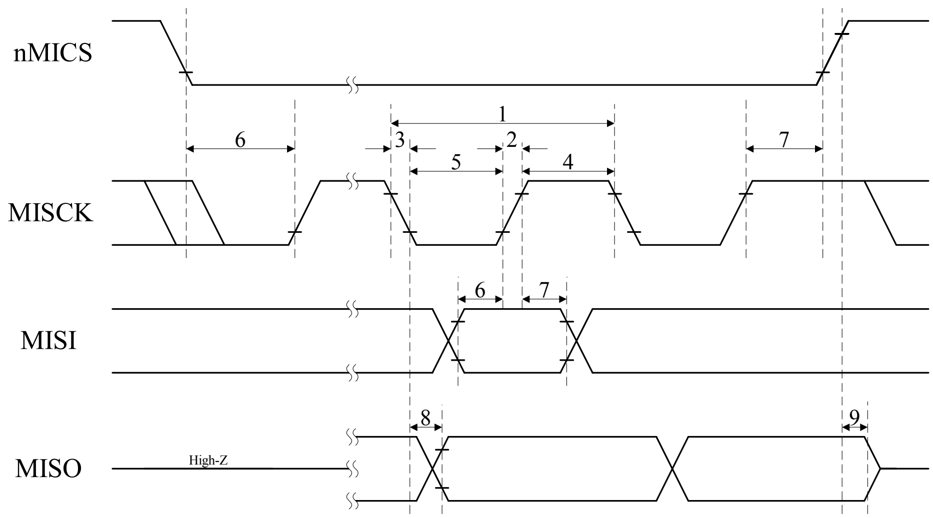


- The XI input and power supply must be stabilized.
- If XI oscillation has stopped during initialization in power-down mode, time is required to stabilize the oscillation.

(b)Microprocessor interface

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
1	MISCK cycle	tcc		160			ns
2	MISCK rise time	tcr				20	ns
3	MISCK fall time	tcf				20	ns
4	MISCK high level time	tch		80			ns
5	MISCK low level time	tcl		80			ns
6	nMICS and MISI setup time	tset	**Note 1)**	10			ns
7	nMICS and MISI hold time	thold	**Note 1)**	10			ns
8	MISO output delay time	tdelay	CL = 50pF			50	ns
9	MISO output High-Z time	tz	CL = 50pF			20	ns

Note 1) Satisfy the setup time/hold time (vs. MISCK) on starting/ending transfer, with nMICS = L.

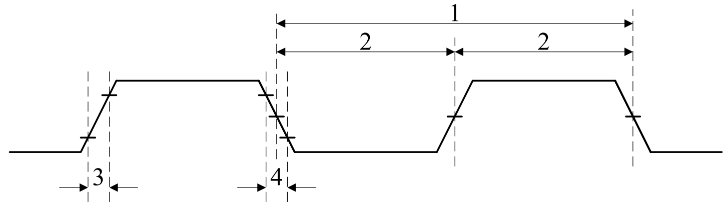


(c) Audio interface

1) SDIMCK

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
1	SDIMCK input frequency	f_{IMCK}				25	MHz
2	SDIMCK duty	d_{IMCK}			50		%
3	SDIMCK rise time	t_{IMR}				10	ns
4	SDIMCK fall time	t_{IMF}				10	ns

SDIMCK

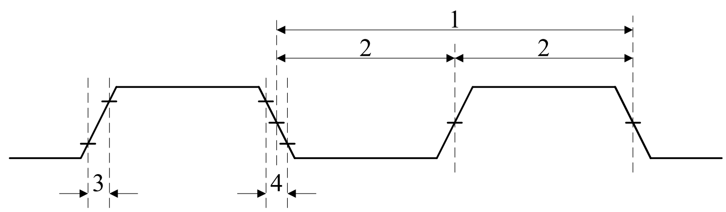


2) SDOMCK

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
1	SDOMCK output frequency	f_{OMCK}				25	MHz
2	SDOMCK duty	d_{OMCK}	**Note 1)**		50		%
3	SDOMCK rise time	t_{OMR}	CL = 50pF			10	ns
4	SDOMCK fall time	t_{OMF}	CL = 50pF			10	ns

Note 1) When MSEL[1:0] = 00 has been set and “through” has been selected for SDIMCK, the SDOMCK duty factor is affected by the SDIMCK duty factor.

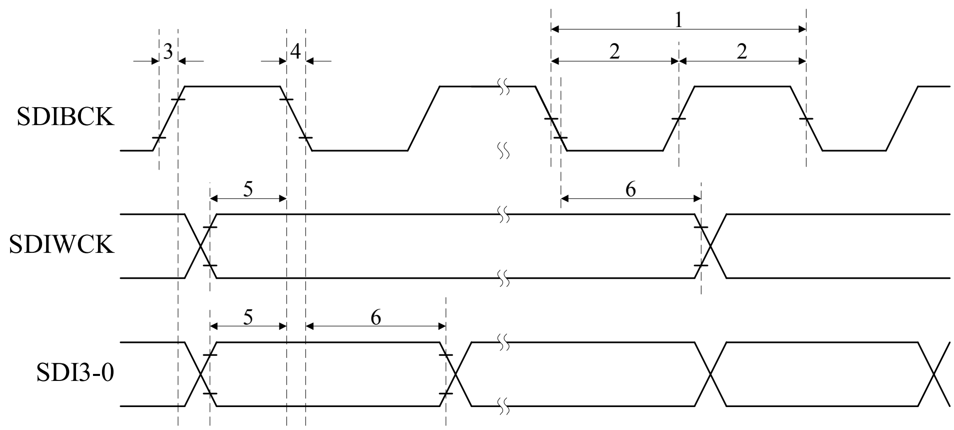
SDOMCK



3) SDIBCK, SDIWCK, SDI3 to SDI0 (slave operation)

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
1	SDIBCK input frequency	f_{IBCK}				12.5	MHz
2	SDIBCK duty	d_{IBCK}	**Note 1)**		50		%
3	SDIBCK rise time	t_{IBR}				10	ns
4	SDIBCK fall time	t_{IBF}				10	ns
5	SDIWCK and SDI3-0 setup time	t_{IWS}		10			ns
6	SDIWCK and SDI3-0 hold time	t_{IWH}		10			ns

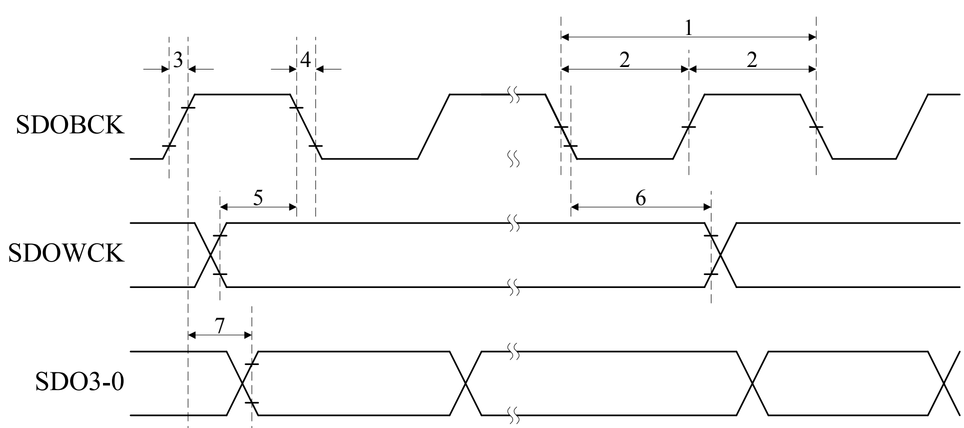
Note 1) The polarity of SDIBCK can be changed by SDIBP. In the figure below, SDIBP = 0.



4) SDOBCK, SDOWCK, SDO3 to SDO0 (slave operation)

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
1	SDOBCK input frequency	f_{OBCK}				12.5	MHz
2	SDOBCK duty	d_{OBCK}	**Note 1)**		50		%
3	SDOBCK rise time	t_{OBR}				10	ns
4	SDOBCK fall time	t_{OBF}				10	ns
5	SDOWCK setup time	t_{OWS}		10			ns
6	SDOWCK hold time	t_{OWH}		10			ns
7	SDO3-0 output delay time	t_{ODLY}	CL = 50pF			30	ns

Note 1) The polarity of SDOBCK can be changed by SDOBP. In the figure below, SDOBP = 0.



5) SDOBCK, SDOWCK, SDO3 to SDO0 (master operation)

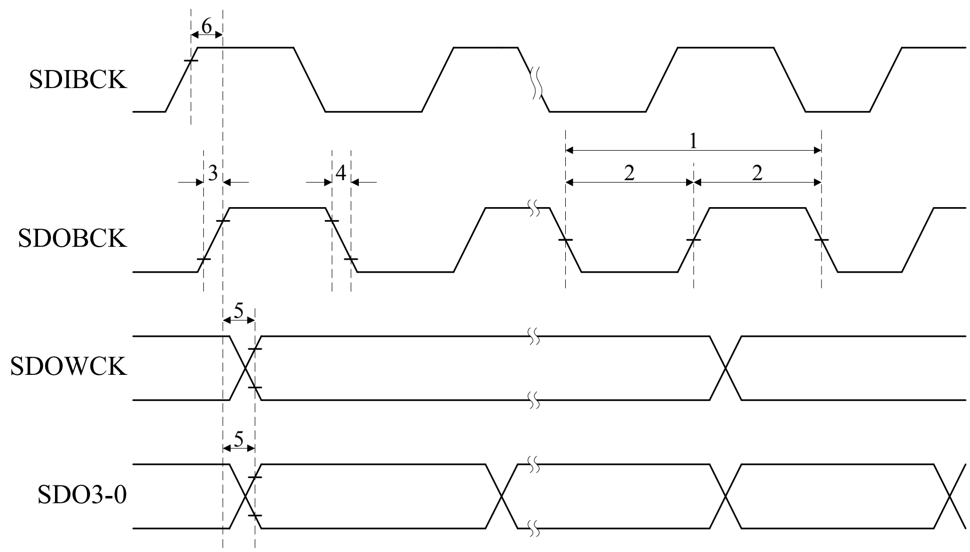
No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
1	SDOBCK output frequency	f_{OBCK}	**Note 2)**			12.5	MHz
2	SDOBCK output duty factor	d_{OBCK}	**Notes 1 and 3)**		50		%
3	SDOBCK rise time	t_{OBR}	CL = 50 pF			10	ns
4	SDOBCK fall time	t_{OBF}	CL = 50 pF			10	ns
5	SDOWCK, SDO3 to SDO0 Output delay time	t_{ODLY}	CL = 50 pF	-15		15	ns
6	SDIBCK → SDOBCK Output delay time	t_{OBDLY}	CL = 50 pF **Note 4)**	0		25	ns

Note 1) The output polarity of SDIBCK and SDOBCK can be changed by DSIBP and DSOBP. In the figure below, SDOBP = SDOBP = 0.

Note 2) Although output divided from SDIMCK can be selected for SDOBCK via WBSEL[2:0], operation is not guaranteed if SDIMCK's frequency exceeds the range noted above.

Note 3) When "SDIBCK through" has been selected (WBSEL[2:0] = 00), the SDDBCK output duty factor is affected by the SDIBCK duty factor.

Note 4) When "SDIBCK through" has been selected (WBSEL[2:0] = 00).

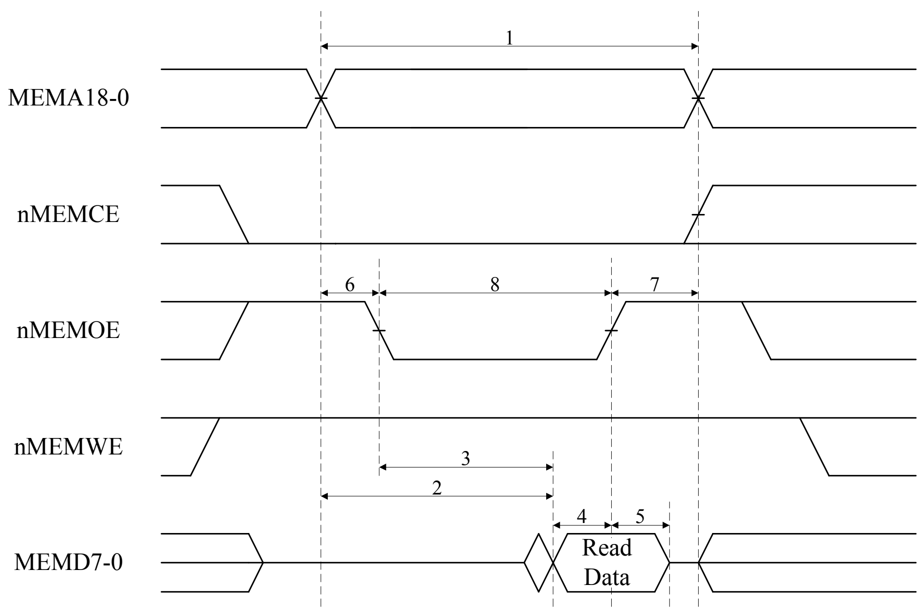


(d)External memory interface

When EM_CYC = c, EM_WEH = w, and EM_OEH = o, the timing is as described below.

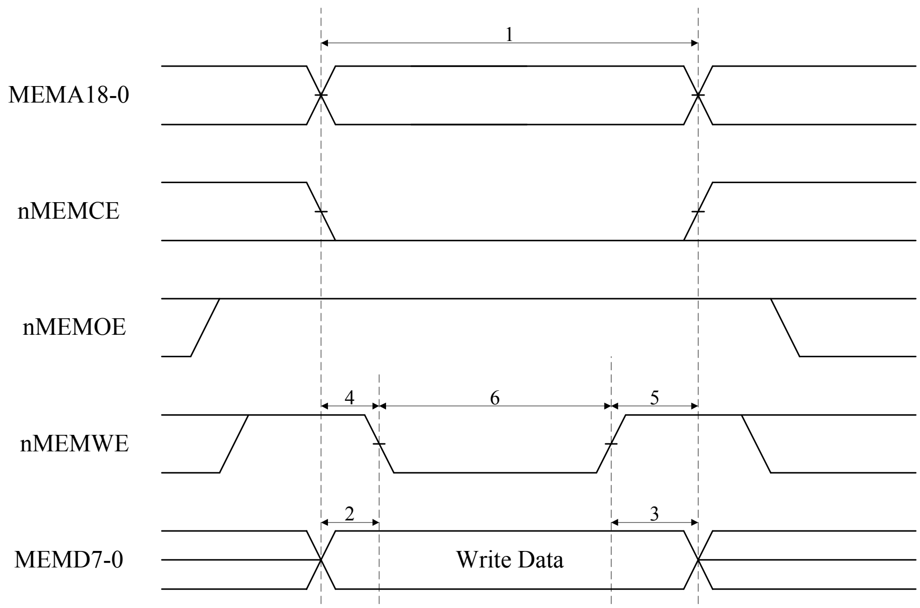
1) Read

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Read cycle time	t_{RCYC}	CL = 20 pF		$t_{ASR}+t_{REP}+t_{AHR}$		ns
2	Address access time	t_{AA}	CL = 20 pF			$T_{CLK}\times(2c+3)-25$	ns
3	nMEMOE access time	t_{EAC}	CL = 20 pF			$T_{CLK}\times(2c+2)-25$	ns
4	Data setup time	t_{DSR}		25			ns
5	Data hold time	t_{DHR}		0			ns
6	Address setup time	t_{ASR}	CL = 20 pF		$T_{CLK}\times1$		ns
7	Address hold time	t_{AHR}	CL = 20 pF		$T_{CLK}\times(2\hat{}o+1)$		ns
8	nMEMOE pulse width	t_{REP}	CL = 20 pF		$T_{CLK}\times(2c+2)$		ns



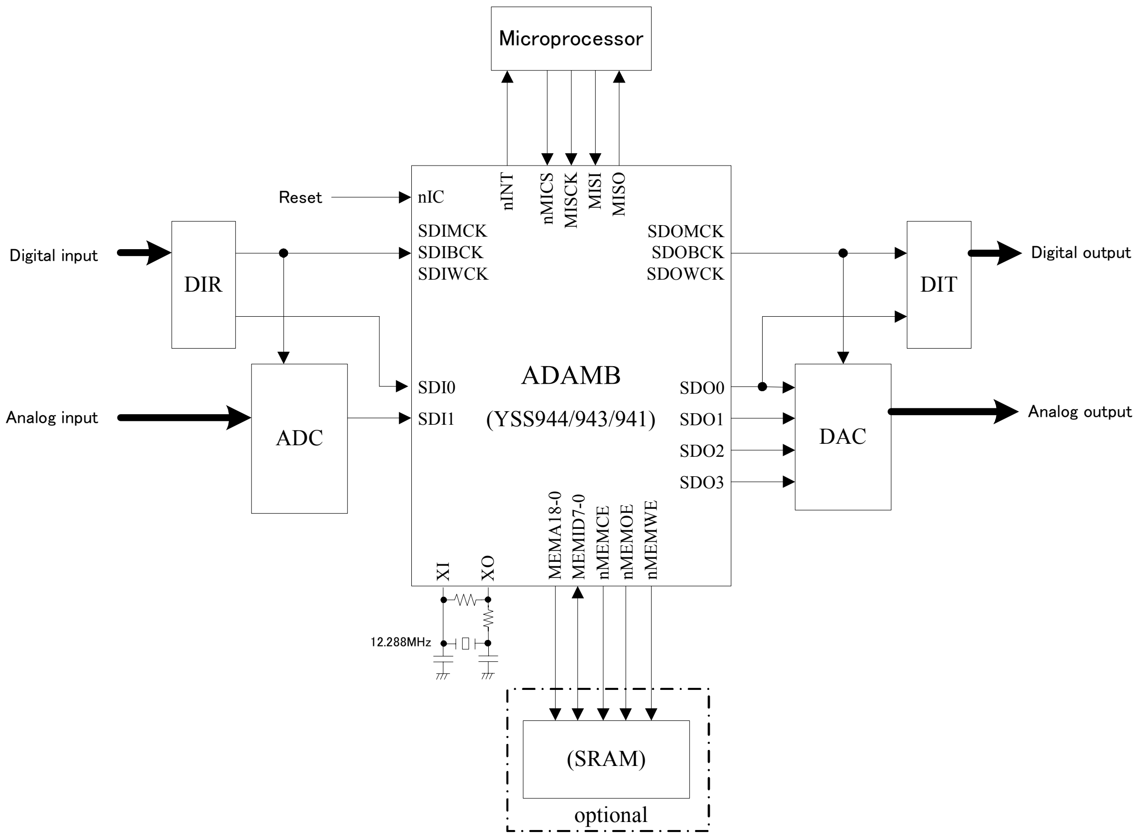
2) Write

No.	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Write cycle time	t_{WCYC}	CL = 20 pF		T_{CLK}×(2c+5+2w)		ns
2	Data setup time	t_{DSW}	CL = 20 pF	0	T_{CLK}×(w+1)		ns
3	Data hold time	t_{DHW}	CL = 20 pF	0	T_{CLK}×(w+2)		ns
4	Address setup time	t_{ASW}	CL = 20 pF		T_{CLK}×(w+1)		ns
5	Address hold time	t_{AHW}	CL = 20 pF		T_{CLK}×(w+2)		ns
6	nMEMWE pulse width	t_{WEP}	CL = 20 pF		T_{CLK}×(2c+2)		ns

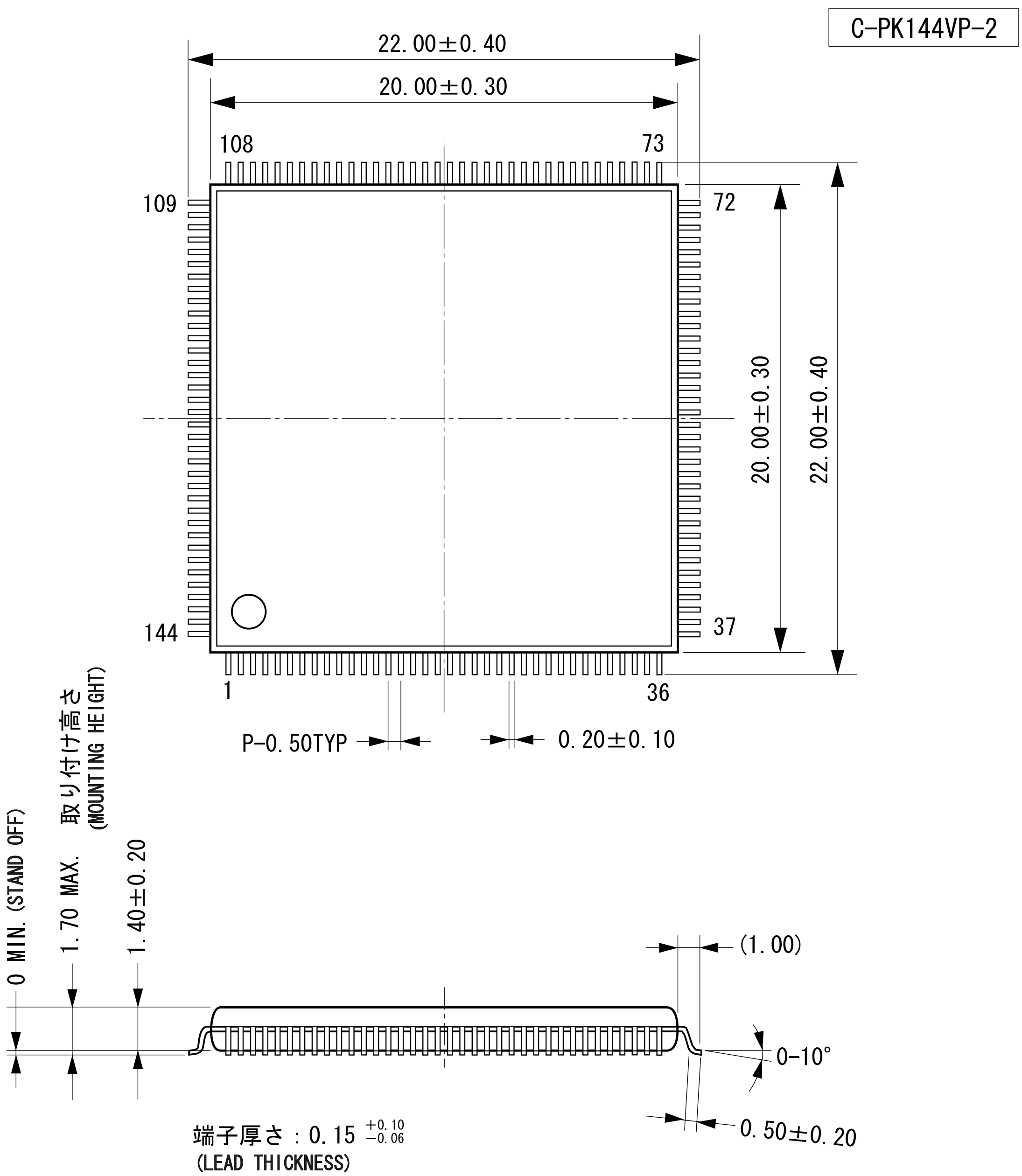


Example of System Configuration

The YSS944/943/940 is connected to CODEC (ADC/DAC) or DIR/DIT via the audio interface.
The YSS944/943/940 is connected to a microprocessor for control via the microcomputer interface.
External memory (SRAM) is an option when using the input/output delay function. The YSS944/943/940 can be used with only the internal RAM (without connecting external memory).



■ **Package Dimensions**



モールドコーナー形状は、この図面と若干異なるタイプもあります。
カッコ内の寸法値は参考値です。
モールド外形寸法はバリを含みません。
単位：mm

The shape of the molded corner may slightly differ from the shape in this diagram.
The figure in the parentheses ( ) should be used as a reference.
Plastic body dimensions do not include resin burr.
UNIT: mm

注） 表面実装LSIは、保管条件、及び半田付けについての特別な配慮が必要です。詳しくはヤマハ代理店までお問い合わせください。

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AGENT

YAMAHA CORPORATION

Address inquiries to:
Semiconductor Sales & Marketing Department

■ Head Office
203, Matsunokijima, Iwata,
Shizuoka, 438-0192, Japan
Tel. +81-539-62-4918 Fax. +81-539-62-5054

■ Tokyo Office
2-17-11, Takanawa, Minato-ku,
Tokyo, 108-8568, Japan
Tel. +81-3-5488-5431 Fax. +81-3-5488-5088

■ Osaka Office
3-12-12, Minami Senba, Chuo-ku,
Osaka City, Osaka, 542-0081, Japan
Tel. +81-6-6252-6221 Fax. +81-6-6252-6229

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