Nm9805

PCI + 1284 Printer Port

Features

- Single 5V operation
- Low power
- PCI compatible 1284 printer port
- Multi-mode compatible controller (SPP, PS2, EPP, ECP)
- Fast data rates up to 1.5 Mbytes/s (parallel port)
- 16-byte FIFO (parallel)
- Re-map function for legacy ports
- Microsoft Compatible
- Software programmable mode selects
- 128-pin QFP package

Applications

- Printer server
- Portable backup units
- Printer interface
- Add-on I/O cards

Application Notes

- AN-9805

General Description

The Nm9805 is a 1284 parallel port controller with PCI bus interface. Nm9805 fully supports the existing Centronics printer interface as well as PS/2, EPP, and ECP modes.

The Nm9805 is ideally suited for PC applications, such as high speed parallel ports. The Nm9805 is available in a 128-pin QFP package. It is fabricated using an advanced submicron CMOS process to achieve low drain power and high-speed requirements.

Ordering Information

Commercial Grade		
Nm9805CV	128-QFP	0° C to +70° C

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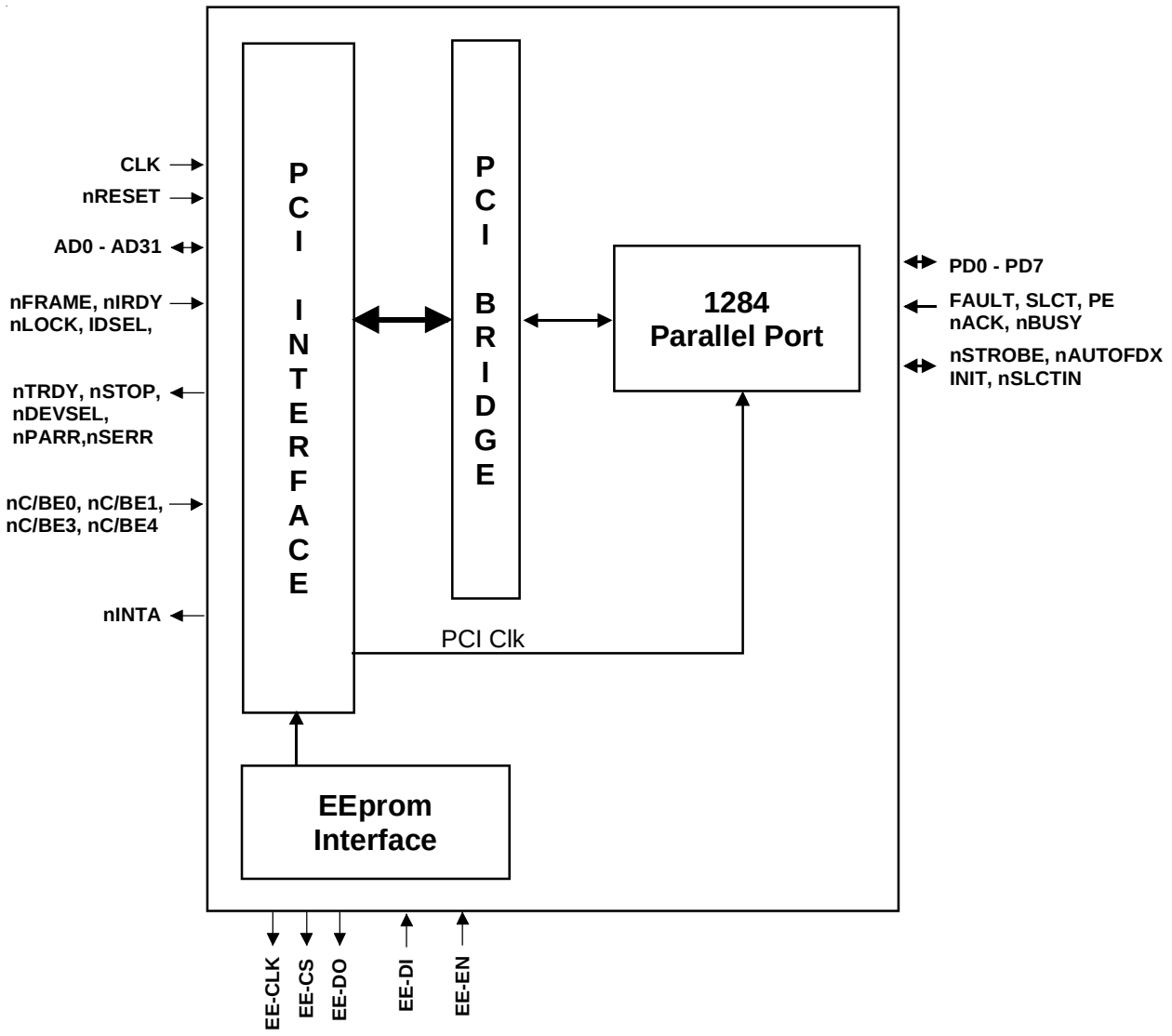
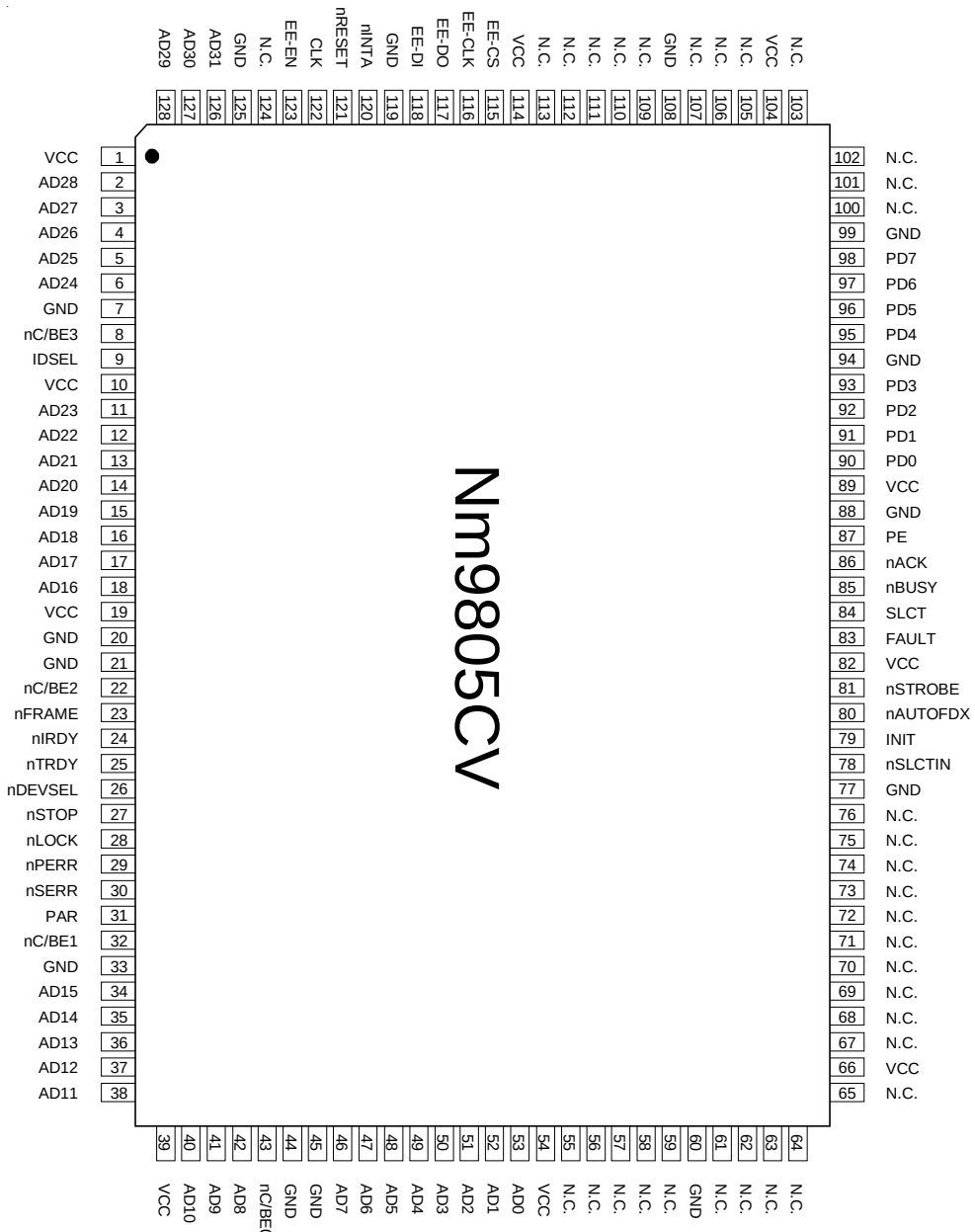
Nm9805 Block Diagram



128-Pin QFP Package



Pin Name	128	Type	Description
CLK	122	I	33 MHz PCI system clock input.
nRESET	121	I	PCI system reset (active low). Resets all internal register, sequencers, and signals to a consistent state. During reset condition AD31-0, nSER are three-stated.
AD31-29	126-128	I/O	Multiplexed PCI address/data bus. A bus transaction consists of an address phase followed by one or more data phases. During the address phase, AD31-0 contain a physical address. Write data is stable and valid when nIRDY and nTRDY are asserted (active).
AD28-24	2-6	I/O	See AD31-29 description.
AD23-16	11-18	I/O	See AD31-29 description.
AD15-11	34-38	I/O	See AD31-29 description.
AD10-8	40-42	I/O	See AD31-29 description.
AD7-0	46-53	I/O	See AD31-29 description.
nFRAME	23	I	Frame is driven by the current master to indicate the beginning and duration of an access. nFRAME is asserted to indicate a bus transaction is beginning. While nFRAME is active, data transfer continues.
nIRDY	24	I	Initiator Ready. During a write, nIRDY asserted indicates that the initiator is driving valid data onto the data bus. During a read, nIRDY asserted indicates that the initiator is ready to accept data from the Nm9805.
nTRDY	25	O	Target Ready (three-state). It is asserted when Nm9805 is ready to complete the current data phase.
nSTOP	27	O	Nm9805 asserts nSTOP to indicate that it wishes the initiator to stop the transaction in process on the current data phase.
nLOCK	28	I	Lock indicates an atomic operation that may require multiple transactions to complete.
IDSEL	9	I	Initialization Device Select. It is used as a chip select during configuration read and write transactions.
nDEVSEL	26	O	Device Select (three-state). Nm9805 asserts nDEVSEL when the Nm9805 has decoded its address.
nPERR	29	O	Parity Error (three-state). Is used to report parity errors during all PCI trans-

Pin Name	128	Type	Description
			actions except a special cycle. The minimum duration of nPERR is one clock cycle.
nSERR	30	O	System Error (open drain). This pin goes low when address parity errors are detected.
PAR	31	I/O	Even Parity. Parity is even parity across AD31-0 and nC/BE3-0. PAR is stable and valid one clock after the address phase. For data phase, PAR is stable and valid one clock after either nIRDY is asserted on a write transaction, or nTRDY is asserted on a read transaction.
nC/BE3	8	I	Bus Command and Byte Enable. During the address phase of a transaction, nC/BE3-0 defines the bus command. During data phase, nC/BE3-0 are used as byte enables. nC/BE3 applies to byte “3”.
nC/BE2	22	I	Bus Command and Byte Enable. During the address phase of a transaction, nC/BE3-0 defines the bus command. During data phase, nC/BE3-0 are used as byte enables. nC/BE2 applies to byte “2”.
nC/BE1	32	I	Bus Command and Byte Enable. During the address phase of a transaction, nC/BE3-0 defines the bus command. During data phase, nC/BE3-0 are used as byte enables. nC/BE1 applies to byte “1”.
nC/BE0	43	I	Bus Command and Byte Enable. During the address phase of a transaction, nC/BE3-0 defines the bus command. During data phase, nC/BE3-0 are used as byte enables. nC/BE0 applies to byte “0”.
nINTA	120	O	PCI active low interrupt output (open-drain). This signal goes low (active) when an interrupt condition occurs.
EE-CS	115	O	External EEprom chip select (active high). After power on reset, Nm9805 reads the EE-Prom and loads the read-only configuration registers sequentially from the first 64 bytes in the EE-Prom.
EE-CLK	116	O	External EEprom clock.
EE-DI	118	I	External EEprom data input.
EE-DO	117	O	External EEprom data output.
EE-EN	123	I	Enable/Disable external EEprom (active high, internal pull-up). External EEprom can be disabled when this pin is tied to GND or pulled low. When external EEprom is disabled, the default values for Nm9805 will be loaded into PCI configuration register.

Pin Name	128	Type	Description
SLCT	84	I	Peripheral/printer selected (internal pull-up). This pin is set to high by peripheral/printer when it is selected.
PE	87	I	Paper empty (internal pull-up). This pin is set to high by peripheral/printer when printer paper is empty.
nBUSY	85	I	Peripheral/printer busy (internal pull-up). This pin is set to high by peripheral/printer when printer or peripheral is not ready to accept data.
nACK	86	I	Peripheral/printer data acknowledge (internal pull-up). This pin is set to low by peripheral/printer to indicate a successful data transfer has taken place. During SPP mode when interrupt is enabled, nINTA pin follows the nACK input pin state.
nFAULT	83	I	Peripheral/printer data error (internal pull-up). This pin is set to low by peripheral/printer during error condition.
nSTROBE	81	I/O	Peripheral/printer data strobe (open drain, active low). On the rising edge of the nSTROBE, data is latched into printer port.
nAUTOFDX	80	I/O	Peripheral/printer auto feed (open-drain, active low). Continuous autofed paper is selected when this pin is set to low.
nINIT	79	I/O	Initialize the Peripheral/printer (open drain, active low). When set to low, peripheral/printer starts it's initialization routine.
nSLCTIN	78	I/O	Peripheral/printer select (open-drain, active low). Selects the peripheral/printer when it is set to low.
PD7-PD4	98-95	I/O	Peripheral/printer data ports.
PD3-PD0	93-90	I/O	Peripheral/printer data ports.
GND	7,20,21, 33,44,45, 60,77,88, 94,99,108 119,125	Pwr	Power and signal ground.
VCC	1,10,19, 39,54,66, 82,89,104, 114	Pwr	5V supply.

PCI bus operation:
The execution of PCI bus transaction takes place in broadly five stages: address phase; transaction claiming; data phase(s); final data transfer; and transaction completion.

Address phase:
Every PCI transaction starts off with an address phase, one PCI clock period in duration. During address phase the initiator (also known as current bus master) identifies the target device (via the address) and type of transaction (via the command). The initiator drives the 32-bit address onto 32-bit address/data bus and 4-bit command onto 4-bit command/byte enable bus. The initiator also asserts the nFRAME signal during the same clock cycle to indicate the presence of valid address and transaction type on those buses. The initiator supplies start address and command type for one PCI clock cycle. The target, Nm9805, generates the subsequent sequential addresses for burst transfers. The address/data bus becomes data bus and command/byte enable bus becomes byte enable bus for the remainder of the clock cycles of that transaction. The target (Nm9805) latches the address and command type on the next rising edge of PCI clock, as do all the devices on that PCI bus. The target (Nm9805) decodes the address and determines whether it is being addressed, and decodes the command to determine the type of transaction.

Claiming the transaction:
When Nm9805 determines that it is the target of a transaction, it claims the transaction by asserting nDEVSEL.

Data phase(s):
The data phase of a transaction is the period during which a data object is transferred between the initiator and the target (Nm9805). The number of data bytes to be transferred during a data phase is determined by the number of command/byte enable signals that are asserted by the initiator during the data phase. Each data phase is at least one PCI clock period in duration. Both initiator and target must indicate that they are ready to complete a data phase. If not, the data phase is extended by a wait state of one clock period in duration. The initiator and the target indicate this by asserting nIRDY and nTRDY respectively and the data transfer is completed at the rising edge of the next PCI clock.

Transaction duration:
The initiator, as stated earlier, gives only start address during address phase but does not tell the number of data transfers in a burst transfer transaction. However, the initiator indicates the completion of data transfer of a transaction by asserting nIRDY and de-asserting nFRAME during the last data transfer phase. The transaction, however, does not complete until the target has also asserted the nTRDY signal and the last data transfer takes place. At this point the nTRDY and nDEVSEL are de-asserted by the target.

Transaction completion:
When all of nIRDY, nTRDY, nDEVSEL, and nFRAME are in inactive state (high state), the bus is in idle state. The bus is ready to be claimed by another bus master.

Internal address select configuration

I/O Address	Function
YX0-YX07	Standard Printer
WX00	Printer Configuration Register A
WX01	Printer Configuration Register B
WX02	Printer ECR Register

Nm9805 configuration space register map

AD 31-23	AD 22-16	AD 15-8	AD 7-0	Addr
Device ID (9805)		Vendor ID (9710)		00H
Status		Command		04H
Class Code (070102)			Revision ID (01)	08H
BIST	Header Type	Latency Timer	Cache Size (08)	0CH
I/O (Y) Base Address				10H
I/O (W) Base Address				14H
Reserved				18H
Reserved				1CH
Reserved				20H
Reserved				24H
Reserved				28H
Subsystem ID		Subsystem Vendor ID		2CH
Reserved				30H
Reserved				34H
Reserved				38H
Max Latency (00)	Min Grant (00)	Interrupt Pin (01)	Interrupt Line	3CH

Printer Register Table

Ex A2 A1 A0	REGISTER	D7	D6	D5	D4	D3	D2	D1	D0
Y 0 0 0	DPR	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Y 0 0 1	DSR	nBUSY	nACK	PE	SLCT	FAULT	INT state	“0”	EPP TIMEOUT
Y 0 1 0	DCR	“0”	“0”	DIR	INTA	nSLCTIN	INIT	nAUTOFD	nSTROBE
Y 0 1 1	EPP Address	ADD-7	ADD-6	ADD-5	ADD-4	ADD-3	ADD-2	ADD-1	ADD-0
Y 1 0 0	EPP data	DAT-7	DAT-6	DAT-5	DAT-4	DAT-3	DAT-2	DAT-1	DAT-0
Y 1 0 1	EPP data	DAT-15	DAT-14	DAT-13	DAT-12	DAT-11	DAT-10	DAT-9	DAT-8
Y 1 1 0	EPP data	DAT-23	DAT-22	DAT-21	DAT-20	DAT-19	DAT-18	DAT-17	DAT-16
Y 1 1 1	EPP data	DAT-31	DAT-30	DAT-29	DAT-28	DAT-27	DAT-26	DAT-25	DAT-24
W 0 0 0	C-FIFO	CDAT-7	CDAT-6	CDAT-5	CDAT-4	CDAT-3	CDAT-2	CDAT-1	CDAT-0
W 0 0 0	CONF-A	“1”	“0”	“0”	“1”	“0”	“1”	“0”	“0”
W 0 0 1	CONF-B	“0”	INT Pin	“0”	“0”	“0”	“0”	“0”	“0”
W 0 1 0	ECR	MODE select			ErrIntrEn enable	“0”	Service Int	FIFO full	FIFO empty

Y: Internal standard printer chip select
W: Internal printer configuration register chip select

Data Register
Data register is cleared at initialization by RESET. During a write operation, the data register latches the contents of the data bus with the rising edge of the nIOW input. The contents of this register are buffered and output onto the PD7-PD0 ports. During a read operation PD7-PD0 ports are buffered and output to the host CPU on the falling edge of the nIOR input.

Device Status Register
The contents of this register are latched for the duration of the nIOR cycle. The bits of the status port are defined as follows.

DSR Bit-0:
0 = Normal.
1 = 10µs timeout (EPP mode only). Cleared by writing 1 into DSR register or consecutive reads (after the first read) always returns to "0".

DSR Bit-1:
Not used, set to "0".

DSR Bit-2:
0 = nACK input pin is at low state (INT follows the nACK pin) when SPP mode is selected. Normal (no interrupt) when PS/2 mode is selected.
1 = Normal (no interrupt). In standard mode operation, INT is active (interrupt is generated on the rising edge of the nACK). It is cleared when DSR is read.

DSR Bit-3:
0 = Printer reports error condition.
1 = Normal operation.

DSR Bit-4:
0 = Printer is off line.
1 = Printer is on line.

DSR Bit-5:
0 = Normal operation
1 = Paper end/empty is detected

DSR Bit-6:
0 = State of the nACK pin (ACK = low).
1 = State of the nACK pin (ACK = high).

DSR Bit-7:
0 = nBUSY pin is high, printer is not ready to take data.
1 = nBUSY pin is low, printer is read to take data.

Device Control Register

DCR Bit-0:
0 = Sets the nSTROBE pin to high.
1 = Sets the nSTROBE pin to low. PD7-PD0 data are latched into printer

DCR Bit-1:
0 = Sets the nAUTOFD pin to high. Printer generates auto line feed after each line is printed.
1 = Sets the nAUTOFD pin to low. No auto feed function.

DCR Bit-2:
0 = Sets the INIT pin to high.
1 = Sets the INIT pin to low. Peripheral/printer starts it's initialization routine.

DCR Bit-3:
0 = Sets the nSLCTIN pin to high. Selects the printer.
1 = Sets the nSLCTIN pin to low. Printer is not selected.

DCR Bit-4:
0 = Disables Printer interrupt function. nACK pin has no effect on the INT pin.
1 = Enables Printer interrupt function. The INT follows the nACK input pin during standard mode, latches high on the rising edge of the nACK, when PS/2 mode is selected.

DCR Bit-5:
0 = PD7-PD0 pins are out put mode.
1 = PD7-PD0 pins are input mode.

DCR Bits 7-6:
Not used, set to "0".

Config-A Register

Configuration A register (read only). Reading this register returns 10010100. Writing to this register has no effect and the data is ignored.

Config-B Register

Configuration B register. This register allows software to control the selecting of interrupts. A read-write implementation implies a "software-configurable" device. Reading this register returns the configured interrupt and interrupt pin state. If a value is not set to 000 (the jumper-default) then it is assumed that the value in the register is correct and software will use the default interrupt.

Config-B Bit-7:
Not used, set to "0".

Config-B Bit-6:
0 = Configured printer interrupt pin is low.
1 = Configured printer interrupt pin is high.

Config-B Bit 7-0:
Interrupt pin select register.

Extended Control Register (ECR)

This register controls the mode selection and DMA operation.

Bit-7	Bit-6	Bit-5	Operating Mode
0	0	0	SPP
0	0	1	PS/2
0	1	0	PPF (FIFO mode)
0	1	1	ECP
1	0	0	EPP
1	0	1	Not used
1	1	0	FIFO test
1	1	1	Config A/B enable

Mode changes

After hardware reset, PS/2 mode is selected as default mode. It is required to select mode 000 or 001 between any other mode configuration.

Mode "000"
SPP/Centronics/Compatible Mode
Forward direction only. The direction bit is forced to "0" and PD7-PD0 are set to output direction. The Nm9805 is under software control. This mode defines the protocol used by most PCs to transfer data to a printer. It is commonly called the Centronics mode and is the method utilized with the standard parallel port. Data is placed on the PD7-PD0 ports, the printer status is checked via DSR register. If no error condition is flagged and printer is not busy, software toggles the nSTROBE pin to latch the PD7-PD0 data into printer. This operating cycle continues when printer/peripheral issues data acknowledge signal (pulses the ACK and nBUSY pin).

Nibble Mode

The nibble mode is the most common way to get reverse channel data from a printer or peripheral. This mode is usually combined with the Centronics mode or a proprietary forward channel mode to create a bi-directional channel. In this mode printer status bits are used as nibble bits.

Bits order for nibble mode

PINS	DATA Bits
nBUSY	Bit-7
PE	Bit-6
SLCT	Bit-5
nFAULT	Bit-4
nBUSY	Bit-3
PE	Bit-2
SLCT	Bit-1
nFAULT	Bit-0

Mode "001"
PS/2, Byte Mode
The byte mode protocol is used to transfer bi-directional data via PD7-PD0 ports without FIFO utilization. The direction of the port is controlled with DIR bit in DCR register. PS/2-byte use SPP protocol for data transfer.

DCR Bit-5:
0 = PD7-PD0 pins are out put mode.
1 = PD7-PD0 pins are input mode.

Mode “010”
FIFO Output Mode
In this mode, bytes written to the FIFO are transmitted automatically using the SPP/Centronics standard protocol.

Mode “011”
Extended Capability Port “ECP” Mode
The ECP provides an advanced mode for communication with printer or peripherals. Like EPP protocol, ECP provides 16-byte FIFO for a high performance bi-directional communication path between the host adapter and the peripheral. The ECP protocol provides the following cycle types in both the forward and reverse directions:

- Data cycle
- Command cycles
- Run-Length counts (RLE)
- Channel address

The RLE feature enables real time data compression that can achieve compression ratios up to 64:1. This is particularly useful for printers and peripherals that are transferring large raster images that have large strings of identical data. In order for the RLE mode to be enabled, both the host and peripheral must support it. Channel addressing is intended to address multiple logical devices within a single physical device, like modem/FAX/printer in one physical package.

Mode “100”
Enhanced Parallel Port “EPP” Mode
In EPP mode, nSLCTIN (address strobe) and nAUTOFD (data strobe) are automatically generated while nSTROBE indicates a write or read cycle. Additional I/O addresses are defined for data and address access and when these locations are used, handshaking is performed automatically by Nm9805.

Mode “110”
FIFO Test Mode
In this mode, the FIFO can be written and read in any direction, but no data will be transmitted on the PD7-PD0 ports. Whatever data is in the FIFO may be displayed on the PD7-PD0 ports.

ECR Bit-4:
Error Interrupt Enable.
0 = Enable nFAULT interrupt. nFAULT pin is used as source of interrupt.
1 = Disable nFAULT interrupt (nACK is used as source of interrupt).

ECR Bit-3:
0 = normal operating mode.

ECR Bit-2:
1 = Disables service interrupt.
0 = Enables one of the following 3 cases of interrupts. One of the 3 service interrupts has occurred. Service interrupt bit will be set to a “1” by hardware. Writing this bit to a “1” will not cause an interrupt.

Port Direction (DCR Bit-5 = 0). This bit will be set to “1” whenever there are write interrupt thresholds (4 characters) or more bytes free in the FIFO. The Nm9805 generates interrupt when this condition is occurred and service interrupt is cleared to “0”.

Port Direction (DCR Bit-5 = 1). This bit will be set to “1” whenever there are read interrupt thresholds (12 characters) or more bytes to be read from the FIFO. The Nm9805 generates interrupt when this condition is occurred and service interrupt is cleared to “0”.

ECR Bit-1:
0 = One or more empty locations in FIFO is available.
1 = FIFO full.

ECR Bit-0:
0 = One or more data in FIFO.
1 = FIFO empty.

Master rest conditions

Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
DPR	X	X	X	X	X	X	X	X
DSR	0	1	1	1	1	0	0	0
DCR	0	0	0	0	0	0	0	0
EPP	0	0	0	0	0	0	0	0
C-FIFO	0	0	0	0	0	0	0	0
CONF-A	1	0	0	1	0	1	0	0
CONF-B	0	X	0	0	0	0	0	0
ECR	0	0	0	0	0	0	0	1

Absolute Maximum Ratings

Supply Range	7 Volts
Voltage at any pin	GND – 0.3 to VCC +0.3
Operating Temperature	-45° C to 90° C
Storage Temperature	-65° C to 150° C
Package Dissipation	500 mW
ESD	±2000 Volts
Latch up	220 mA

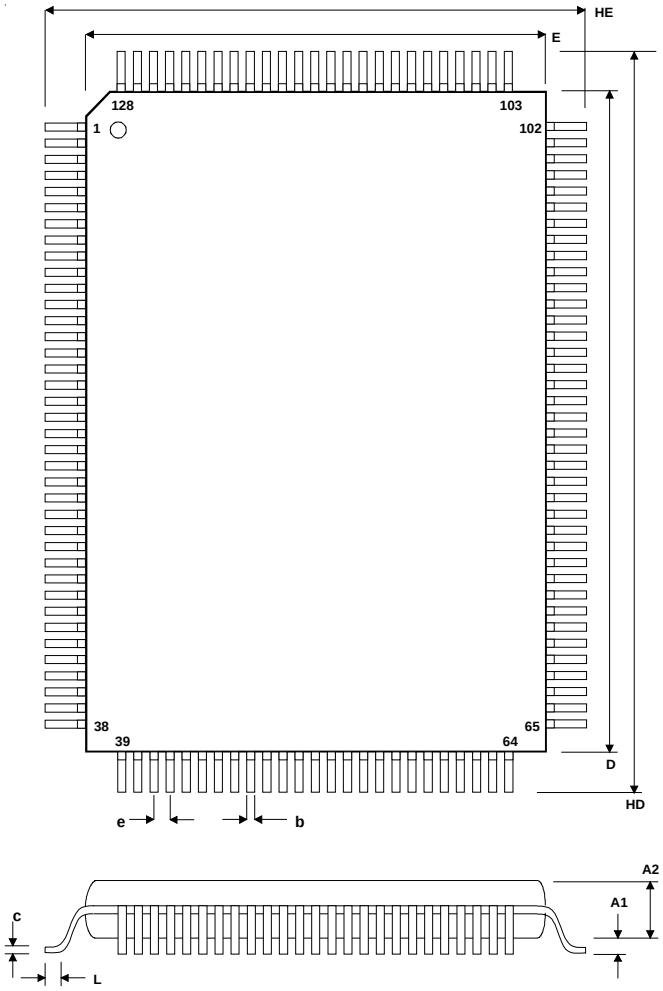
DC Electrical Specification

T = 0° C to 70° C, VCC = 5V ± 10% unless otherwise specified.

Symbol	Parameter	5V Min	5V Max	Unit	Condition
Vil	Input Low voltage	-0.3	0.8	V	
Vih	Input High voltage	2.0		V	
Vt-	Schmitt trigger negative going threshold voltage	1.10		V	
Vt+	Schmitt trigger positive going threshold voltage	1.87		V	
Vol	Output low voltage		0.4	V	Iol=4 mA
Voh	Output high voltage	3.5		C	Ioh=4 mA
Iil	Input low current		±1	µA	
Iih	Input high current		±1	µA	
Ioz	Three state leakage current		±10	µA	
Cin	Input capacitance	3	5	pF	
Cout	Output capacitance	3	5	pF	
Icc	Operating current		60	mA	No load

Revision	Notes	Date
1.1	Ordering information changed	7/02

128-Pin QFP (14X20) Package



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A1	0.10	0.30	0.004	0.012
A2	2.73	2.97	0.107	0.117
b	0.17	0.27	0.007	0.011
c	0.09	0.20	0.004	0.008
e	0.50 TYP		0.020 TYP	
L	0.70	1.03	0.029	0.041
HD	23.00	23.40	0.906	0.921
D	19.90	20.10	0.783	0.791
HE	17.00	17.40	0.669	0.685
E	13.90	14.10	0.547	0.555

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