Genesys Logic, Inc.

GL819

USB 2.0 Generation 3 Multi-I/F Card Reader Controller

Version-11/13

Datasheet
Revision 1.03
Oct. 16, 2007

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Revision History

Revision	Date	Description
1.00	09/27/2006	First formal release
1.01	03/22/2007	1. Pin List, Ch3.2, p.10 2. Pin Out, Ch3.3, p.11 3. Absolute Maximum Ratings, Ch6.1, p16 4. DC Characteristics, Ch6.3, p.16
1.02	04/30/2007	Remove over current protection support
1.03	10/16/2007	Modify: 1. SD Interface Timing , Ch6.5.7, p.29, 30 2. SD_WP description, Table3.2, p.12

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CHAPTER 1 GENERAL DESCRIPTION

The GL819 is the 3rd generation USB 2.0 Multi-Interface Flash Card Reader controller. It supports USB 2.0 high-speed transmission to:

CompactFlash™ (CF) Type I/II, Micro Drive, Secure Digital™ (SD), Mini SD™, MultiMediaCard™ (MMC), RS MultiMediaCard™ (RS MMC), HS-MMC, MMC-Mobile , Memory Stick™ (MS), Memory Stick Duo™ (MS Duo), High Speed Memory Stick™ (HS MS), Memory Stick PRO™ (MS PRO), Memory Stick PRO™ Duo (MS PRO Duo) Memory Stick ROM, and SmartMedia™ (SM) 5V/3.3V and xD-Picture Card™ (xD)on one chip. Besides the flash card interface controller each, the GL819 integrates Genesys Logic own design USB 2.0 high-speed UTMI (**U**SB 2.0 **T**ransceiver **M**acrocell **I**nterface) transceiver. As a single chip solution for USB 2.0 multi flash card reader, the GL819 complies with Universal Serial Bus specification rev. 2.0, USB Storage Class specification ver.1.0, and flash card interface specification each.

The GL819 can support different kinds of multi-interface combinations. For the best performance consideration, the GL819 integrates high efficiency card interface hardware engine for data transfer. The GL819 also supports firmware upgrade via USB interface, and external flash read/ write for firmware upgrade and other applications.

The GL819 pin assignment design fits to card sockets to provide easier PCB layout. Package type is 128-pin LQFP (14mm x 14mm), the GL819 can fit your various designs in both standalone and PC embedded USB 2.0 multi-interface flash card reader/ writer applications.

CHAPTER 2 FEATURES

- USB specification compliance
  - Comply with 480Mbps Universal Serial Bus specification rev. 2.0.
  - Comply with USB Storage Class specification rev. 1.0.
  - Support 1 device address and up to 4 endpoints: Control (0)/ Bulk Read (1)/ Bulk Write (2)/Interrupt (3).
- Integrated USB building blocks
  - USB2.0 transceiver macro (UTM), Serial Interface Engine (SIE), Build-in power-on reset (POR) and low-voltage detector (LVD)
- Embedded 8051 micro-controller
  - Operate @ 60 MHz clock, 12 clocks per instruction cycle
  - Embedded 48K-byte mask ROM and internal 256 byte SRAM
  - Embedded 4K-byte external SRAM
  - Support up to external 48K code ROM
- Support firmware upgrade to external flash via USB (ISP : in system programming)
- USB 2.0 certified (Test ID=40002675)
- WHQL submission number 938163
- Vista submission number 1220953
- On-Chip power MOSFETs to control flash media card power.
- CompactFlash™ interface
  - Support CFA specification v2.1 / v3.0
  - Support True IDE mode
  - Support 8 / 16 bit data mode and different timing
- SmartMedia™ interface
  - 8 bit data width and different speed
  - Support different page size, and automatic append redundant area data (8 / 16 bytes)
- xD-Picture Interface (Submission ID: AA-RG0435)
  - Compliant with xD-Picture specification v1.2B.
  - xD-Picture Type M/H card support.
- MemoryStick™ / MemoryStick PRO interface
  - Compliant with MemoryStick interface specification v1.40-00
  - Compliant with MemoryStick PRO interface specification v1.00-01
  - Support automatic CRC16 generation and verification
- Secure Digital™ and MultiMediaCard™
  - Compliant with Secure Digital specification v2.0
  - Compliant with MMC interface specification v4.2 (external flash)
  - Support both SD / MMC mode access CLK/CMD/DAT0/DAT1/DAT2/DAT3/DAT4/DAT5/DAT6/DAT7
  - Support SD specification v1.0 / v1.1 / v2.0
  - Support MMC specification v4.0 / v4.1 / v4.2(ext flash support) x1 / x4 / x8 data transmission.
  - Automatic CRC7 generation for command and CRC7 verification for response on CMD
  - Support automatic CRC16 generation and verification on DAT0:7
  - In addition to full packet transaction, optional single byte / bit operation on both CMD and DAT line / lines
  - Process data in block or byte
- High efficient hardware engine
  - Automatic data read / write with card by hardware engine
  - Easier firmware development
- On board 12 MHz Crystal driver circuit
- Available in 128-pin LQFP 14x14 mm package

CHAPTER 3 PIN ASSIGNMENT

3.1 Pinout

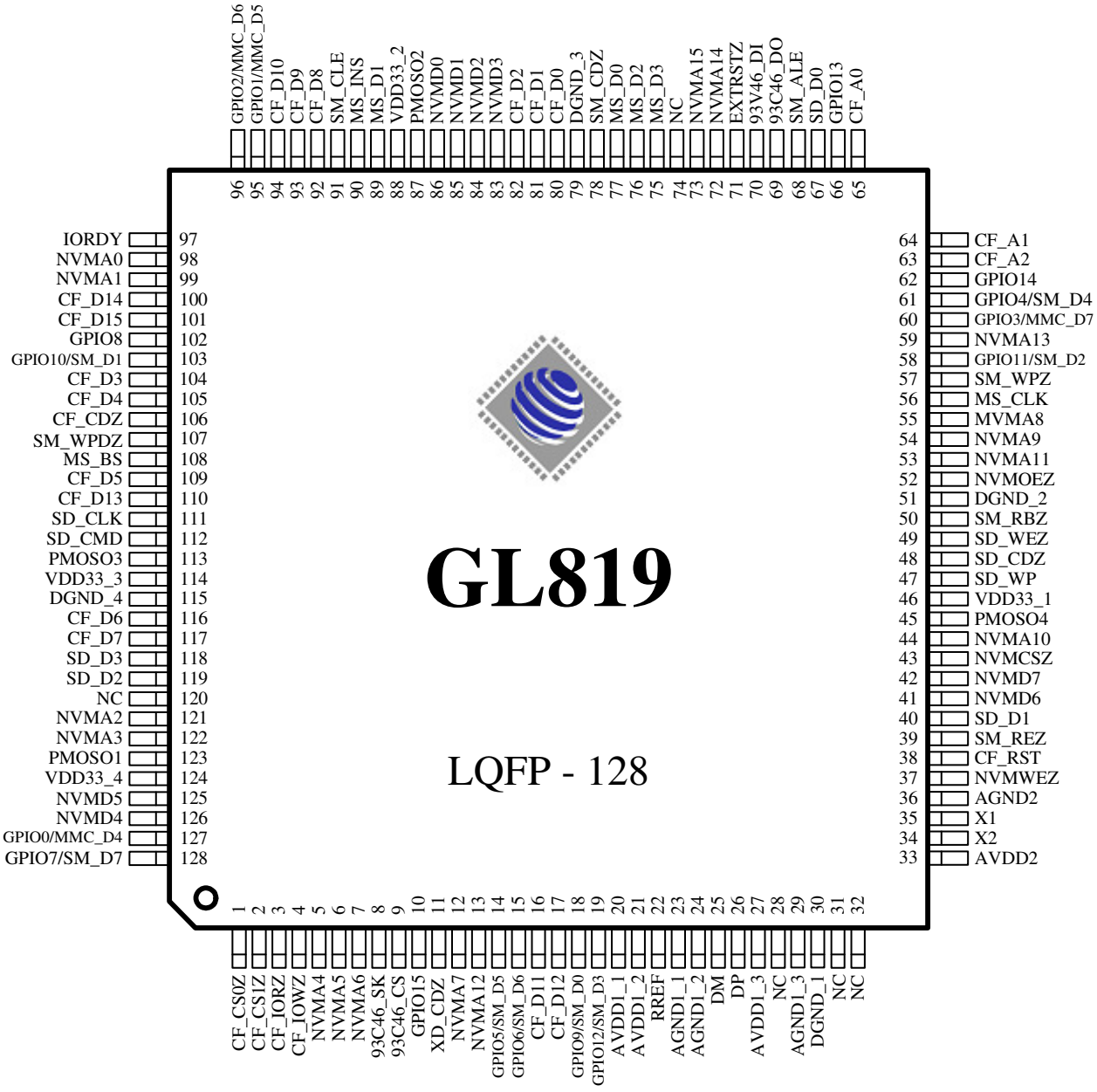


Figure 3.1 - 128 Pin LQFP Pinout Diagram

3.2 Pin List

Table 3.1 - Pin List

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	CF_CS0Z	O	33	AVDD2	P	65	CF_A0	O	97	IORDY	I
2	CF_CS1Z	O	34	X2	B	66	GPIO13	B	98	NVMA0	O
3	CF_IORZ	O	35	X1	I	67	SD_D0	B	99	NVMA1	O
4	CF_IOWZ	O	36	AGND2	P	68	SM_ALE	O	100	CF_D14	B
5	NVMA4	O	37	NVMWEZ	O	69	93C46_DO	O	101	CF_D15	B
6	NVMA5	O	38	CF_RST	O	70	93C46_DI	I	102	GPIO8	B
7	NVMA6	O	39	SM_REZ	O	71	EXTRSTZ	I,PU	103	GPIO10/ SM_D1	B
8	93C46_SK	O	40	SD_D1	B	72	NVMA14	O	104	CF_D3	B
9	93C46_CS	O	41	NVMD6	B	73	NVMA15	O	105	CF_D4	B
10	GPIO15	B	42	NVMD7	B	74	NC	—	106	CF_CDZ	I
11	XD_CDZ	I	43	NVMCSZ	O	75	MS_D3	B	107	SM_WPDZ	I
12	NVMA7	O	44	NVMA10	O	76	MS_D2	B	108	MS_BS	O
13	NVMA12	O	45	PMOSO4	P	77	MS_D0	B	109	CF_D5	B
14	GPIO5/ SM_D5	B	46	VDD33_1	P	78	SM_CDZ	I	110	CF_D13	B
15	GPIO6/ SM_D6	B	47	SD_WP	I	79	DGND_3	P	111	SD_CLK	O
16	CF_D11	B	48	SD_CDZ	I	80	CF_D0	B	112	SD_CMD	B
17	CF_D12	B	49	SM_WEZ	O	81	CF_D1	B	113	PMOSO3	P
18	GPIO9 SM_D0	B	50	SM_RBZ	I	82	CF_D2	B	114	VDD33_3	P
19	GPIO12/ SM_D3	B	51	DGND_2	P	83	NVMD3	B	115	DGND_4	P
20	AVDD1_1	P	52	NVMOEZ	O	84	NVMD2	B	116	CF_D6	B
21	AVDD1_2	P	53	NVMA11	O	85	NVMD1	B	117	CF_D7	B
22	RREF	A	54	NVMA9	O	86	NVMD0	B	118	SD_D3	B
23	AGND1_1	A	55	NVMA8	O	87	PMOSO2	P	119	SD_D2	B
24	AGND1_2	A	56	MS_CLK	O	88	VDD33_2	P	120	NC	—
25	DM	A	57	SM_WPZ	B	89	MS_D1	B	121	NVMA2	O
26	DP	A	58	GPIO11/ SM_D2	B	90	MS_INS	I	122	NVMA3	O
27	AVDD1_3	P	59	NVMA13	O	91	SM_CLE	O	123	PMOSO1	P
28	NC	—	60	GPIO3/ MMC_D7	B	92	CF_D8	B	124	VDD33_4	P
29	AGND1_3	A	61	GPIO4/ SM_D4	B	93	CF_D9	B	125	NVMD5	B
30	DGND_1	P	62	GPIO14	B	94	CF_D10	B	126	NVMD4	B
31	NC	—	63	CF_A2	O	95	GPIO1/ MMC_D5	B	127	GPIO0/ MMC_D4	B
32	NC	—	64	CF_A1	O	96	GPIO2/ MMC_D6	B	128	GPIO7/ SM_D7	B

Note: For NC pins, please leave them unconnected (floating).

3.3 Pin Descriptions

Table 3.2 - Pin Descriptions

Pin Name	Pin#	Type	Description
CF_CS0Z	1	O	CF CS0#
CF_CS1Z	2	O	CF_CS1#
CF_IORZ	3	O	CF IOR#
CF_IOWZ	4	O	CF IOW#
NVMA0~15	98,99,121, 122,5~7,12, 55,54,44,53, 13,59,72,73	O	Ext. flash address 0~15
93C46_SK	8	O	93C46 Clock
93C46_CS	9	O	93C46 CS
xD_CDZ	11	I	xD-Picture card detection pin, normal high, active low.
GPIO0~3/ MMC_D4~7	127,95,96, 60	B	GPIO0~3 / MMC data 4~7
GPIO4~7/ SM_D4~7	61,14,15, 128	B	GPIO4~7 / SM data 4~7
GPIO9~12/ SM_D0~3	18,103,58, 19	B	GPIO9~12 / SM data 0~3
GPIO8,13~15	102,66,62, 10	B	GPIO8, 13~15
CF_D8~12	92~94,16,17	B	CF data 8~12
AVDD1_1~3	20,21,27	P	Analog power #1
RREF	22	A	Reference resistor
AGND1_1~3	23,24,29	A	Analog ground 1~3
DM	25	A	USB D-
DP	26	A	USB D+
DGND_1~4	30,51,79,115	P	Digital ground
AVDD2	33	P	Analog power #2
X2	34	B	12MHz Crystal This is the other terminal of the crystal, or left open when an external clock source is used to drive XTAL/CLK.
X1	35	I	12MHz Crystal This pin can be connected to one terminal of the crystal or can be connected to an external 12MHz clock when a crystal is not used.
AGND2	36	P	Analog ground #2
NVMWEZ	37	O	Ext. flash WE#
CF_RST	38	O	CF reset (active-low)
SM_REZ	39	O	SmartMedia RE#
SD_D0~3	67,40,119, 118,	B	SD DAT0~3
NVMD0~7	86~83,126, 125,41,42	B	Ext. flash data 0~7

NVMCSZ	43	O	Ext. flash CS#
VDD33_1~4	46,88,114, 124	P	Digital power 3.3V
SD_WP	47	I	SD Write Protect Detection, this pin is an active high write protect signal for the SD device; Default high when card inserted.
SD_CDZ	48	I	SD Card detection#, this is the card detection signal from SD device to indicate if the device is inserted, Normal high.
SM_WEZ	49	O	SmartMedia WE#
SM_RBZ	50	I	SmartMedia RDY/BSY#
NVMOEZ	52	O	Ext. flash OE#
MS_CLK	56	O	Memory Stick SCLK output.
SM_WPZ	57	B	SmartMedia WP#
CF_A0~2	65~63	O	CF address 0~2
SM_ALE	68	O	SmartMedia ALE
93C46_DO	69	O	93C46 Data out
93C46_DI	70	I	93C46 Data in
EXTRSTZ	71	I,PU	External reset #, the active low signal is used by the system to reset the chip, The active low pulse should be at least 1 us wide.
NC	28,31,32,74, 120	—	Not connected
MSD0~3	77,89,76,75	B	MS DAT0~3
SM_CDZ	78	I	SmartMedia CD#, this is the card detection signal from SM device to indicate if the device is inserted, active low.
CF_D0~7,13	80~82,104, 105,109, 116,117,110	B	CF Data 0~7, 13
PMOSO1	123	P	PMOS1: SM/XD Power MOS output (250mA output for idea)
PMOSO2	87	P	PMOS2: MS Power MOS output(250mA output for idea)
PMOSO3	113	P	PMOS3: SD Power MOS output(250mA output for idea)
PMOSO4	45	P	PMOS4: CF Power MOS output(250mA output for idea) or Access LED
MS_INS	90	I	Memory Stick INS
SM_CLE	91	O	SmartMedia CLE
IORDY	97	I	CF IORDY
CF_D14~15	100,101	B	CF data 14~15
CF_CDZ	106	I	CF CD# . CF card detection, this pin is connected to the ground on the CF card, when the CF device is inserted.
SM_WPDZ	107	I	SmartMedia Write Protect Detect, this pin is an active low write protect signal for the SM device, when SM is enable. Normal high.
MS_BS	108	O	MemoryStick BS
SD_CLK	111	O	SD/MMC CLK
SD_CMD	112	B	SD/MMC CMD

Note:

Type	**O**	Output
	I	Input
	B	Bi-directional
	IPU	Input with internal pull-up
	IPD	Input with internal pull-down
	P	Power / Ground
	A	Analog

CHAPTER 4 BLOCK DIAGRAM

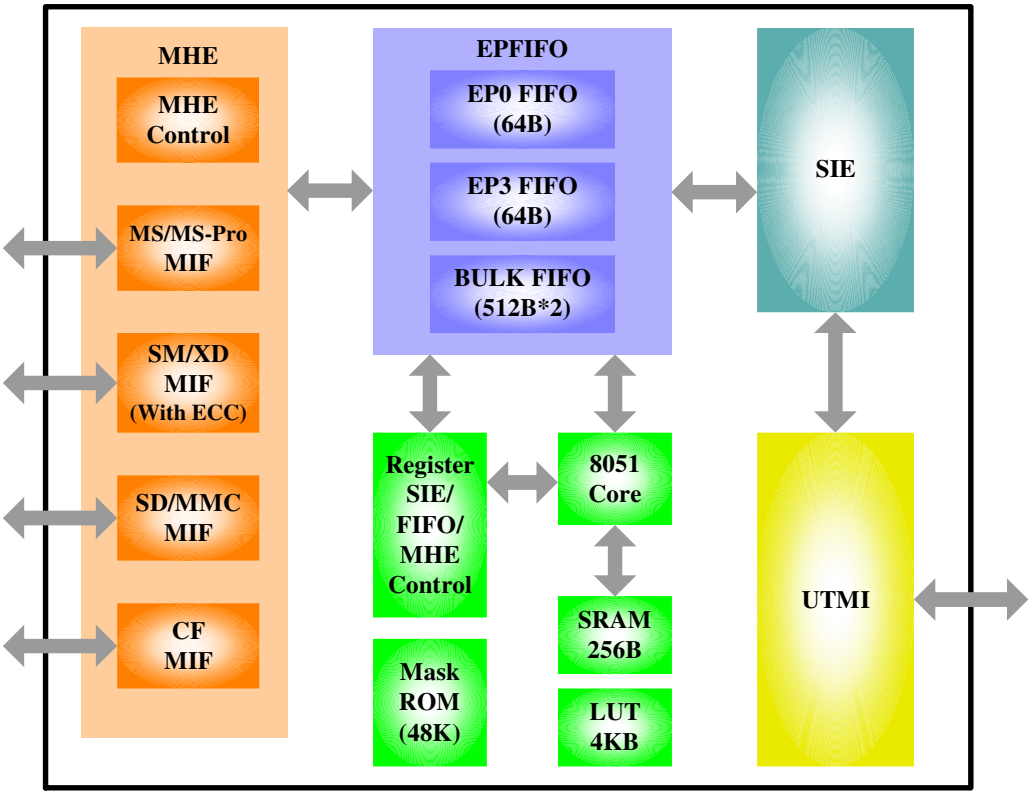


Figure 4.1 - Block Diagram

CHAPTER 5 FUNCTIONAL DESCRIPTION

UTMI

The USB 2.0 Transceiver Macrocell, it's the analog circuitry that handles the low level USB protocol and signaling, and shifts the clock domain of the data from the USB 2.0 rate to one that is compatible with the general logic.

SIE

The Serial Interface Engine, which contains the USB PID and address recognition logic, and other sequencing and state machine logic to handle USB packets and transactions.

EPFIFO

Endpoint FIFO includes Control FIFO (FIFO0), interrupt FIFO (FIFO3), Bulk In/Out FIFO (BULKFIFO)

- **Control FIFO** FIFO of control endpoint 0.
  It is 64-byte FIFO, and it is used for endpoint 0 data transfer.
- **Interrupt FIFO** 64-byte depth FIFO of endpoint 3 for status interrupt
- **Bulk In/Out FIFO** It can be in the TX mode or RX mode:
  1. It contains ping-pong FIFO (512 bytes each bank) for transmit/receive data continuously.
  2. It can be directly accessed by Uc
  3. Support automatic hardware SmartMedia ECC error correction

MHE

It contains 5 MIF (Media Interface)

- **MIFs**
  1. CF/Micro Drive MIF
  2. SmartMedia/xD/Flash MIF
  3. SD/MMC MIF
  4. MemoryStick MIF
  5. MemoryStick PRO MIF

8051 Core/SRAM/LUT/Mask ROM

An 8-bit Micro-controller to manage card operation, card power, USB Storage Class, data transfer between USB and card interface, and GPIOs control

CHAPTER 6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

Table 6.1 - Absolute Maximum Ratings

Parameter	Value
Storage Temperature	-40°C to + 125°C
Ambient Temperature	0°C to + 70°C
Supply Voltage to Ground Potential	-0.5V to + 4.0V
DC Input Voltage to Any Pin	-0.5V to + 5.8V

6.2 Operating Conditions

Table 6.2 - Operating Conditions

Parameter	Value
Ta (Ambient Temperature Under Bias)	0°C to 70°C
Supply Voltage	+3.0V to +3.6V
Ground Voltage	0V
F_{OSC} (Oscillator or Crystal Frequency)	12 MHz ± 0.05% 12 MHz ± 0.25% (for USB full-speed only)

6.3 DC Characteristics

Table 6.3 - DC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		3.0	-	3.6	V
V_{IH}	Input High Voltage		2.0	-	3.6	V
V_{IL}	Input Low Voltage		-0.3	-	0.8	V
I_I	Input Leakage current	0 < VIN < VCC (The value is under without the pull-up or pull-down resistance, It means it is the value that the pin state is Hi-z)	-10	-	10	µA
V_{OH}	Output High Voltage		2.4	-	-	V
V_{OL}	Output Low Voltage		-	-	0.4	V
I_{OH}	Output Current High	VDD=3.3V V_{OH}=2.4V	-	8	-	mA
I_{OL}	Output Current Low	VDD=3.3V V_{OL}=0.4V	-	8	-	mA
I_{SUSP}	Suspend current	1.5K external pull-up included	-	-	450	µA
I_{CC}	Supply current	Connect to USB with 8051 operating without the card	-	-	90	mA

6.4 PMOS Characteristics

Before over-current dectection:

Table 6.4 - PMOS Driving Strength versus Junction Temperature

(IO Power=3.3V, Register setting =250mA)

Junction Temperature	70 °C	25 °C	0 °C
Max. Driving Strength (Ma), PMOS output voltage(V)	190± 20% 2.81v± 5%	202± 20% 2.84V± 5%	218 ± 20% 2.85v± 5%

When over-current dectection:

Table 6.5 - PMOS Driving Strength versus Junction Temperature

(IO Power=3.3V, Register setting =250mA)

Junction Temperature	70 °C	25 °C	0 °C
Max. Driving Strength (Ma), PMOS output voltage(V)	198± 20% 2.8v± 5%	215± 20% 2.83V± 5%	232 ± 20% 2.84v± 5%

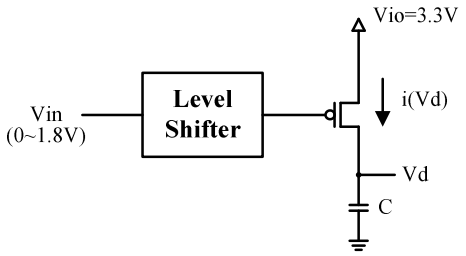


Figure 6.1 - Embedded PMOS Switch Architecture

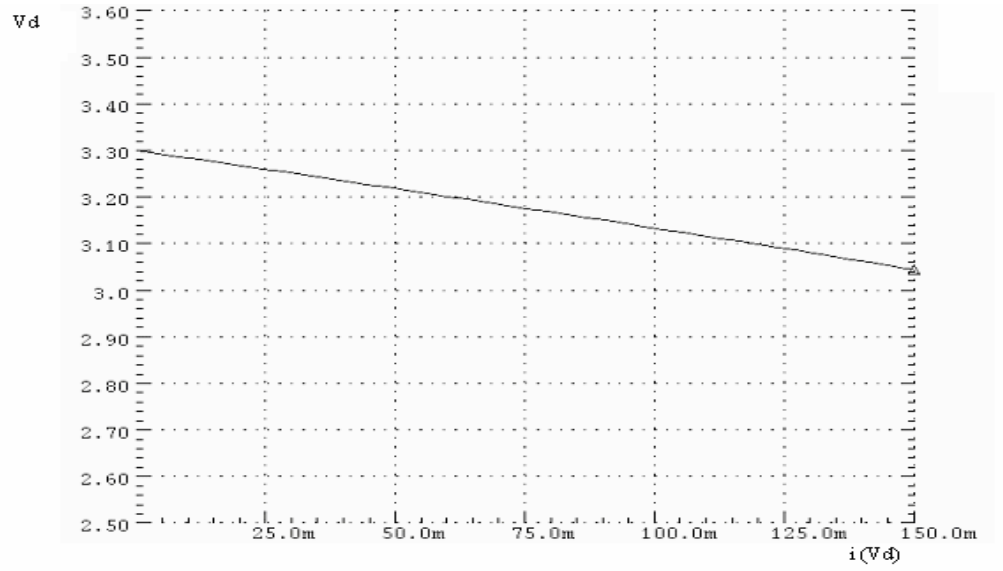


Figure 6.2 – V-I Curve of PMOS Switch @ 25 °C

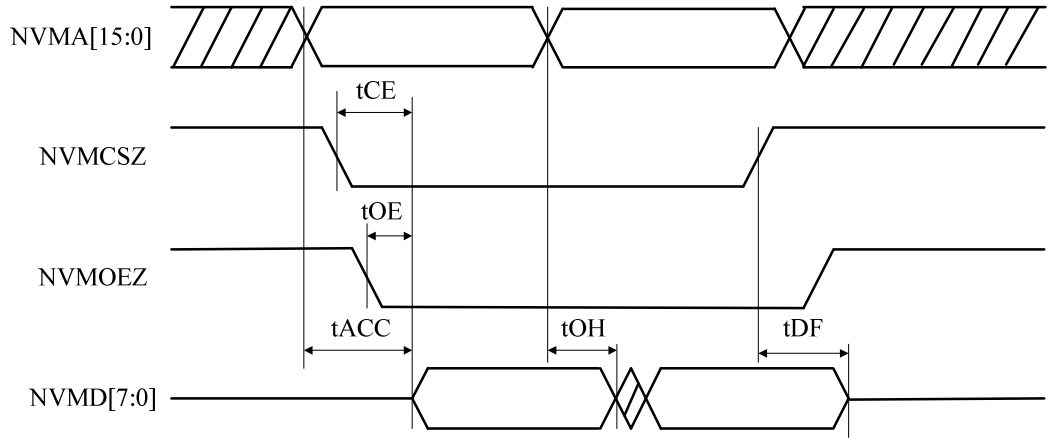
6.5 AC Characteristics

6.5.1 UTMI Transceiver

The GL819 is fully compatible with Universal Serial Bus specification rev. 2.0 and USB 2.0 Transceiver Macercell Interface (UTMI) specification rev. 1.01. Please refer to the specifications for more information.

6.5.2 External Flash

Read Cycle



Program Cycle

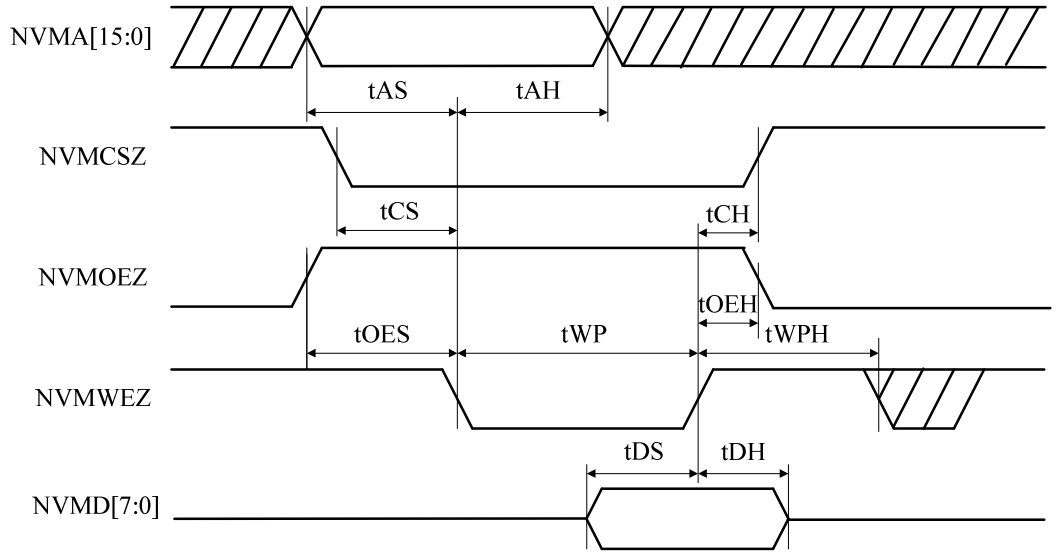


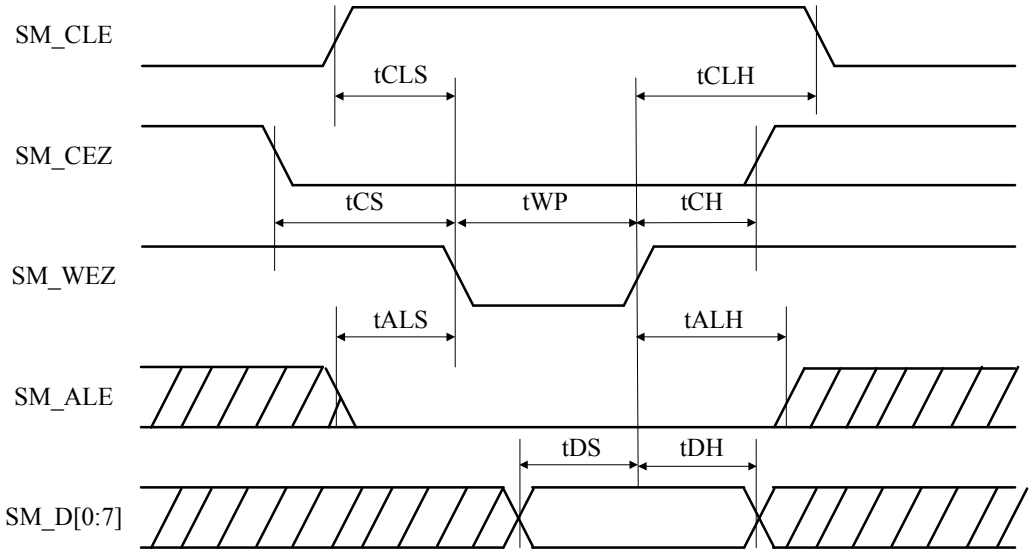
Figure 6.3 - Timing Diagram of External Flash

AC Characteristics of Flash Interface (C_{LOAD} = 30pF)

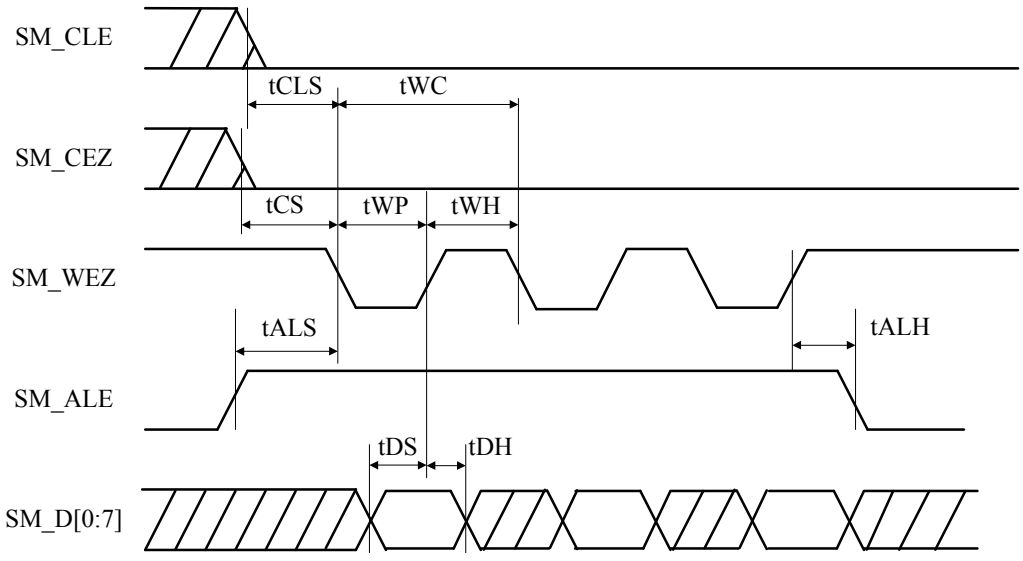
Symbol	Parameter	Max	Unit
tACC	Address to Output Delay (max)	83	ns
tCE	NVMCSZ to Output Delay (max)	83	
tDF	NVMCEZ or NVMOEZ, whichever occurred first, to Output Float (max)	0	
tOH	Output Hold from NVMOEZ, NVMCSZ or Address, whichever occurred first (min)	0	
tAS	Address Setup Time (min)	760	
tAH	Address Hold Time (min)	760	
tOES	NVMOEZ Setup Time (min)	300	
tCS	NVMCSZ Setup Time (min)	0	
tCH	NVMCSZ Hold Time (min)	0	
tWP	Write Pulse Width (min)	66	
tWPH	Write Pulse Width High (min)	300	
tDS	Data Setup Time (min)	300	
tDH	Data Hold Time (min)	0	
tOEH	NVMOEZ Hold Time (min)	16	

6.5.3 SmartMedia

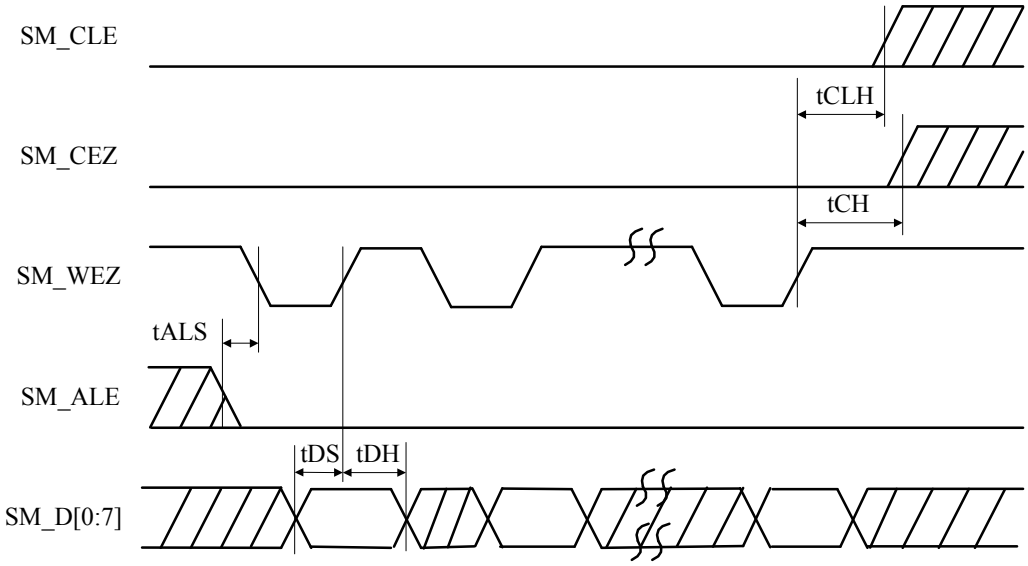
Command Input Cycle



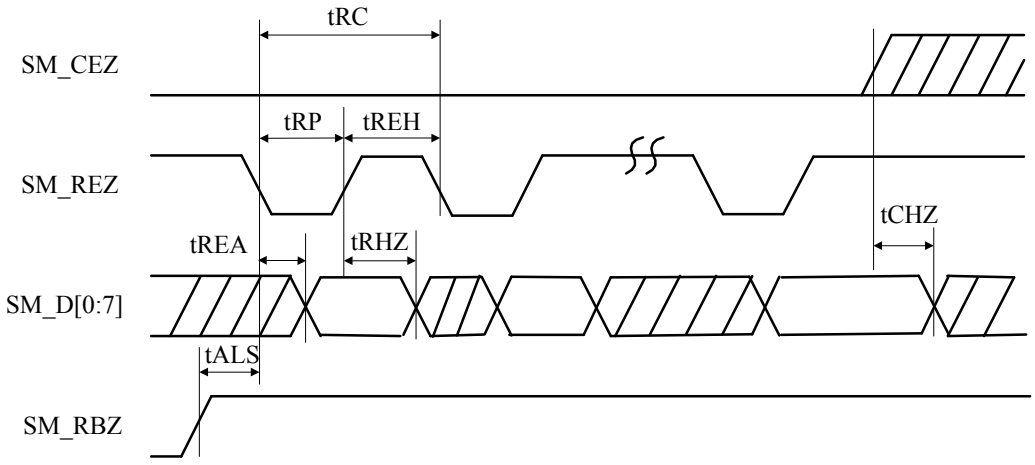
Address Input Cycle



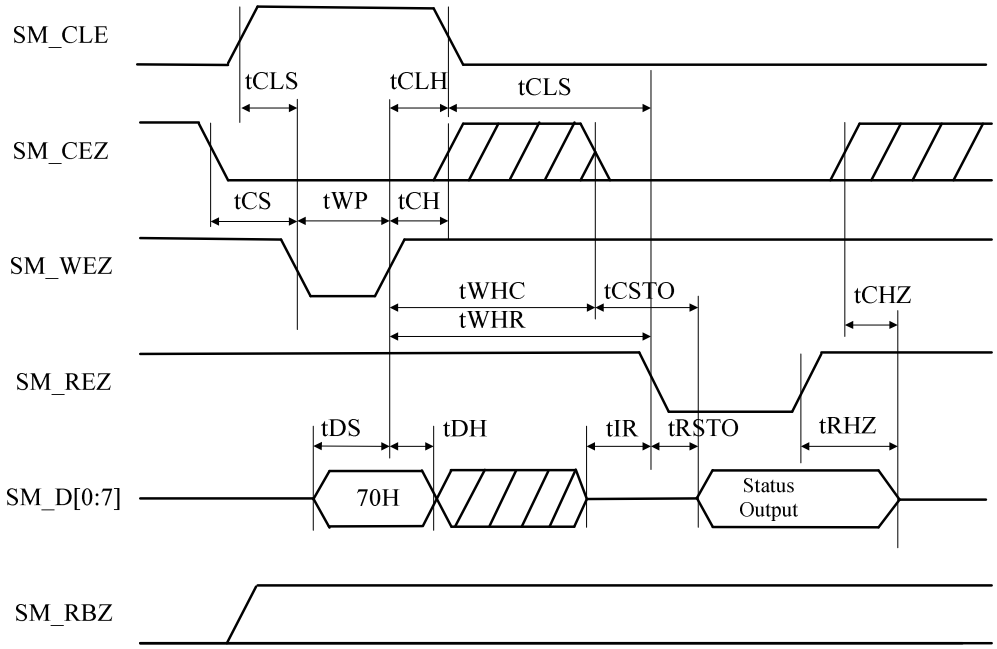
Data Input Cycle



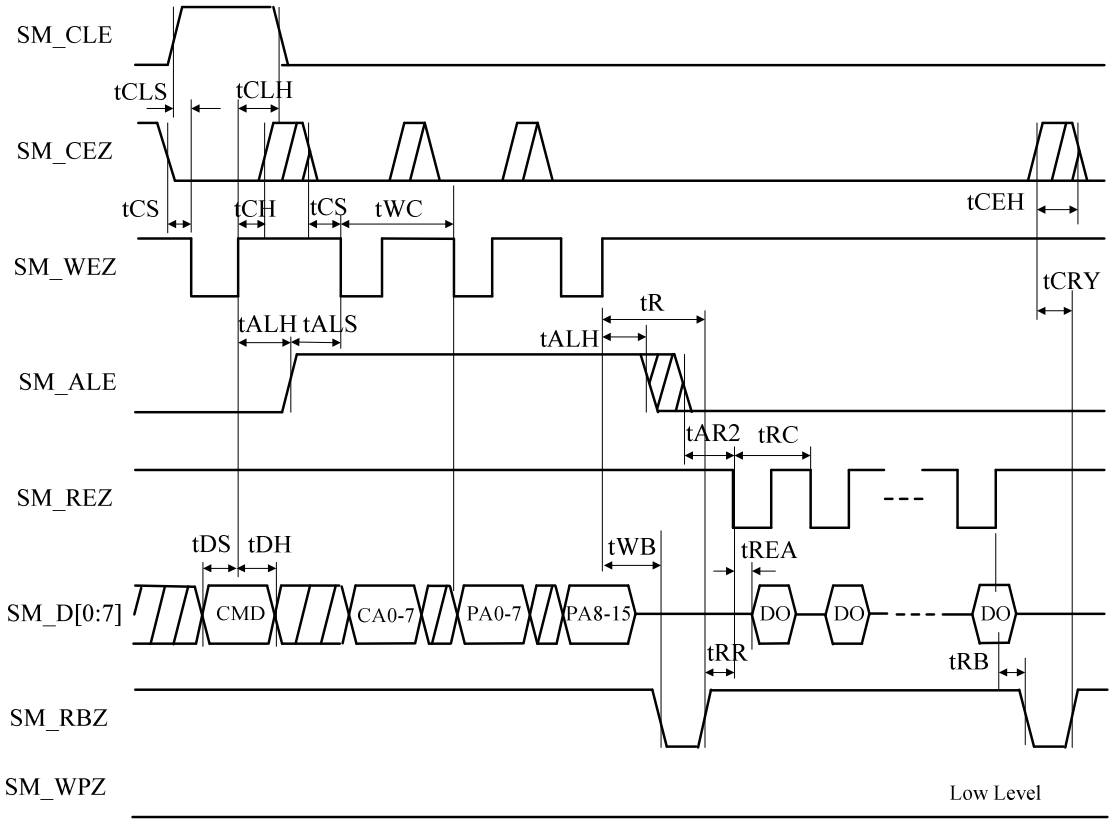
Serial Read Cycle



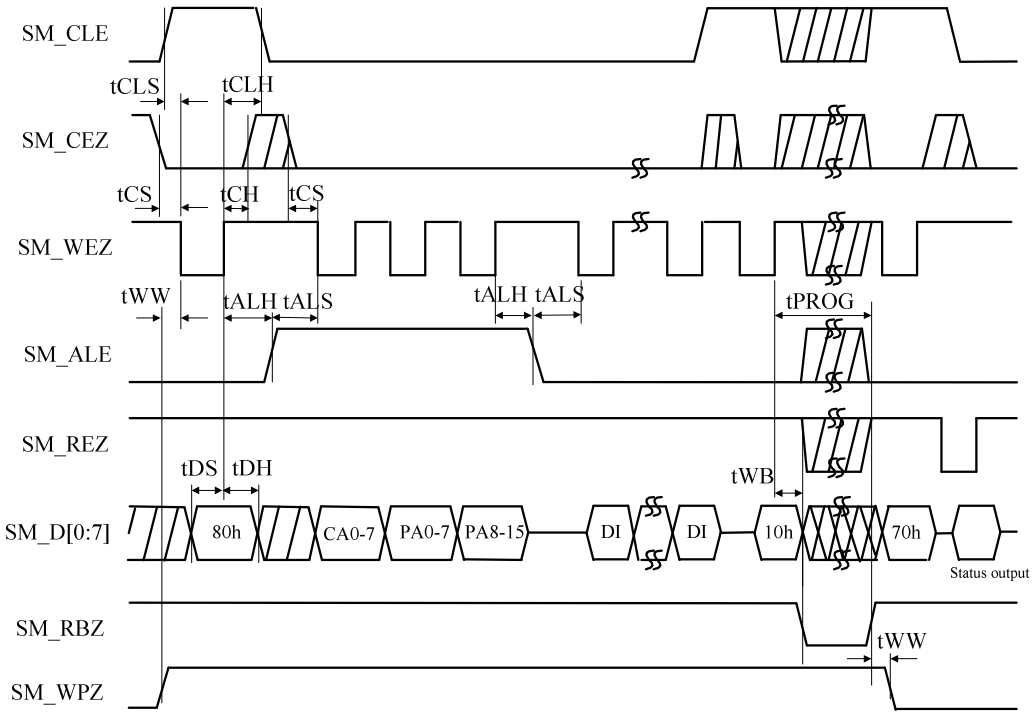
Status Read Cycle



Read Cycle



Auto Page Program Timing



ID Read Timing

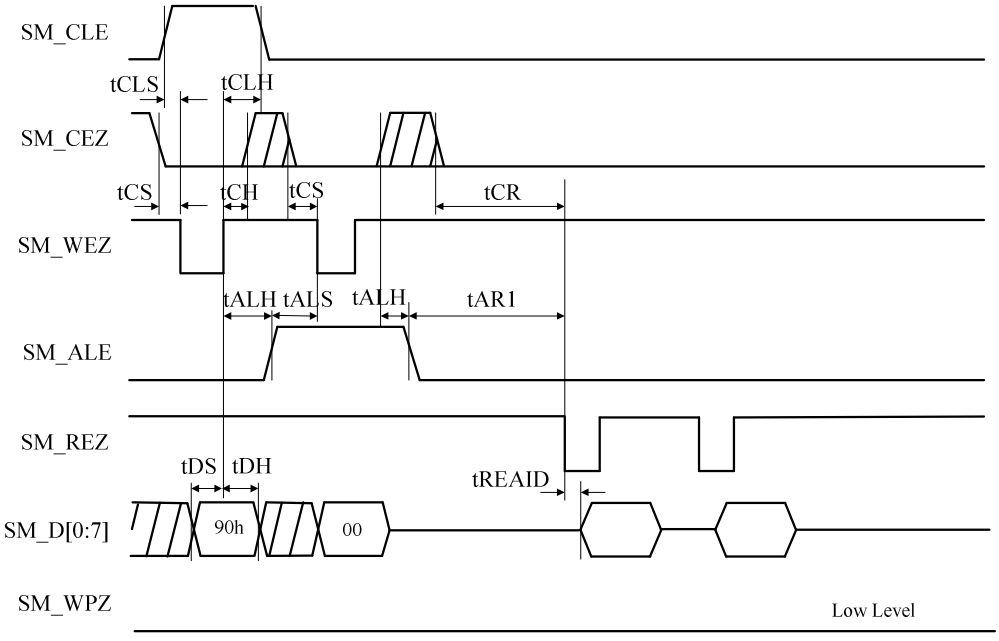


Figure 6.4 - Timing Diagram of SmartMedia

AC Characteristics of Smart Media Interface (C_{LOAD} = 30 pF)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
tCLS	CLE Setup Time	35	-	ns
tCLH	CLE Hold Time	45	-	ns
tCS	-CE Setup Time	160	-	ns
tCH	-CE Hold Time	160	-	ns
tWP	-WE Pulse Width	50	-	ns
tALS	ALE Setup Time	35	-	ns
tALH	ALE Hold Time	79	-	ns
tDS	Data Setup Time	48	-	ns
tDH	Data Hold Time	35	-	ns
tWC	Write Cycle Time	83	-	ns
tWH	-WE High Hold Time	33	-	ns
tWW	-WP High to –WE Low	199	-	ns
tRR	Ready to –RE Low	216	-	ns
tRP	Read Pulse Width	67	-	ns
tRC	Read cycle Time	100	-	ns
tREA	-RE Access Time (Serial Data Access)	-	25	ns
tCEH	-CE High Hold Time (At the Last Serial Read)	400	-	ns
tREAID	-RE Access Time (ID Read)	-	25	ns
tRHZ	-RE High to Output Hi-Z	10	15	ns
tCHZ	-CE High to Output Hi-Z	-	10	ns
tREH	-RE High Hold Time	30	-	ns
tRSTO	-RE Access Time	-	42	ns
tCSTO	-CE Access Time	-	42	ns
tRHW	-RE High to -WE Low	36	-	ns
tWHC	-WE High to –CE Low	160	-	ns
tWHR	-WE High to –RE Low	83	-	ns
tAR1	ALE Low to –RE Low (Address Register Read, ID Read)	330	-	ns
tCR	-CE Low to –RE Low (Data Register Read, ID Read)	235	-	ns
tWB	-WE High to Busy	-	100	ns
tAR2	ALE Low to RE Low (Read Cycle)	330		ns
tRB	Last –RE High to Busy (at Sequential Read)	-	32	ns
tCRY	-CE High to Ready	-	1	µs

6.5.4 xD

The Timing diagrams are the same as SM.

AC Characteristics:

Parameter	Description	Spec. Min	Spec. Max	GL819 (30pF)	Unit
tCLS	CLE Set up Time	20		35.2	ns
tCLH	CLE Hold Time	40		44.6	
tCS	CE Setup up Time	20		163.5	
tCH	CE Hold Time	40		163.5	
tWP	WE Pulse Width	40		51.9	
tALS	ALE Setup Time	20		35.2	
tALH	ALE Hold Time	40		95.2	
tDS	Data Setup Time	30		51.9	
tDH	Data Hold Time	20		35.5	
tWC	Write Cycle Time	80		83.2	
tWH	WE High Hold Time	20		31.7	
tWW	WP High to WE Low	100		199	
tRR	Ready to RE Low	20		232	
tRP	Read Pulse Width	60		68.6	
tRC	Read Cycle Time	80		100	
tREA	RE Access Time(Serial Data Access)		45	25	
tCEH	CE High Hold Time	250		400	
tREAID	RE Access Time(ID Read)		90	25	
tRHZ	RE High to Output Hi-Z	5	30	26.9	
tCHZ	CE High to Output Hi-Z		30	26.9	
tREH	RE High Hold Time	20		31.2	
tRSTO	RE Access Time		45	10	
tCSTO	CE Access Time		55	10	
tRHW	RE High to WE Low	0		35.2	
tWHC	WE High to CE Low	50		163	
tWHR	WE High to RE Low	60		83	
TAR1	ALE Low to RE Low	200		366	
tCR	CE Low to RE Low	200		235	
tWB	WE High to Busy		200	100	
TAR2	ALE LOW to RE LOW	150		352	
tRB	Last RE High to Busy		200	48	

6.5.5 Memory Stick

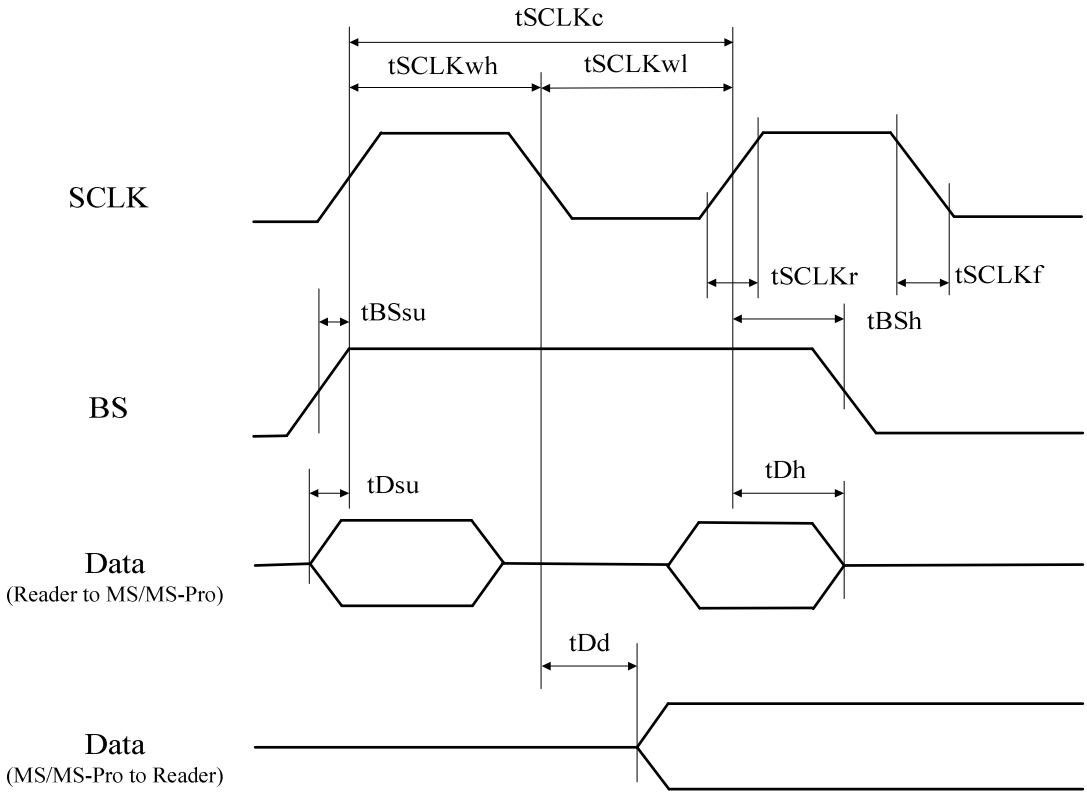


Figure 6.5 - Timing Diagram of MemoryStick

Memory Stick Frequency Mode

Parameter	Description	Mode	Typ	Unit	Remark
F_{SCLK}	SCLK frequency	0	1.5M	Hz	
		1	6M		
		2	15M		
		3	20M		

AC Characteristics of Memory Stick Interface (C_{LOAD} = 30 pF)

PARAMETER	DESCRIPTION	F_{SCLK} = 1.5 MHZ	F_{SCLK} = 6 MHZ	F_{SCLK} = 15 MHZ	F_{SCLK} = 20 MHZ	UNIT
tSCLKc	SCLK Cycle	666.6	166.6	66.6	50.0	ns
tSCLKwh	SCLK H pulse length (min)	323.3	73.3	23.3	15	ns
tSCLKwl	SCLK L pulse length (min)	323.3	73.3	23.3	15	ns

tSCLKr	SCLK rise time (min)	5	5	5	5	ns
tSCLKr	SCLK rise time (max)	10	10	10	10	ns
tSCLKf	SCLK Fall time (min)	5	5	5	5	ns
tSCLKf	SCLK Fall time (max)	10	10	10	10	ns
tBSsu	BS setup time (min)	5	5	5	5	ns
tBSh	BS hold time (min)	5	5	5	5	ns
tDsu	DATA setup time (min)	5	5	5	5	ns
tDh	DATA hold time (min)	5	5	5	5	ns
tDd	DATA output delay time (max)	5	5	5	5	ns

6.5.6 Memory Stick PRO

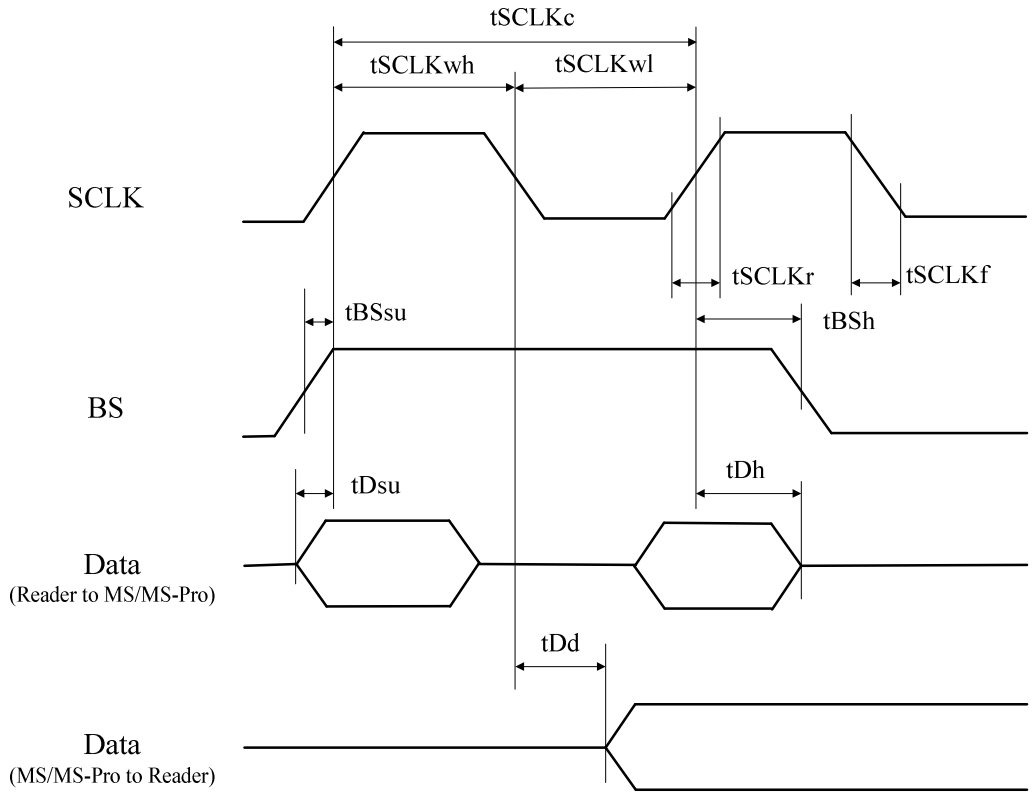


Figure 6.6 - Timing Diagram of MemoryStick PRO

Memory Stick PRO Frequency Mode

Parameter	Description	Mode	Typ	Unit	Remark
F_{SCLK}	SCLK frequency	0	1.5M	Hz	Same as Memory Stick
		1	6M		
		2	15M		
		3	20M		
		4	30M		
		5	40M		

AC Characteristics of MS Interface (C_{LOAD} = 15 pF)

PARAMETER	DESCRIPTION	F_{SCLK} = 30 MHZ	F_{SCLK} = 40 MHZ	UNIT
tSCLKc	SCLK Cycle	33.3	25.0	ns
tSCLKwh	SCLK H pulse length (min)	9	5	ns
tSCLKwl	SCLK L pulse length (min)	9	5	ns
tSCLKr	SCLK rise time (min)	5	5	ns
tSCLKr	SCLK rise time (max)	7.5	7.5	ns
tSCLKf	SCLK Fall time (min)	5	5	ns
tSCLKf	SCLK Fall time (max)	7.5	7.5	ns
tBSsu	BS setup time (min)	8	8	ns
tBSh	BS hold time (min)	1	1	ns
tDsu	DATA setup time (min)	8	8	ns
tDh	DATA hold time (min)	1	1	ns
tDd	DATA output delay time (max)	5	5	ns

6.5.7 Secure Digital / MultiMedia Card

Normal Mode:

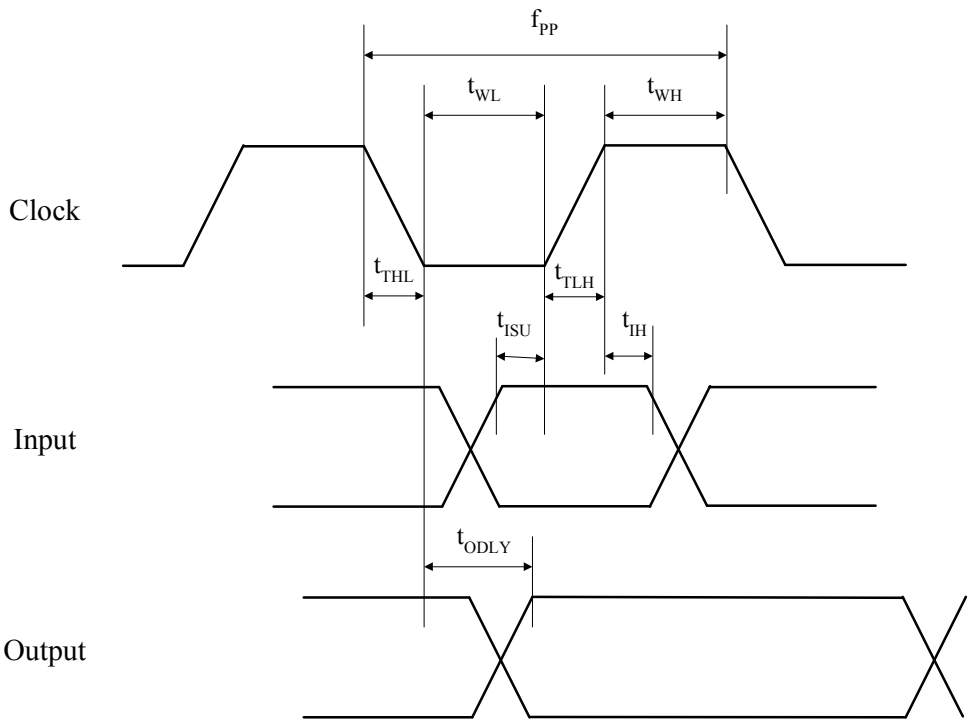
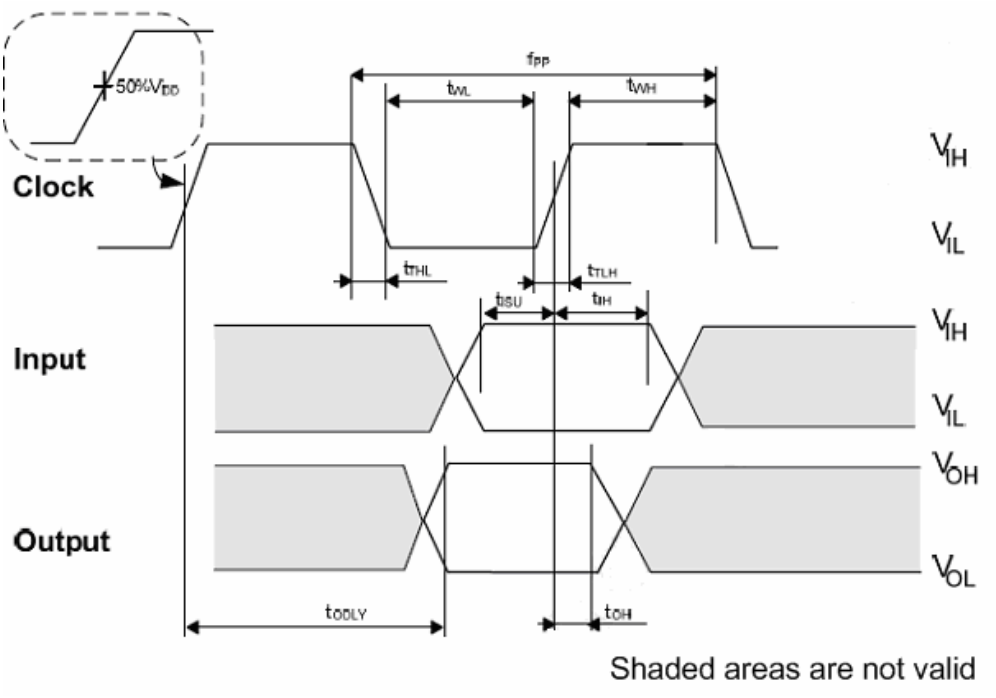


Figure 6.7 - Timing Diagram of Secure Digital / MultiMedia Card

SD Interface Timing (C_L = 30PF)

SYMBOL	PARAMETER	CLOCK RATE				UNIT
f_{PP}	Clock frequency Data Transfer Mode	24	20	15	6	MHz
f_{OD}	Clock frequency Identification Mode	375	375	375	375	KHz
t_{WL}	Clock low time (min)	18	22	30	80	ns
t_{WH}	Clock high time (min)	18	22	30	80	ns
t_{TLH}	Clock rise time (max)	3	3	3	3	ns
t_{THL}	Clock fall time (max)	3	3	3	3	ns
t_{ISU}	Input set-up time (min)	5	5	5	5	ns
t_{IH}	Input hold time (min)	5	5	5	5	ns
t_{ODLY}	Output delay time (max)	14	14	14	14	ns

High-Speed Mode:



High-Speed Mode:

SD Interface Timing (C_L = 30PF)

SYMBOL	PARAMETER	CLOCK RATE	UNIT
f_{PP}	Clock frequency Data Transfer Mode	48	MHz
f_{OD}	Clock frequency Identification Mode	375	KHz
t_{WL}	Clock low time (min)	7.4	ns
t_{WH}	Clock high time (min)	7.4	ns
t_{TLH}	Clock rise time (max)	3	ns
t_{THL}	Clock fall time (max)	3	ns
t_{ISU}	Input set-up time (min)	6	ns
t_{IH}	Input hold time (min)	2	ns
t_{ODLY}	Output delay time (max)	14	ns

6.5.8 CompactFlash Card

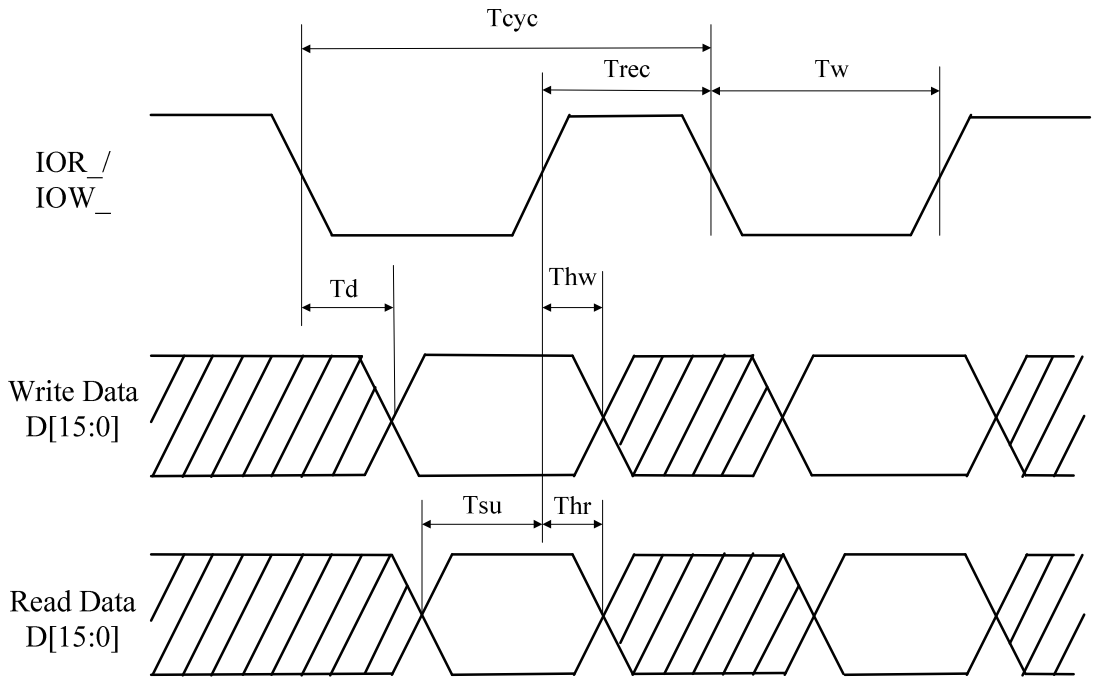


Figure 6.8 - Timing Diagram of CompactFlash

True IDE PIO Mode Read/Write Timing (with C_{LOAD} = 30 pF)

PARAMETER	ITEM	MODE 0	MODE 1	MODE 2	MODE 3	MODE 4	MODE 5	MODE 6	UNITS
Tcyc	Cycle Time (min)	600	399	249	183	133	100	83	ns
Tw	Read/Write Active Width (min)	399	266	150	100	83	66	58	ns
Trec	Read/Write Recovery Time (min)	199	132	99	83	49	33	24	ns
Td	Write Data Setup (min)	0	0	0	0	0	0	0	ns
Twh	Write Data Hold (min)	208	142	109	90	55	40	24	ns
Tsu	Read Data Setup (min)	50	35	20	20	20	15	10	ns
Thr	Read Data Hold (min)	5	5	5	5	5	5	5	ns

6.5.9 EEPROM 93C46 Timing

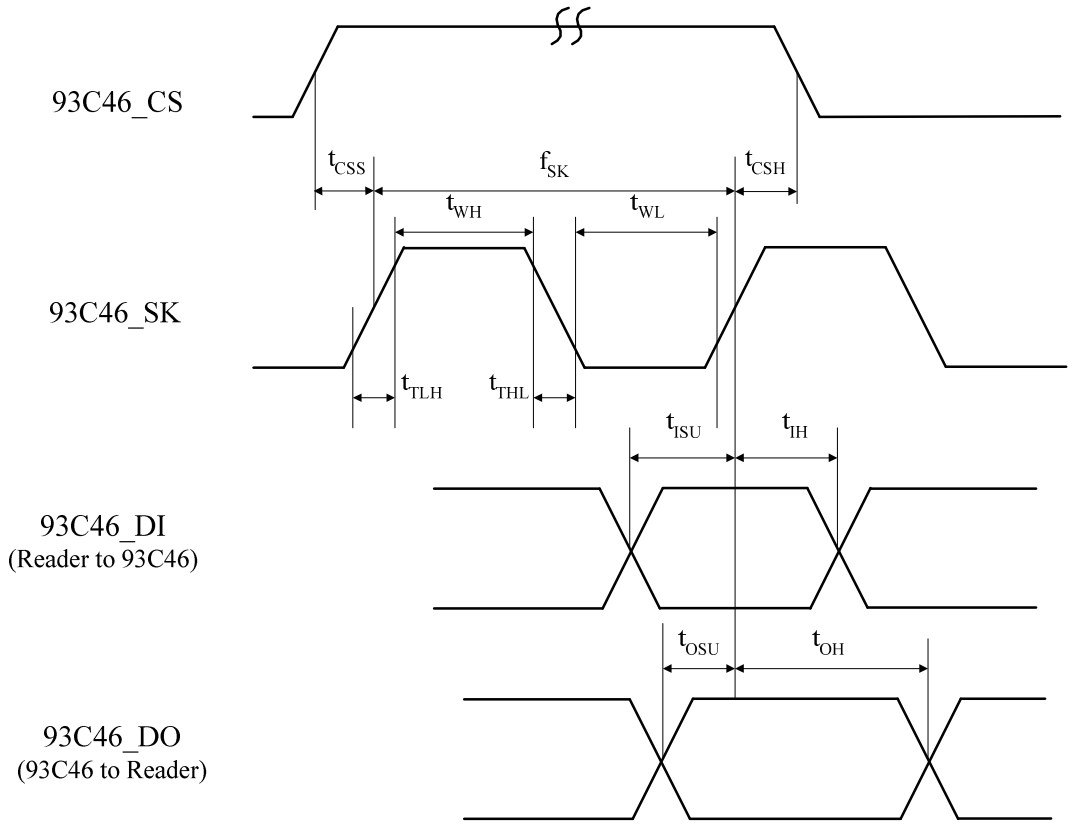
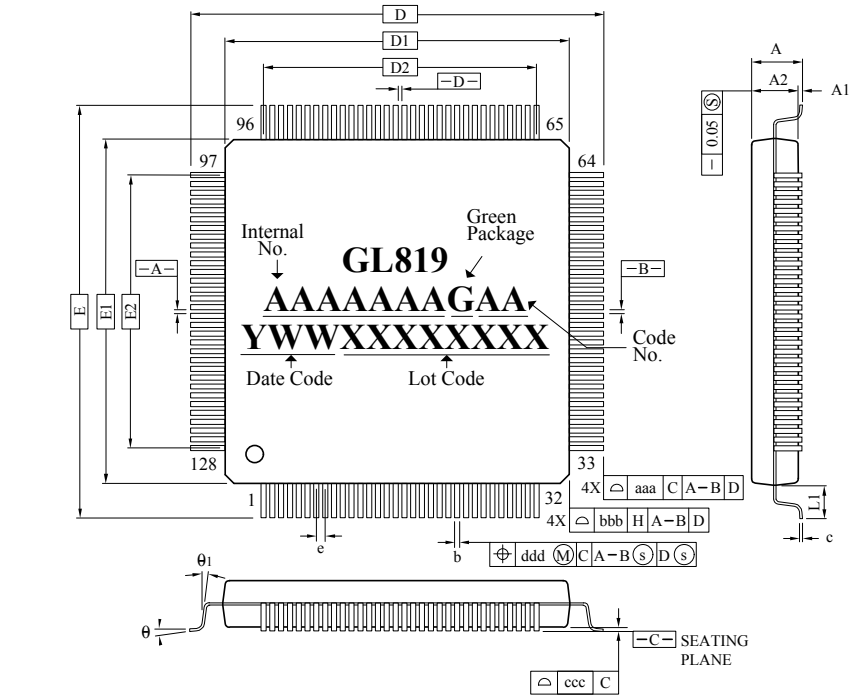


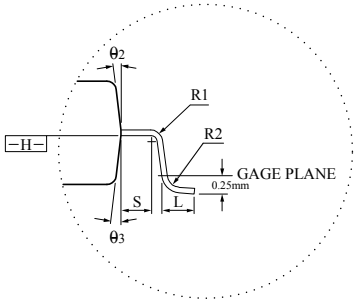
Figure 6.9 - Timing Diagram of EEPROM 93C46

AC Characteristics of 93C46 Interface (with C_{LOAD} = 15 pF)

PARAMETER	DESCRIPTION	MINIMUM	MAXIMUM	UNIT
f_{SK}	SK clock frequency	200k	400k	Hz
t_{WH}	SK H pulse length	500	—	ns
t_{WL}	SK L pulse length	500	5	ns
t_{TLH}	SK rise time	—	10	ns
t_{THL}	SK fall time	—	10	ns
t_{CSS}	CS setup time	1	—	µs
t_{CSH}	CS hold time	1	—	µs
t_{ISU}	DI setup time	1	—	µs
t_{IH}	DI hold time	1	—	µs
t_{OSU}	DO setup time	5	—	ns
t_{OH}	DO hold time	5	—	ns

CHAPTER 7 PACKAGE DIMENSION





NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BASIC			0.630 BASIC		
E	16.00 BASIC			0.630 BASIC		
D1	14.00 BASIC			0.551 BASIC		
E1	14.00 BASIC			0.551 BASIC		
D2	12.40 BASIC			0.488 BASIC		
E2	12.40 BASIC			0.488 BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0	3.5	7	0	3.5	7
θ1	0	—	—	0	—	—
θ2	11	12	13	11	12	13
θ3	11	12	13	11	12	13
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BASIC			0.016 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

Figure 7.1 - GL819 128 Pin LQFP Package

CHAPTER 8 ORDERING INFORMATION

Table 8.1 - Ordering Information

Part Number	Package	Normal/Green	Version	Status
GL819MXG	128-pin LQFP	Green Package	11/13	Available