

AZ100LVEL16VV



Dual Frequency PECL/ECL Oscillator Gain Stage & Buffer with Enable

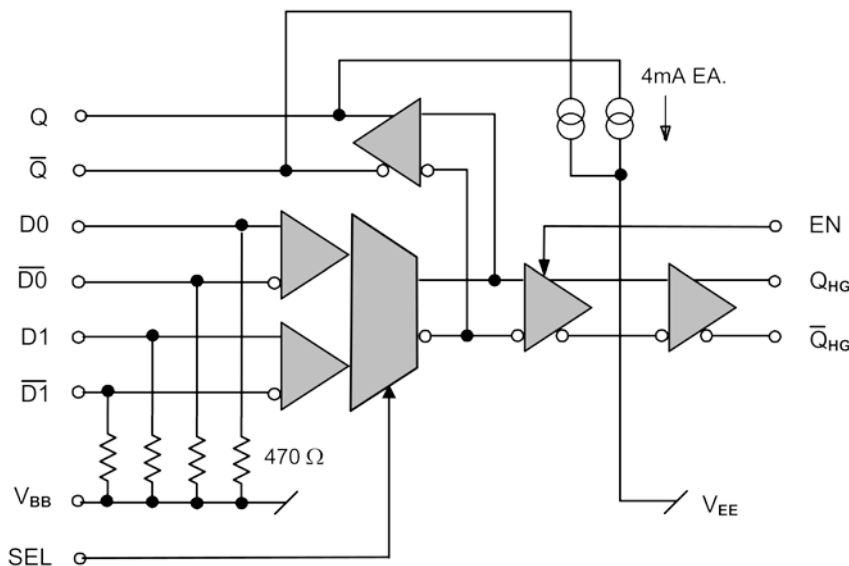
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DESCRIPTION

The [AZ100LVEL16VV](#) is a specialized oscillator gain stage with two selectable data input pairs and a high gain output buffer including an enable. Selectable data input pairs permit switching between two different oscillator frequencies. The Q_{HG}/\bar{Q}_{HG} outputs have a voltage gain several times greater than the Q/\bar{Q} outputs. An enable allows continuous oscillator operation by only controlling the Q_{HG}/\bar{Q}_{HG} outputs.

The AZ100LVEL16VV also provides a reference voltage (V_{BB}) with internal biasing resistors to each input to minimize external components.

BLOCK DIAGRAM



FEATURES

- Minimizes External Components
- High Bandwidth for $\geq 1\text{GHz}$
- Similar Operation as [AZ100LVEL16VR](#) except with selectable data input pairs
- -147 dBc/Hz Typical Noise Floor

APPLICATIONS

- Dual frequency oscillators
- Crystal or saw oscillators that require minimal external components.

PACKAGE AVAILABILITY

- MLP16
 - Green/RoHS Compliant/Pb-Free

Order Number	Package	Marking
AZ100LVEL16VRL ¹	MLP16	AZM+16K <Date Code> ²

¹ [Tape & Reel](#) - Add 'R1' at end of PN for 7in (1k parts), 'R2' (2.5k) for 13in

² See www.azmicrotek.com for [date code format](#)

PIN DESCRIPTION AND CONFIGURATION

Table 1 - Pin Description AZ100LVEL16VTNA+

Pin	Name	Type	Function
1	D0	Input	Data Input
2	$\overline{D0}$	Input	Inverting Data Input
3	D1	Input	Data Input
4	$\overline{D1}$	Input	Inverting Data Input
5	V_{BB}	Output	Reference Voltage
6	NC	-	N/A
7	V_{EE}	Power	Negative Supply
8	NC	-	N/A
9	EN	Input	Output Enable
10	Q_{HG}	Output	High Gain Inverting PECL Output
11	Q_{HG}	Output	High Gain PECL Output
12	SEL	Input	Data Input Select
13	V_{CC}	Power	Positive Supply
14	NC	-	N/A
15	Q	Output	PECL Output
16	\overline{Q}	Output	Inverting PECL Output

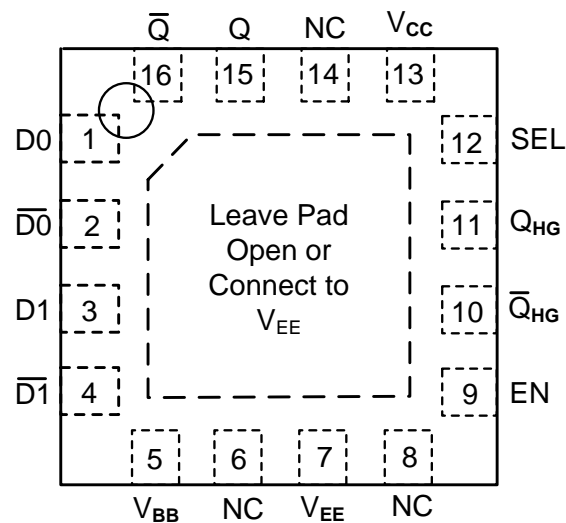


Figure 1 - Pin Configuration

ENGINEERING NOTES

The data inputs are selected with the select pin (SEL). When SEL is LOW or open (NC) data from the D0/D $\bar{0}$ is selected. When SEL is HIGH data from the D1/D $\bar{1}$ is selected. See Table 2 for data selection.

The enable pin (EN) works with either data input pair. When EN is HIGH or open (NC), input data is passed to both sets of outputs. When EN is LOW, the Q_{HG}/Q_{HG} outputs will be forced LOW/HIGH respectively, while input data will continue to be passed to the Q/Q outputs. The EN and SEL inputs can be driven with an ECL/PECL signal or a full supply swing CMOS type logic signal. See table 2 for enable operation.

Internal Input biasing is accomplished with a V_{BB} and separate 470 Ω bias resistors connecting each data input to V_{BB}. The V_{BB} pin supports 1.5mA sink/source current and should be bypassed to ground with a 0.01 μ F capacitor.

Each Q/Q output has a 4 mA on-chip pull-down current source. External resistors may also be used to increase pull-down current of the Q/Q to a maximum of 25mA each (includes a 4 mA on-chip current source).

NOTE: Specifications in the ECL/PECL tables are valid when thermal equilibrium is established.

Table 2 - Truth Table

EN	CS-SEL	Q	Q	Q _{HG}	Q _{HG}
High/Open	Low/Open	D0/D $\bar{0}$	D0/D $\bar{0}$	D0/D $\bar{0}$	D0/D $\bar{0}$
High/Open	High	D1/D $\bar{1}$	D1/D $\bar{1}$	D1/D $\bar{1}$	D1/D $\bar{1}$
Low	Low/Open	D0/D $\bar{0}$	D0/D $\bar{0}$	Low	High
Low	High	D1/D $\bar{1}$	D1/D $\bar{1}$	Low	High

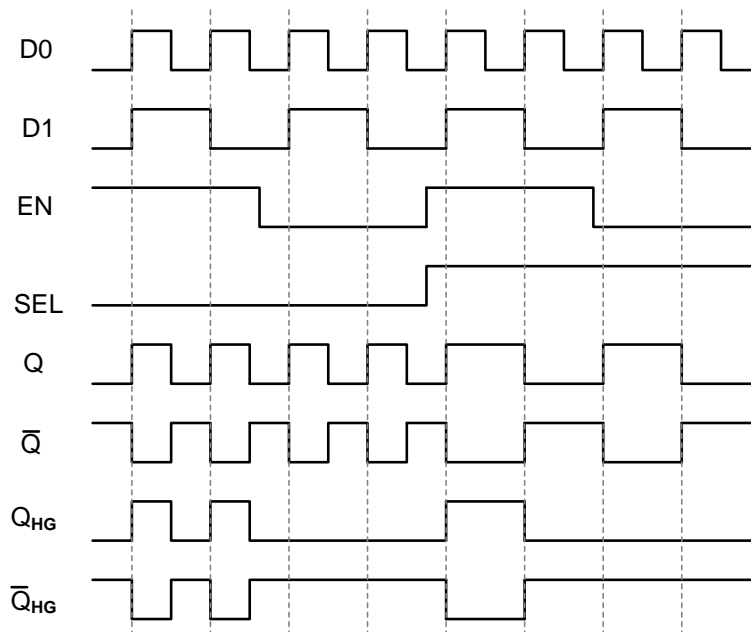


Figure 2 - Timing Diagram

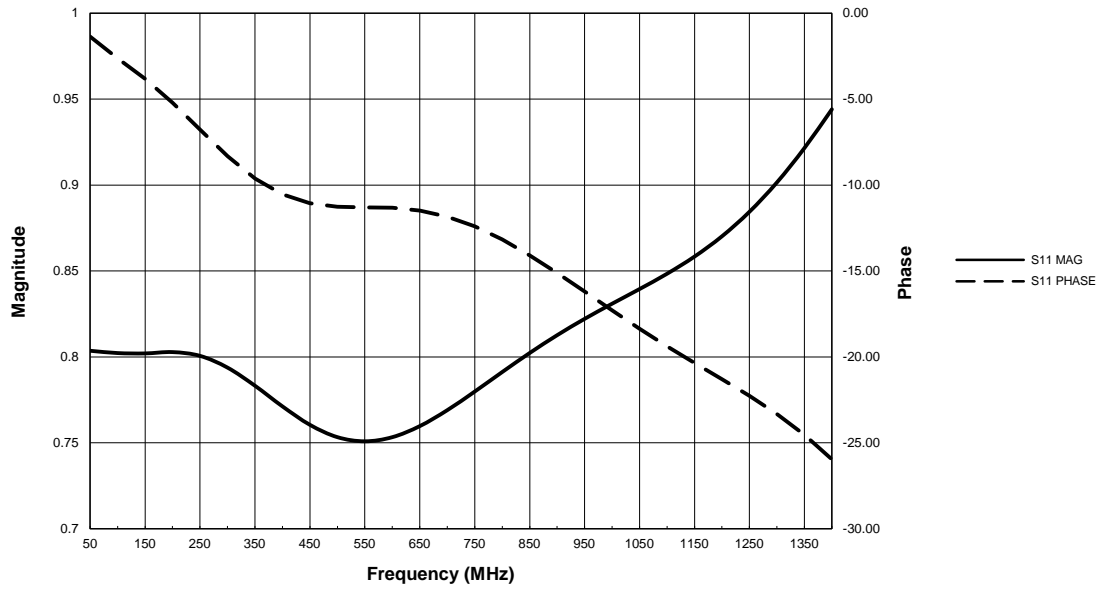


Figure 3 - S11

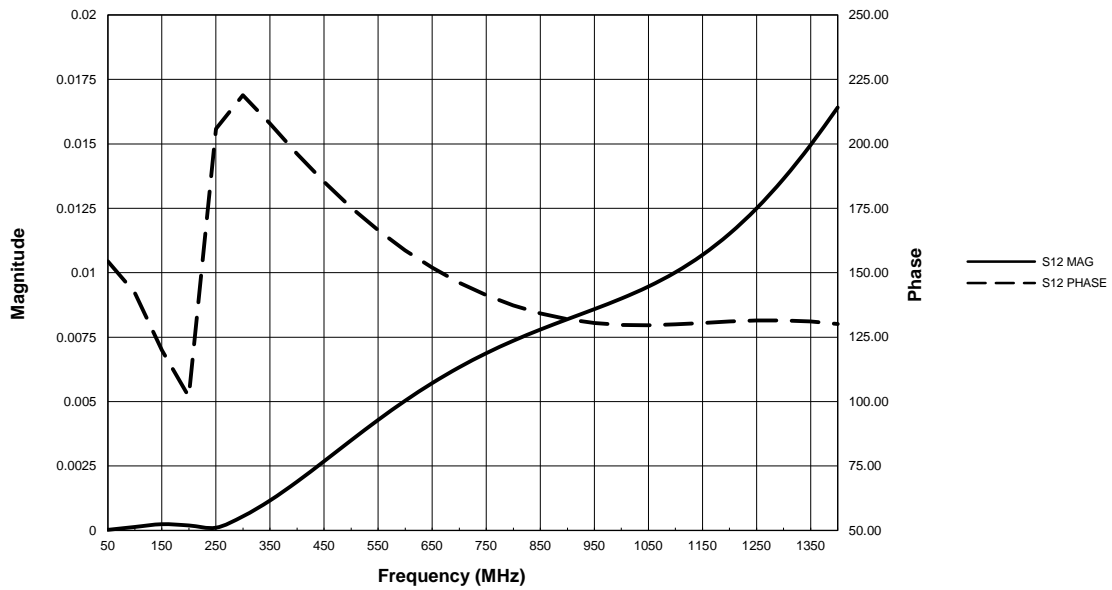


Figure 4 - S12

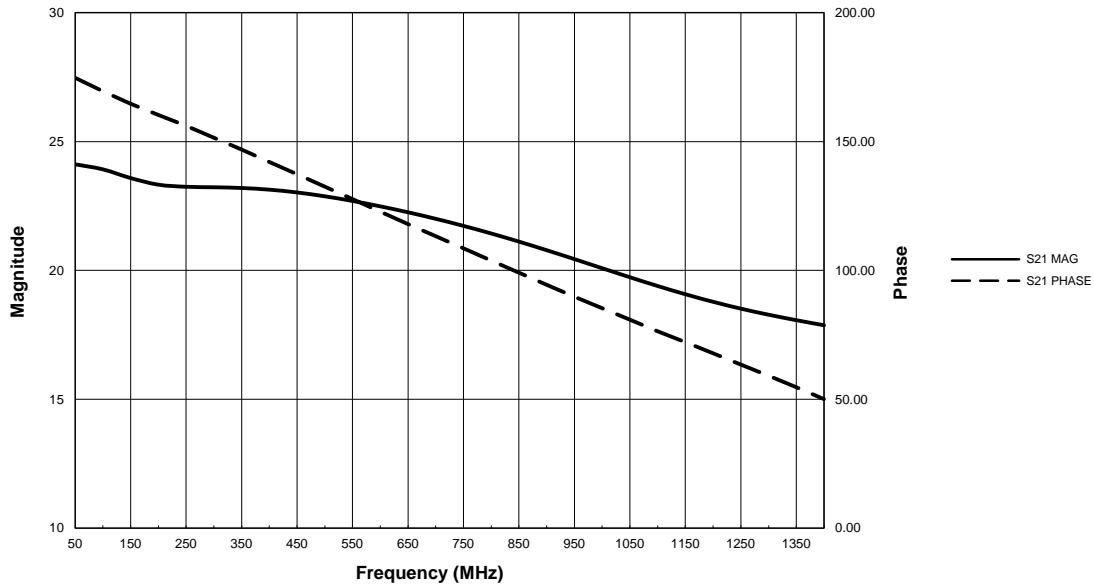


Figure 5 – S21

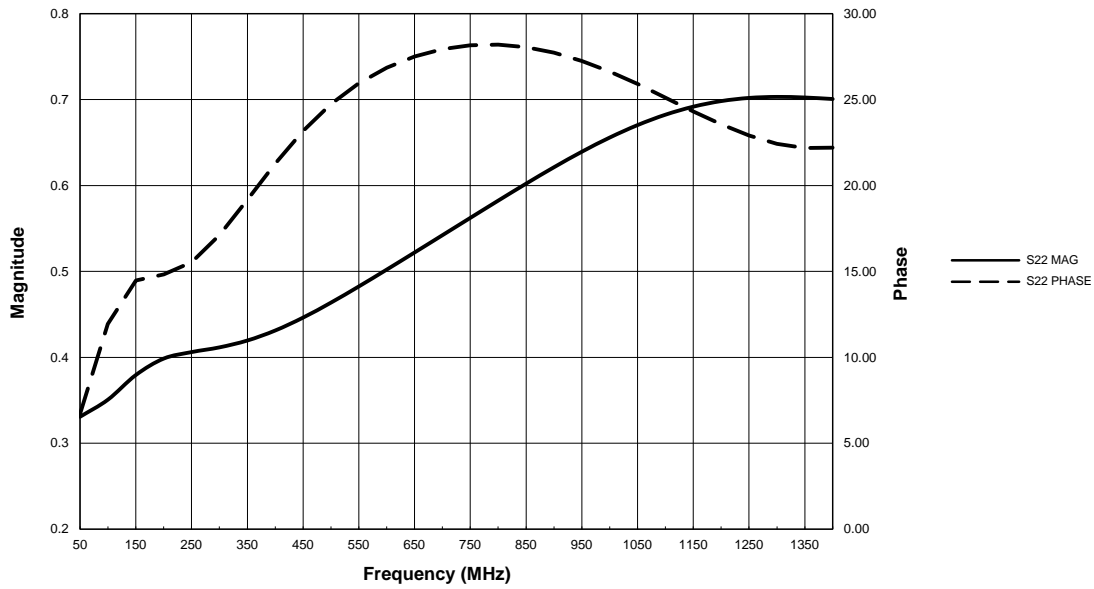


Figure 6 – S22

PERFORMANCE DATA

Table 3 – Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Condition	Rating	Unit
V _{CC}	PECL Power Supply	V _{EE} = 0V	0 to + 6.0	V
V _I	PECL Input Voltage	V _{EE} = 0V	0 to + 6.0	V
V _{D/D}	D/D Input Voltage	Referenced to V _{BB}	±0.75	V
I _{OUT}	Output Current	Continuous Q/Q	25	mA
		Surge Q/Q	50	
		Continuous Q _{HG} /Q _{HG}	50	
		Surge Q _{HG} /Q _{HG}	100	
T _A	Operating Temperature Range	-	-40 to +85	°C
T _{STG}	Storage Temperature Range	-	-65 to +150	°C
ESD _{HBM}	Human Body Model Electro Static Discharge	-	2500	V
ESD _{MM}	Machine Model Electro Static Discharge	-	200	V
ESD _{CDM}	Charged Device Model Electro Static Discharge	-	2000	V

Table 4 - 100K ECL DC Characteristics

100K ECL DC Characteristics (V_{EE} = -3.0V to -5.5V, V_{CC} = GND)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V _{OH}	Output HIGH Voltage ¹	-1045	-835	-1025	-835	-1025	-835	-1025	-835	mV
V _{OL}	Output LOW Voltage ¹	-1925	-1555	-1900	-1620	-1900	-1620	-1900	-1620	mV
V _{BB}	Reference Voltage	-1390	-1250	-1390	-1250	-1390	-1250	-1390	-1250	mV
V _{IH}	Input HIGH Voltage D/D	-1165	-740	-1165	-740	-1165	-740	-1165	-740	mV
	Input HIGH Voltage EN, SEL	-1165	V _{CC}	-1165	V _{CC}	-1165	V _{CC}	-1165	V _{CC}	mV
V _{IL}	Input LOW Voltage D/D	-1900	-1475	-1900	-1475	-1900	-1475	-1900	-1475	mV
	Input LOW Voltage EN, SEL	V _{EE}	-1475	V _{EE}	-1475	V _{EE}	-1475	V _{EE}	-1475	mV
I _{IH}	Input HIGH Current EN		150		150		150		150	μA
I _{IL}	Input LOW Current EN	-100		-100		-100		-100		μA
I _{EE}	Power Supply Current ¹		47		47		47		51	mA

1. Specified with Q/Q open and each Q_{HG}/Q_{HG} output terminated through a 50Ω resistor to V_{CC}-2V.

Table 5 - 100K LVPECL DC Characteristics

100K LVPECL DC Characteristics ($V_{EE} = \text{GND}$, $V_{CC} = +3.3\text{V}$)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage ^{1,2}	2255	2465	2275	2465	2275	2465	2275	2465	mV
V_{OL}	Output LOW Voltage ^{1,2}	1375	1745	1400	1680	1400	1680	1400	1680	mV
V_{BB}	Reference Voltage ¹	1910	2050	1910	2050	1910	2050	1910	2050	mV
V_{IH}	Input HIGH Voltage D/D ¹	2135	2560	2135	2560	2135	2560	2135	2560	mV
	Input HIGH Voltage EN, SEL ¹	2000	V_{CC}	2000	V_{CC}	2000	V_{CC}	2000	V_{CC}	mV
V_{IL}	Input LOW Voltage D/D ¹	1400	1825	1400	1825	1400	1825	1400	1825	mV
	Input LOW Voltage EN, SEL	V_{EE}	1825 ¹	V_{EE}	1825 ¹	V_{EE}	1825 ¹	V_{EE}	1825 ¹	mV
I_{IH}	Input HIGH Current EN		150		150		150		150	μA
I_{IL}	Input LOW Current EN ³	-400		-400		-400		-400		μA
I_{EE}	Power Supply Current		47		47		47		51	mA

1. For supply voltages other than 5.0V, use the ECL table values and ADD supply voltage value.
2. Specified with Q/Q open and each Q_{HG}/Q_{HG} output terminated through a 50Ω resistor to $V_{CC}-2\text{V}$.
3. Specified with EN and SEL forced to V_{EE} .

Table 6 - 100K PECL DC Characteristics

100K PECL DC Characteristics ($V_{EE} = \text{GND}$, $V_{CC} = +5.0\text{V}$)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage ^{1,2}	3955	4165	3975	4165	3975	4165	3975	4165	mV
V_{OL}	Output LOW Voltage ^{1,2}	3075	3445	3100	3380	3100	3380	3100	3380	mV
V_{BB}	Reference Voltage ¹	3610	3750	3610	3750	3610	3750	3610	3750	mV
V_{IH}	Input HIGH Voltage D/D ¹	3835	4260	3835	4260	3835	4260	3835	4260	mV
	Input HIGH Voltage EN, SEL ¹	2000	V_{CC}	2000	V_{CC}	2000	V_{CC}	2000	V_{CC}	mV
V_{IL}	Input LOW Voltage D/D ¹	3100	3525	3100	3525	3100	3525	3100	3525	mV
	Input LOW Voltage EN, SEL	V_{EE}	3525 ¹	V_{EE}	3525 ¹	V_{EE}	3525 ¹	V_{EE}	3525 ¹	mV
I_{IH}	Input HIGH Current EN		150		150		150		150	μA
I_{IL}	Input LOW Current EN ³	-1000		-1000		-1000		-1000		μA
I_{EE}	Power Supply Current		47		47		47		51	mA

1. For supply voltages other than 5.0V, use the ECL table values and ADD supply voltage value.
2. Specified with Q/Q open and each Q_{HG}/Q_{HG} output terminated through a 50Ω resistor to $V_{CC}-2\text{V}$.
3. Specified with EN and SEL forced to V_{EE} .

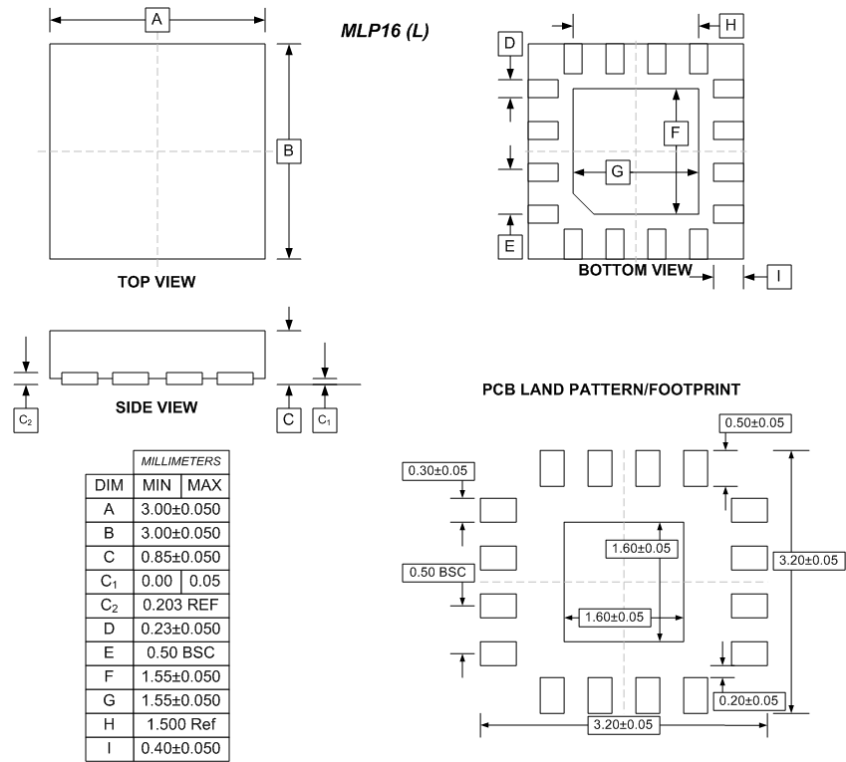
Table 7 - AC Characteristics

AC Characteristics ($V_{EE} = -3.0V$ to $-5.5V$; $V_{CC}=GND$ or $V_{EE}=GND$; $V_{CC} = +3.0V$ to $+5.5V$)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH}/t_{PHL}	Propagation Delay													
	D to Q/Q ¹			400			400			400			430	ps
	D to Q _{HG} /Q _{HG} ²			550			550			550			630	ps
t_{SKEW}	Duty Cycle Skew ³		5	20		5	20		5	20		5	20	ps
V_{PP} (AC)	Input Swing ⁴													
	Differential	80		1000	80		1000	80		1000	80		1000	mV
	Single Ended	150		2000	150		2000	150		2000	150		2000	mV
t_r/t_f	Output Rise/Fall ^{1,2} (20%-80%)	100		260	100		260	100		260	100		260	ps

1. Specified with each output terminated through a 50Ω resistor to $V_{CC}-2V$.
2. Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.
3. V_{PP} is the minimum peak-to-peak input swing for which AC parameters guaranteed. The device has a voltage gain of ≈ 20 to Q/Q outputs and a voltage gain of ≈ 100 to Q_{HG}/Q_{HG} outputs.

PACKAGE DIAGRAM
MLP16
Green/RoHS compliant/Pb-Free
MSL=1



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