AZ100LVEL16VR

PECL/ECL Oscillator Gain Stage & Buffer with Selectable Enable

www.azmicrotek.com

DESCRIPTION

The AZ100LVEL16VR is a specialized oscillator gain stage with a high gain output buffer including an enable function. The $Q_{HG}/\overline{Q}_{HG}$ outputs have voltage gain several times greater than the $Q/\overline{Q}$ outputs. It provides a selectable $Q_{HG}/\overline{Q}_{HG}$ enable that allows continuous oscillator operation via the $Q/\overline{Q}$ outputs.

The AZ100LVEL16VR provides adjustable internal pull-down current sources for the $Q/\overline{Q}$ outputs and optional 10mA current sources for the $Q_{HG}/\overline{Q}_{HG}$ outputs. Internal input biasing further reduces the number of needed external components

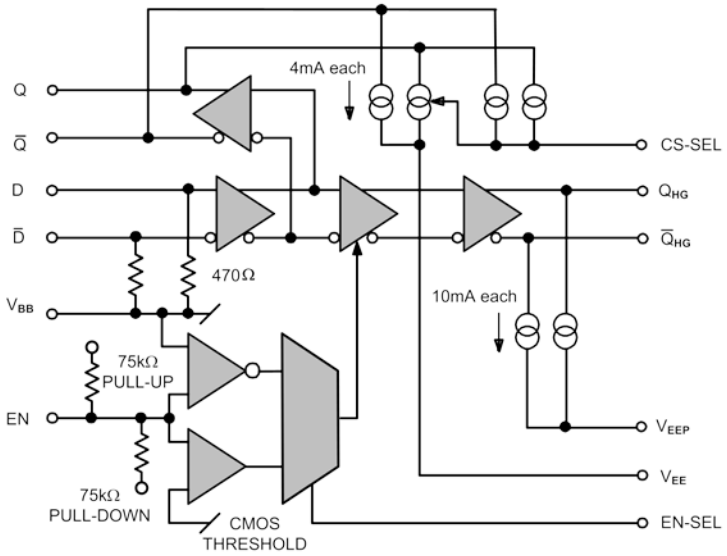
FEATURES

- Minimizes External Components
- Selectable Enable Polarity and Threshold (CMOS or PECL)
- High Bandwidth for ≥1GHz
- Similar Operation as AZ100EL16VO
- -147 dBc/Hz Typical Noise Floor

APPLICATIONS

- Crystal or saw oscillators that require minimal external components.

BLOCK DIAGRAM



PACKAGE AVAILABILITY

- MLP8
  - Green/RoHS Compliant/Pb-Free
- MLP16
  - Green/RoHS Compliant/Pb-Free

Order Number	Package	Marking
AZ100LVEL16VRL[1]	MLP16	AZM+16R <Date Code>[2]
AZ100LVEL16VRNEG[1]	MLP8	R5G <Date Code>[2]

[1] Tape & Reel - Add 'R1' at end of PN for 7in (1k parts), 'R2' (2.5k) for 13in

[2] See www.azmicrotek.com for date code format

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Mesa, AZ 85204 USA

May 2012, Rev 2.0

PIN DESCRIPTION AND CONFIGURATION

Table 1 - Pin Description AZ100LVEL16VRL

Pin	Name	Type	Function
1	NC	-	N/A
2	D	Input	Data Input
3	$\overline{D}$	Input	Inverting Data Input
4	V_{BB}	Output	Reference Voltage
5	EN	Input	Output Enable
6	NC	-	N/A
7	V_{EE}	Power	Negative Supply
8	V_{EEP}	Input	High Gain Current Source Enable
9	EN-SEL	Input	Enable Polarity Select
10	$\overline{Q}_{HG}$	Output	High Gain Inverting PECL Output
11	Q_{HG}	Output	High Gain PECL Output
12	CS-SEL	Input	Current Source Select
13	V_{CC}	Power	Positive Supply
14	NC	-	N/A
15	Q	Output	PECL Output
16	$\overline{Q}$	Output	Inverting PECL Output

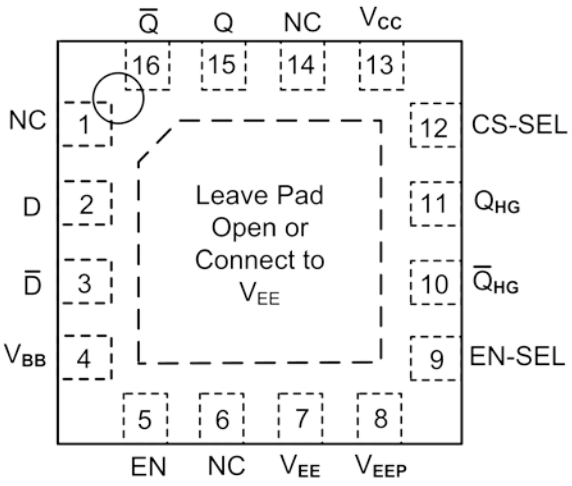


Figure 1 - Pin Configuration for AZ100LVEL16VRL

Table 2 - Pin Description AZ100LVEL16VRNEG

Pin	Name	Type	Function
1	D	Input	Data Input
2	V_{BB}	Output	Reference Voltage
3	EN	Input	Output Enable
4	V_{EE}	Power	Negative Supply
5	$\overline{Q}_{HG}$	Output	High Gain Inverting PECL Output
6	Q_{HG}	Output	High Gain PECL Output
7	V_{CC}	Power	Positive Supply
8	$\overline{Q}$	Output	Inverting PECL Output

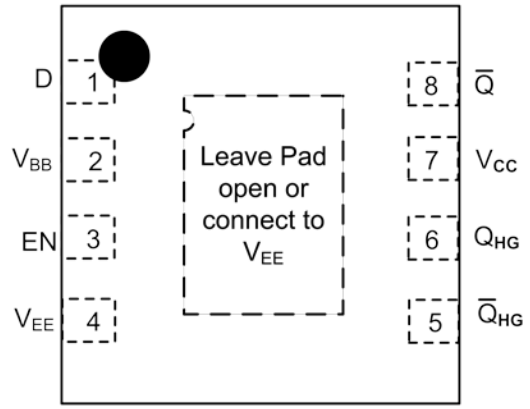


Figure 2 - Pin Configuration for AZ100LVEL16VRNEG

ENGINEERING NOTES

FUNCTIONALITY MLP 16 PACKAGE (AZ100LVEL16VRL)

The AZ100LVEL16VR provides a selectable $Q_{HG}/\overline{Q}_{HG}$ enable that allows continuous oscillator operation via the $Q/\overline{Q}$ outputs. Table 3 shows the operating modes. Leaving EN-SEL open (NC) selects PECL/ECL operation for the EN pad/pin. In this mode the $Q_{HG}/\overline{Q}_{HG}$ outputs are enabled when EN is left open (NC) or set to a PECL/ECL low.

Connecting EN-SEL to V_{CC}, V_{EE} or V_{BB} selects CMOS operation for the EN pad/pin. When EN-SEL is tied to V_{EE}, the $Q_{HG}/\overline{Q}_{HG}$ outputs are disabled when EN is left open (NC). When EN-SEL is tied to V_{CC} or V_{BB}, the $Q_{HG}/\overline{Q}_{HG}$ outputs are enabled when EN is left open. This default logic condition can be overridden by a ≤ 20kΩ resistor connected to the opposite supply.

The AZ100LVEL16VR also provides a V_{BB} and 470Ω internal bias resistors from D to V_{BB} and $\overline{D}$ to V_{BB}. The V_{BB} pin supports 1.5mA sink/source current. V_{BB} should be bypassed to ground or V_{CC} with a 0.01 µF capacitor.

Outputs $Q/\overline{Q}$ each have a selectable on-chip pull-down current source. See Table 4 for the supported values. External resistors may also be used to increase pull-down current to a maximum total of 25mA for the $Q/\overline{Q}$ outputs.

Each of the $Q_{HG}/\overline{Q}_{HG}$ outputs has an optional on-chip pull-down current source of 10mA. When pad/pin V_{EEP} is left open (NC), the output current sources are disabled and the $Q_{HG}/\overline{Q}_{HG}$ operate as standard PECL/ECL. When V_{EEP} is connected to V_{EE}, the current sources are activated. The $Q_{HG}/\overline{Q}_{HG}$ pull-down current can be decreased by using a resistor between V_{EEP} and V_{EE}.

Table 3 – Enable Truth Table

EN-SEL	EN	$Q/\overline{Q}$	Q_{HG}	$\overline{Q}_{HG}$
NC	PECL Low, V_{EE} or NC	Data	Data	Data
	PECL High or V_{CC}	Data	Low	High
V_{EE}[1]	CMOS Low, V_{EE} or NC	Data	Low	High
	CMOS High or V_{CC}	Data	Data	Data
V_{CC} or V_{BB}[1,2]	CMOS Low or V_{EE}	Data	Low	High
	CMOS High, V_{CC} or NC	Data	Data	Data

[1] EN-SEL connections must be ≤1Ω.

[2] Date codes prior to 0428 do not support this operating mode.

Table 4 - Current Source Truth Table

CS-SEL	Q	$\overline{Q}$
NC	4mA typ	4mA typ
V_{EE}[1]	8mA typ	8mA typ
V_{CC}[1]	0	4mA typ

1. Connection must be less than 1Ω

Figure 3 illustrates the timing sequences for the AZ100LVEL16VR in the MLP 16 package or as die. It is shown here with the enable operating in active Low mode with a PECL threshold. This mode is determined by leaving the EN-SEL open (NC). An active High enable with a CMOS/TTL threshold is also an option.

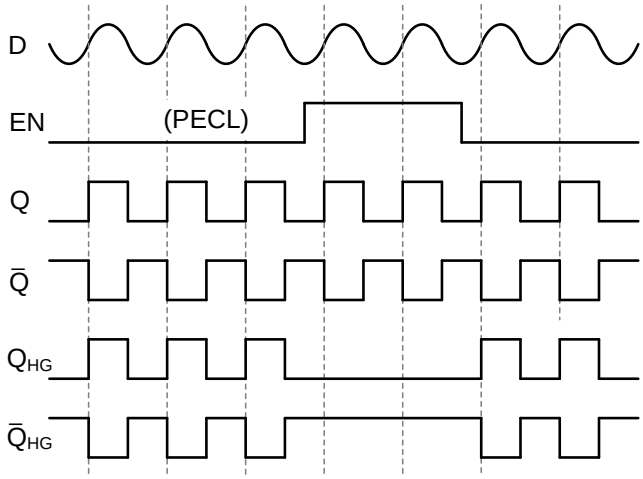


Figure 3 - AZ100LVEL16VRL Timing Diagram

FUNCTIONALITY MLP 8 PACKAGE (AZ100LVEL16VRNEG)

A CMOS enable input (EN) allows continuous oscillator operation. When the EN input is HIGH or left open (NC), the $\overline{Q}$ and $Q_{HG}/\overline{Q}_{HG}$ outputs follow the data input. When EN is LOW, the Q_{HG} output is forced high and the $\overline{Q}_{HG}$ output is forced low while $\overline{Q}$ continues to follow the data input. The $\overline{Q}$ output has an internal 4 mA current source to V_{EE}, in most cases eliminating the need for an external pull-down resistor.

The AZ100LVEL16VRNEG also provides biasing. Data input D is tied to the VBB pin through a 470Ω internal bias resistor while the inverting input $\overline{D}$ is connected directly to V_{BB}. The V_{BB} pin supports 1.5mA sink/source current. V_{BB} should be bypassed to ground with a 0.01 µF capacitor.

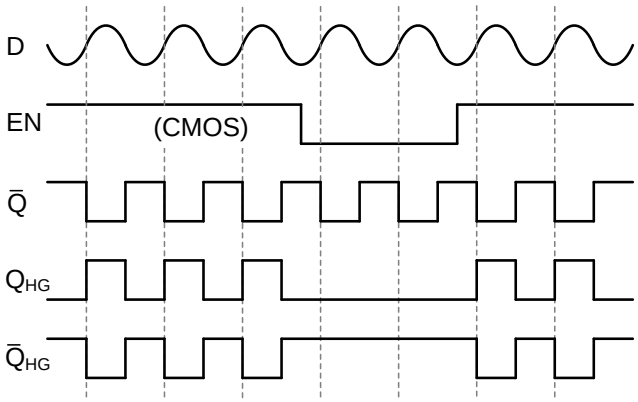
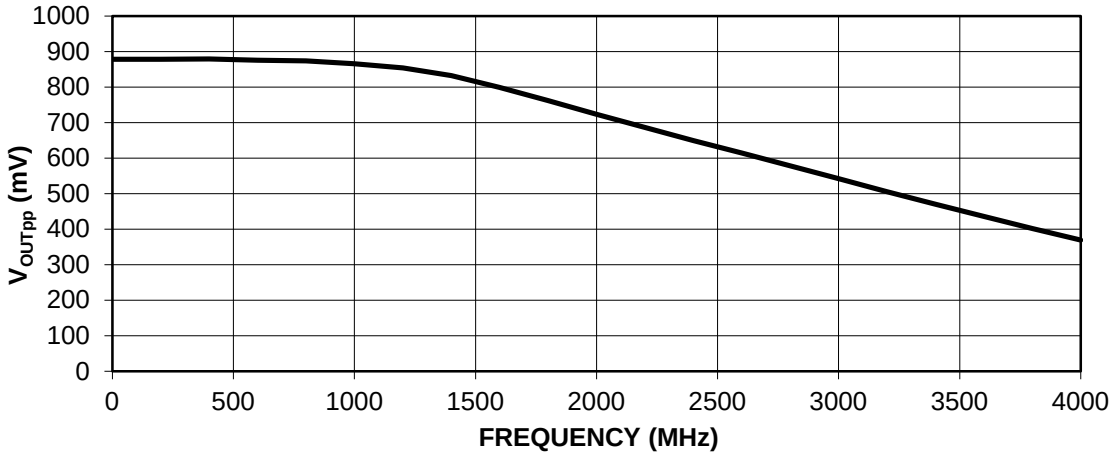


Figure 4 - AZ100LVEL16VRNEG Timing Diagram



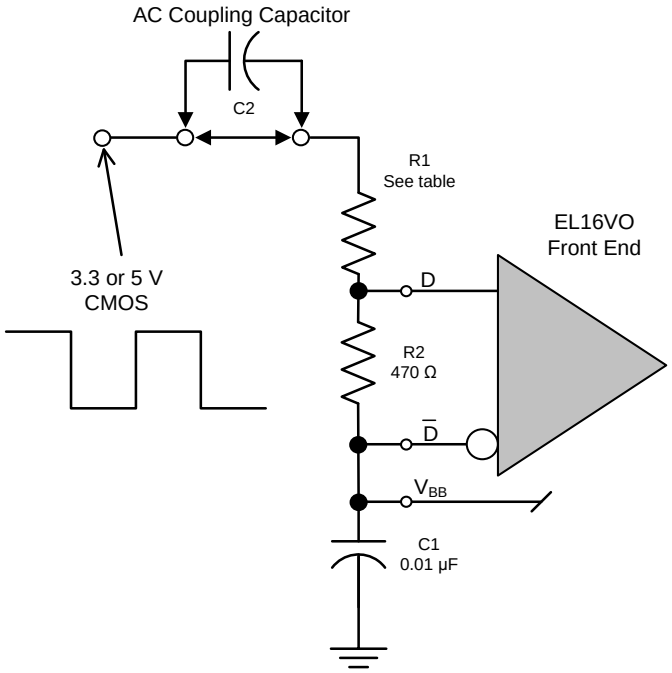


Figure 5 - Application Circuit for CMOS Inputs

Recommended Component Values for CMOS Single Ended Inputs

Input Type	R1[1] Value	
	AC Coupled (C2 in circuit)	DC Coupled (C2 shorted)
3.3 V CMOS	1.1 kΩ	2.0 kΩ
5 V CMOS	1.6 kΩ	3.3 kΩ

1. R1 should be chosen so that the input swing on the D input with respect to $\overline{D}$ is in the range of ±80 to ±1000 mV, per the AC Characteristics table and the D input is < ±750 mV with respect to V_{BB}.

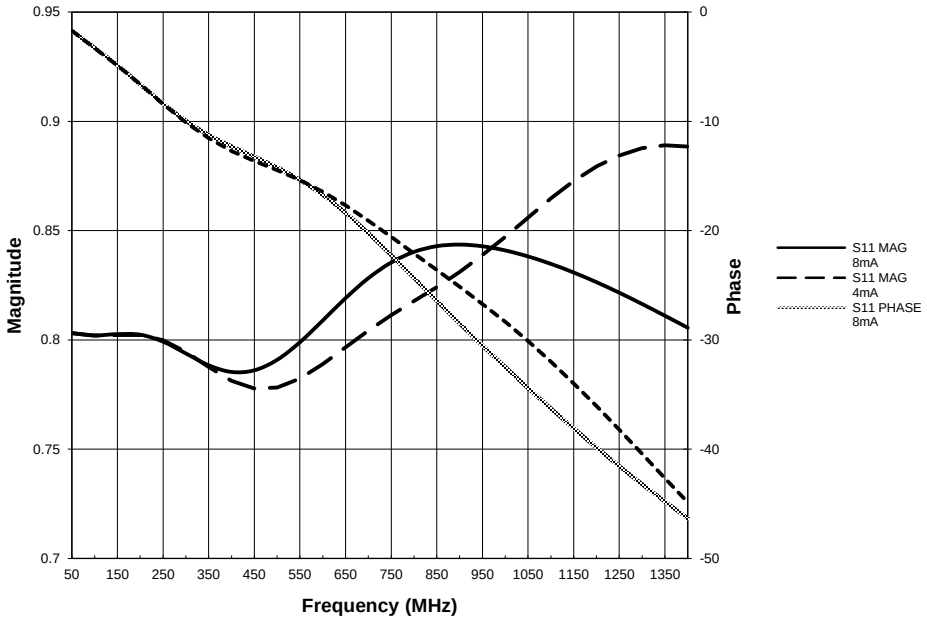


Figure 6 - S11 50Ω external AC, 4 & 8mA internal DC load

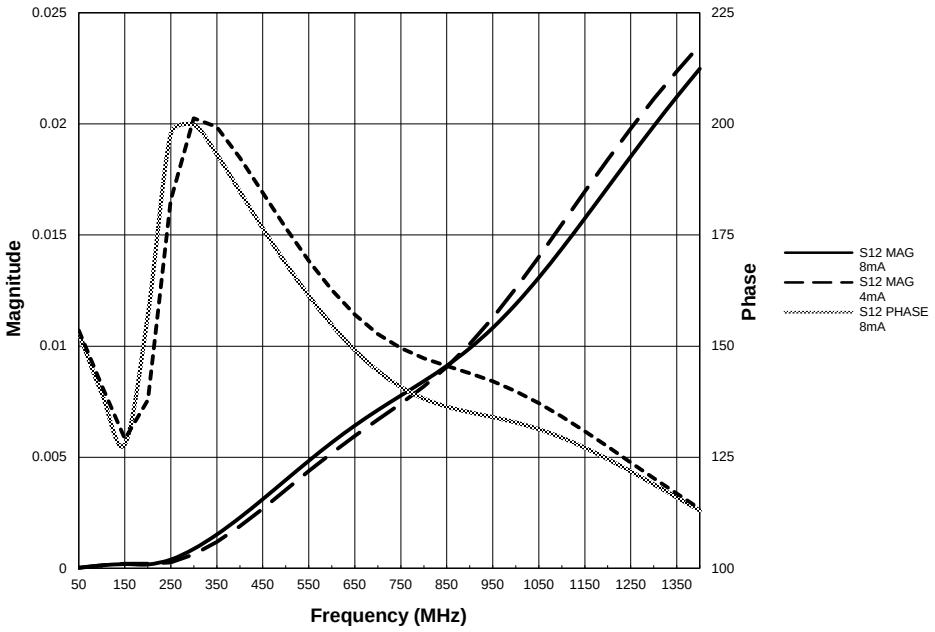


Figure 7 - S12 50Ω external AC, 4 & 8mA internal DC load

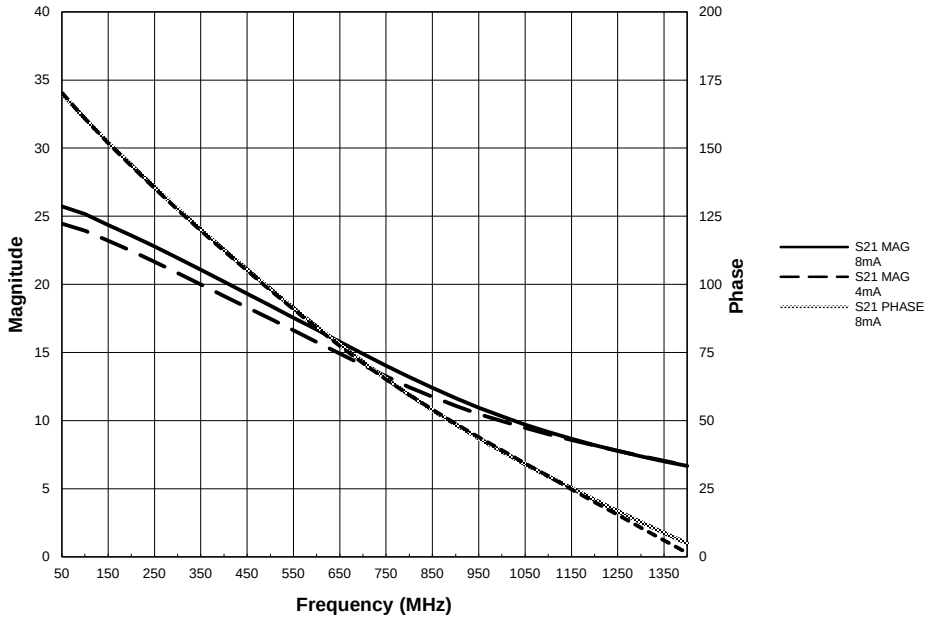


Figure 8 – S21 50Ω external AC, 4 & 8mA internal DC load

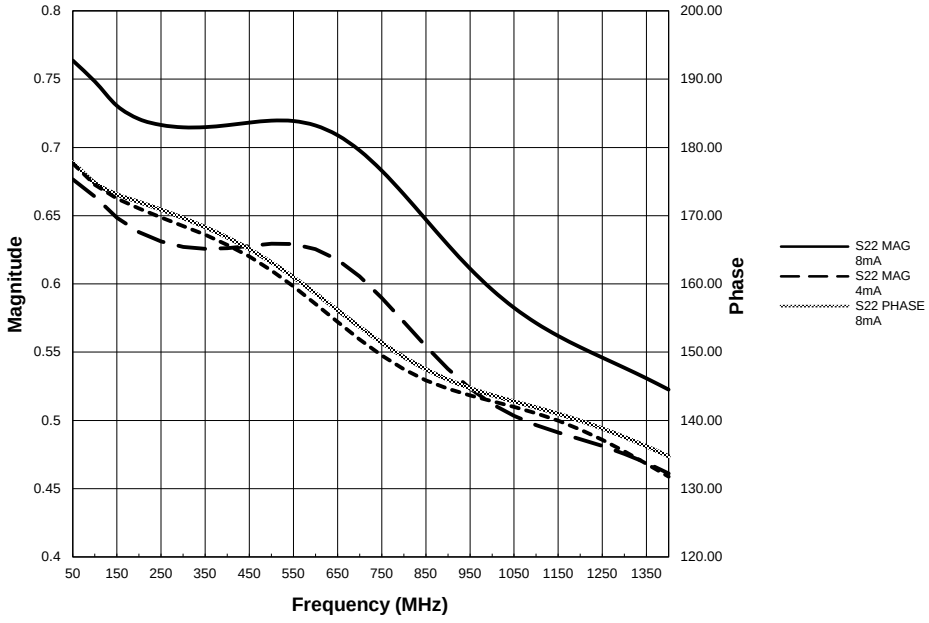


Figure 9 – S22 50Ω external AC, 4 & 8mA internal DC load

PERFORMANCE DATA

Table 5 – Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Condition	Rating	Unit
V_{CC}	PECL Power Supply	V_{EE} = 0V	0 to + 6.0	V
V_I	PECL Input Voltage	V_{EE} = 0V	0 to + 6.0	V
$V_{D/\overline{D}}$	D/$\overline{D}$ Input Voltage	Referenced to V_{BB}	±0.75	V
I_{OUT}	Output Current	Continuous Q/$\overline{Q}$	25	mA
		Surge Q/$\overline{Q}$	50	
		Continuous Q_{HG}/$\overline{Q}_{HG}$	50	
		Surge Q_{HG}/$\overline{Q}_{HG}$	100	
T_A	Operating Temperature Range	-	-40 to +85	°C
T_{STG}	Storage Temperature Range	-	-65 to +150	°C
ESD_{HBM}	Human Body Model Electro Static Discharge	-	2500	V
ESD_{MM}	Machine Model Electro Static Discharge	-	200	V
ESD_{CDM}	Charged Device Model Electro Static Discharge	-	2000	V

Table 6 - 100K ECL DC Characteristics

100K ECL DC Characteristics (V_{EE} = -3.0V to -5.5V, V_{CC} = GND)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1]	-1045	-835	-1025	-835	-1025	-835	-1025	-835	mV
V_{OL}	Output LOW Voltage[1]	-1925	-1555	-1900	-1620	-1900	-1620	-1900	-1620	mV
V_{BB}	Reference Voltage	-1390	-1250	-1390	-1250	-1390	-1250	-1390	-1250	mV
V_{IH}	Input HIGH Voltage D/$\overline{D}$, EN (ECL)[2]	-1165	-740	-1165	-740	-1165	-740	-1165	-740	mV
	Input HIGH Voltage EN (CMOS)[2]	-1165	V_{CC}	-1165	V_{CC}	-1165	V_{CC}	-1165	V_{CC}	mV
V_{IL}	Input LOW Voltage D/$\overline{D}$, EN (ECL)[2]	-1900	-1475	-1900	-1475	-1900	-1475	-1900	-1475	mV
	Input LOW Voltage EN (CMOS)[2]	V_{EE}	V_{EE}+800	V_{EE}	V_{EE}+800	V_{EE}	V_{EE}+800	V_{EE}	V_{EE}+800	mV
I_{IH}	Input HIGH Current EN		150		150		150		150	µA
I_{IL}	Input LOW Current EN (ECL)[2]	0.5		0.5		0.5		0.5		µA
	Input LOW Current EN (CMOS)[3]	-150		-150		-150		-150		µA
I_{EE}	Power Supply Current[1]		48		48		48		54	mA

1. Specified with V_{EEP} and CS-SEL NC, Q_{HG}/$\overline{Q}_{HG}$ terminated through 50Ω resistors to V_{CC} - 2V.
2. EN-SEL = NC.
3. EN-SEL = V_{CC} or V_{EE}.

Table 7 - 100K LVPECL DC Characteristics

100K LVPECL DC Characteristics (VEE = GND, VCC = +3.3V)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1,2]	2255	2465	2275	2465	2275	2465	2275	2465	mV
V_{OL}	Output LOW Voltage[1,2]	1375	1745	1400	1680	1400	1680	1400	1680	mV
V_{BB}	Reference Voltage[1]	1910	2050	1910	2050	1910	2050	1910	2050	mV
V_{IH}	Input HIGH Voltage D/$\overline{D}$, EN (ECL)[3]	2135	2560	2135	2560	2135	2560	2135	2560	mV
	Input HIGH Voltage EN (CMOS)[4]	2000	V_{CC}	2000	V_{CC}	2000	V_{CC}	2000	V_{CC}	mV
V_{IL}	Input LOW Voltage D/$\overline{D}$, EN (ECL)[3]	1400	1825	1400	1825	1400	1825	1400	1825	mV
	Input LOW Voltage EN (CMOS)[4]	GND	800	GND	800	GND	800	GND	800	mV
I_{IH}	Input HIGH Current EN		150		150		150		150	µA
I_{IL}	Input LOW Current EN (ECL)	0.5		0.5		0.5		0.5		µA
	Input LOW Current EN (CMOS)	-150		-150		-150		-150		µA
I_{EE}	Power Supply Current[2]		48		48		48		54	mA

1. For supply voltages other that 3.3V, use the ECL table values and ADD supply voltage value.
2. Specified with V_{EEP} and CS-SEL NC, $Q_{HG}/\overline{Q}_{HG}$ terminated through 50Ω resistors to V_{CC} - 2V.
3. EN-SEL = NC.
4. EN-SEL = V_{CC} or V_{EE}.

Table 8 - 100K PECL DC Characteristics

100K PECL DC Characteristics (VEE = GND, VCC = +5.0V)

Symbol	Characteristic	-40°C		0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage[1,2]	3955	4165	3975	4165	3975	4165	3975	4165	mV
V_{OL}	Output LOW Voltage[1,2]	3075	3445	3100	3380	3100	3380	3100	3380	mV
V_{BB}	Reference Voltage[1]	3610	3750	3610	3750	3610	3750	3610	3750	mV
V_{IH}	Input HIGH Voltage D/$\overline{D}$, EN (ECL)[3]	3835	4260	3835	4260	3835	4260	3835	4260	mV
	Input HIGH Voltage EN (CMOS)[4]	2000	V_{CC}	2000	V_{CC}	2000	V_{CC}	2000	V_{CC}	mV
V_{IL}	Input LOW Voltage D/$\overline{D}$, EN (ECL)[3]	3100	3525	3100	3525	3100	3525	3100	3525	mV
	Input LOW Voltage EN (CMOS)[4]	GND	800	GND	800	GND	800	GND	800	mV
I_{IH}	Input HIGH Current EN		150		150		150		150	µA
I_{IL}	Input LOW Current EN (ECL)	0.5		0.5		0.5		0.5		µA
	Input LOW Current EN (CMOS)	-150		-150		-150		-150		µA
I_{EE}	Power Supply Current[2]		48		48		48		54	mA

1. For supply voltages other that 5.0V, use the ECL table values and ADD supply voltage value.
2. Specified with V_{EEP} and CS-SEL NC, $Q_{HG}/\overline{Q}_{HG}$ terminated through 50Ω resistors to V_{CC} - 2V.
3. EN-SEL = NC.
4. EN-SEL = V_{CC} or V_{EE}.

Table 9 - AC Characteristics

AC Characteristics (V_{EE} = -3.0V to -5.5V; V_{CC}=GND or V_{EE}=GND; V_{CC} = +3.0V to +5.5V)

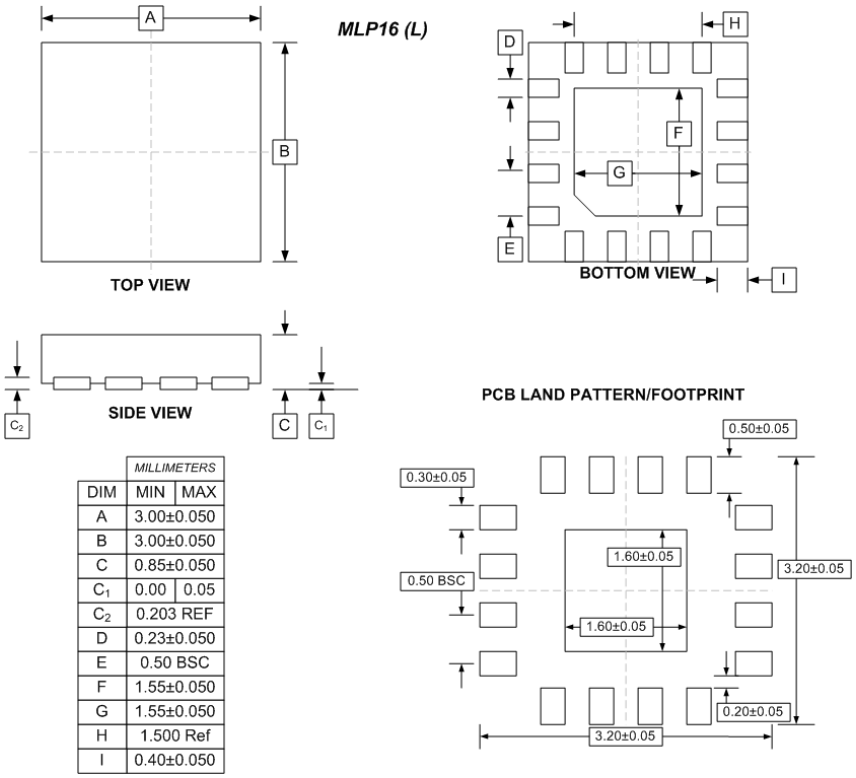
Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH}/t_{PHL}	Propagation Delay													
	D to $Q/\overline{Q}$[1]			400			400			400			400	ps
	D to $Q_{HG}/\overline{Q}_{HG}$[2]			450			450			450			450	ps
t_{SKEW}	Duty Cycle Skew[3]		5	20		5	20		5	20		5	20	ps
Vpp (AC)	Input Swing[4]													
	Differential	80		1000	80		1000	80		1000	80		1000	mV
	Single Ended	150		2000	150		2000	150		2000	150		2000	mV
t_r/t_f	Output Rise/Fall[1,2] (20%-80%)	80		200	80		200	80		200	80		200	ps

1. Specified with CS-SEL connected to V_{EE}, $Q/\overline{Q}$ terminated with an AC coupled 50Ω load.
2. Specified with V_{EEP} NC, $Q_{HG}/\overline{Q}_{HG}$ terminated through 50Ω resistors to V_{CC} - 2V.
3. Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.
4. The peak-to-peak differential input swing is the range for which AC parameters are guaranteed. See figure 7 V_D and $V_{\overline{D}}$ must remain within the range of ± 750 mV with respect to V_{BB}. The device has a voltage gain of ≈ 20 to the $Q/\overline{Q}$ outputs and a voltage gain of ≈ 100 to the $Q_{HG}/\overline{Q}_{HG}$ outputs.

PACKAGE DIAGRAM

MLP16

Green/RoHS compliant/Pb-Free
MSL=1

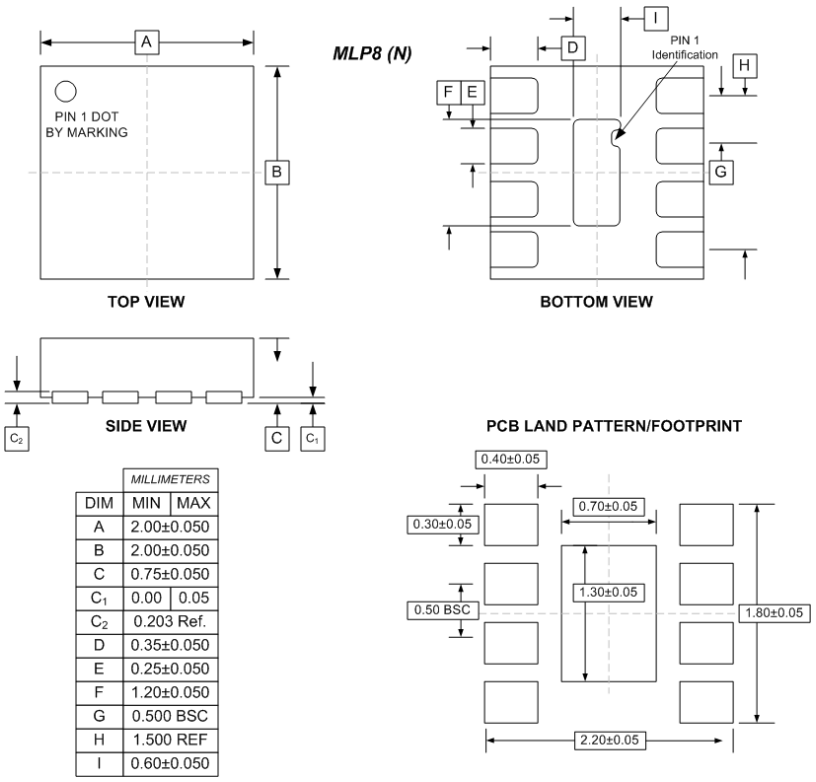


	MILLIMETERS	
DIM	MIN	MAX
A	3.00±0.050	
B	3.00±0.050	
C	0.85±0.050	
C_1	0.00	0.05
C_2	0.203 REF	
D	0.23±0.050	
E	0.50 BSC	
F	1.55±0.050	
G	1.55±0.050	
H	1.500 Ref	
I	0.40±0.050	

PACKAGE DIAGRAM

MLP8

Green/RoHS compliant/Pb-Free
MSL=1



DIM	MILLIMETERS MIN	MAX
A	2.00±0.050	
B	2.00±0.050	
C	0.75±0.050	
C_1	0.00	0.05
C_2	0.203 Ref.	
D	0.35±0.050	
E	0.25±0.050	
F	1.20±0.050	
G	0.500 BSC	
H	1.500 REF	
I	0.60±0.050	