ARIZONA MICROTEK, INC.

AZ10LVEL33
AZ100LVEL33

ECL/PECL ÷4 Divider

FEATURES

- Green / RoHS Compliant / Lead (Pb) Free package available
- Operating Range of 3.0V to 5.5V
- 470ps Propagation Delay
- 4.0GHz Toggle Frequency
- Internal Input Pulldown Resistors
- Direct Replacement for ON Semiconductor MC10EL33, MC100EL33, and MC100LVEL33
- Transistor Count = 91 Devices
- IBIS Model Files Available on Arizona Microtek Web Site

PACKAGE AVAILABILITY

PACKAGE	PART NUMBER	MARKING	NOTES
MLP 8 (2x2) Green / RoHS Compliant / Lead (Pb) Free	AZ100LVEL33NG	C3G <Date Code>	1,2
MLP 16 (3x3)	AZ10/100LVEL33L	AZM L33 <Date Code>	1,2
SOIC 8	AZ10LVEL33D	AZM10 LVEL33	1,2,3
SOIC 8	AZ100LVEL33D	AZM100 LVEL33	1,2,3
TSSOP 8	AZ10LVEL33T	AZT LV33	1,2,3
TSSOP 8	AZ100LVEL33T	AZH LV33	1,2,3

1 Add R1 at end of part number for 7 inch (1K parts), R2 for 13 inch (2.5K parts) Tape & Reel.
2 Date code format: "Y" or "YY" for year followed by "WW" for week.
3 Date code "YWW" or "YYWW" on underside of part.

DESCRIPTION

The AZ10/100LVEL33 is an integrated ÷4 divider. The RESET pin is asynchronous and clears the output (Q Low, $\overline{Q}$ High) on the rising edge. Upon power-up, the internal flip-flop will be in a random logic state. RESET allows for the synchronization of multiple LVEL33's in a system.

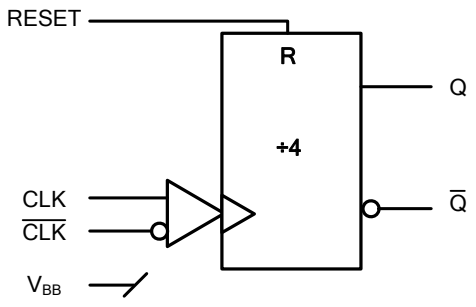
The LVEL33 provides a V_{BB} output for single-end use or a DC bias reference for AC coupling to the device. For single-ended input applications, the V_{BB} reference should be connected to one side of the CLK/$\overline{CLK}$ differential input pair. The input signal is then fed to the other CLK/$\overline{CLK}$ input. The V_{BB} pin can support 1.0mA sink/source current. When used, the V_{BB} pin should be bypassed to ground via a 0.01μF capacitor.

NOTE: Specifications in the ECL/PECL tables are valid when thermal equilibrium is established.

PIN DESCRIPTION

PIN	FUNCTION
CLK, $\overline{CLK}$	Clock Inputs
RESET	Asynchronous Reset
V_{BB}	Reference Voltage Output
Q, $\overline{Q}$	Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

LOGIC DIAGRAM



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Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Rating	Unit
V_{CC}	PECL Power Supply (V_{EE} = 0V)	0 to +8.0	Vdc
V_I	PECL Input Voltage (V_{EE} = 0V)	0 to +6.0	Vdc
V_{EE}	ECL Power Supply (V_{CC} = 0V)	-8.0 to 0	Vdc
V_I	ECL Input Voltage (V_{CC} = 0V)	-6.0 to 0	Vdc
I_{OUT}	Output Current --- Continuous --- Surge	50 100	mA
T_A	Operating Temperature Range	-40 to +85	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C

10K ECL DC Characteristics (V_{EE} = -3.0V to -5.5V, V_{CC} = GND)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage[1]	-1080		-890	-1020		-840	-980		-810	-910		-720	mV
V_{OL}	Output LOW Voltage[1]	-1950		-1650	-1950		-1630	-1950		-1630	-1950		-1595	mV
V_{IH}	Input HIGH Voltage	-1230		-890	-1170		-840	-1130		-810	-1060		-720	mV
V_{IL}	Input LOW Voltage	-1950		-1500	-1950		-1480	-1950		-1480	-1950		-1445	mV
V_{BB}	Reference Voltage	-1430		-1300	-1380		-1270	-1350		-1250	-1310		-1190	mV
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{IL}	Input LOW Current CLK, $\overline{CLK}$ RESET	 -150 0.5			 -150 0.5			 -150 0.5			 -150 0.5			µA
I_{EE}	Power Supply Current		27	33		27	33		27	33		27	33	mA

1. Each output is terminated through a 50Ω resistor to V_{CC} – 2V.

10K LVPECL DC Characteristics (V_{EE} = GND, V_{CC} = +3.3V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage[1,2]	2220		2410	2280		2460	2320		2490	2390		2580	mV
V_{OL}	Output LOW Voltage[1,2]	1350		1650	1350		1670	1350		1670	1350		1705	mV
V_{IH}	Input HIGH Voltage[1]	2070		2410	2130		2460	2170		2490	2240		2580	mV
V_{IL}	Input LOW Voltage[1]	1350		1800	1350		1820	1350		1820	1350		1855	mV
V_{BB}	Reference Voltage[1]	1870		2000	1920		2030	1950		2050	1990		2110	mV
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{IL}	Input LOW Current CLK, $\overline{CLK}$ RESET	 -150 0.5			 -150 0.5			 -150 0.5			 -150 0.5			µA
I_{EE}	Power Supply Current		27	33		27	33		27	33		27	33	mA

1. For supply voltages other that 3.3V, use the ECL table values and ADD supply voltage value.
2. Each output is terminated through a 50Ω resistor to V_{CC} – 2V.

10K PECL DC Characteristics (V_{EE} = GND, V_{CC} = +5.0V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage[1,2]	3920		4110	3980		4160	4020		4190	4090		4280	mV
V_{OL}	Output LOW Voltage[1,2]	3050		3350	3050		3370	3050		3370	3050		3405	mV
V_{IH}	Input HIGH Voltage[1]	3770		4110	3830		4160	3870		4190	3940		4280	mV
V_{IL}	Input LOW Voltage[1]	3050		3500	3050		3520	3050		3520	3050		3555	mV
V_{BB}	Reference Voltage[1]	3570		3700	3620		3730	3650		3750	3690		3810	mV
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{IL}	Input LOW Current CLK, $\overline{CLK}$ RESET	 -150 0.5			 -150 0.5			 -150 0.5			 -150 0.5			µA
I_{EE}	Power Supply Current		27	33		27	33		27	33		27	33	mA

1. For supply voltages other that 5.0V, use the ECL table values and ADD supply voltage value.
2. Each output is terminated through a 50Ω resistor to V_{CC} – 2V.

100K ECL DC Characteristics (V_{EE} = -3.0V to -5.5V, V_{CC} = GND)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage[1]	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	-1025	-955	-880	mV
V_{OL}	Output LOW Voltage[1]	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	-1810	-1705	-1620	mV
V_{IH}	Input HIGH Voltage	-1165		-880	-1165		-880	-1165		-880	-1165		-880	mV
V_{IL}	Input LOW Voltage	-1810		-1475	-1810		-1475	-1810		-1475	-1810		-1475	mV
V_{BB}	Reference Voltage	-1380		-1260	-1380		-1260	-1380		-1260	-1380		-1260	mV
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{IL}	Input LOW Current CLK, $\overline{CLK}$ RESET	-150 0.5			-150 0.5			-150 0.5			-150 0.5			µA
I_{EE}	Power Supply Current		27	33		27	33		27	33		31	37	mA

1. Each output is terminated through a 50Ω resistor to V_{CC} – 2V.

100K LVPECL DC Characteristics (V_{EE} = GND, V_{CC} = +3.3V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage[1,2]	2215	2295	2420	2275	2345	2420	2275	2345	2420	2275	2345	2420	mV
V_{OL}	Output LOW Voltage[1,2]	1470	1605	1745	1490	1595	1680	1490	1595	1680	1490	1595	1680	mV
V_{IH}	Input HIGH Voltage[1]	2135		2420	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage[1]	1490		1825	1490		1825	1490		1825	1490		1825	mV
V_{BB}	Reference Voltage[1]	1920		2040	1920		2040	1920		2040	1920		2040	mV
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{IL}	Input LOW Current CLK, $\overline{CLK}$ RESET	-150 0.5			-150 0.5			-150 0.5			-150 0.5			µA
I_{EE}	Power Supply Current		27	33		27	33		27	33		31	37	mA

1. For supply voltages other that 3.3V, use the ECL table values and ADD supply voltage value.
2. Each output is terminated through a 50Ω resistor to V_{CC} – 2V.

100K PECL DC Characteristics (V_{EE} = GND, V_{CC} = +5.0V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage[1,2]	3915	3995	4120	3975	4045	4120	3975	4045	4120	3975	4045	4120	mV
V_{OL}	Output LOW Voltage[1,2]	3170	3305	3445	3190	3295	3380	3190	3295	3380	3190	3295	3380	mV
V_{IH}	Input HIGH Voltage[1]	3835		4120	3835		4120	3835		4120	3835		4120	mV
V_{IL}	Input LOW Voltage[1]	3190		3525	3190		3525	3190		3525	3190		3525	mV
V_{BB}	Reference Voltage[1]	3620		3740	3620		3740	3620		3740	3620		3740	mV
I_{IH}	Input HIGH Current			150			150			150			150	µA
I_{IL}	Input LOW Current CLK, $\overline{CLK}$ RESET	-150 0.5			-150 0.5			-150 0.5			-150 0.5			µA
I_{EE}	Power Supply Current		27	33		27	33		27	33		31	37	mA

1. For supply voltages other that 5.0V, use the ECL table values and ADD supply voltage value.
2. Each output is terminated through a 50Ω resistor to V_{CC} – 2V.

AC Characteristics (V_{EE} = -3.0V to -5.5V; V_{CC} = GND or V_{EE} = GND; V_{CC} = +3.0V to +5.5V)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency	3.4	4.0		3.8	4.0		3.8	4.0		3.8	4.0		GHz
t_{PLH} / t_{PHL}	Propagation Delay CLK, $\overline{CLK}$ to Q/$\overline{Q}$ RESET to Q/$\overline{Q}$	 360 310	 450 460	 540 610	 320 340	 460 460	 550 580	 380 360	 470 460	 560 560	 400 380	 490 480	 580 580	ps
t_{RR}	Reset Recovery	300			300			300			300			ps
t_{skew}	Within-Device Skew			20			20			20			20	ps
V_{PP} (AC)	Input Swing[1]	150		1000	150		1000	150		1000	150		1000	mV
V_{CMR}	Common Mode Range[2] Vpp < 500mV Vpp ≥ 500mV	V_{EE} + 1.2 1.4		V_{CC} - 0.4 0.4	V_{EE} + 1.1 1.3		V_{CC} - 0.4 0.4	V_{EE} + 1.1 1.3		V_{CC} - 0.4 0.4	V_{EE} + 1.1 1.3		V_{CC} - 0.4 0.4	V
t_r / t_f	Output Rise/Fall Times Q/$\overline{Q}$ (20% - 80%)	100		260	100		260	100		260	100		260	ps

1. V_{PP} is the peak-to-peak differential input swing for which AC parameters are guaranteed.
2. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that V_{PP} is within the differential input swing range specified.

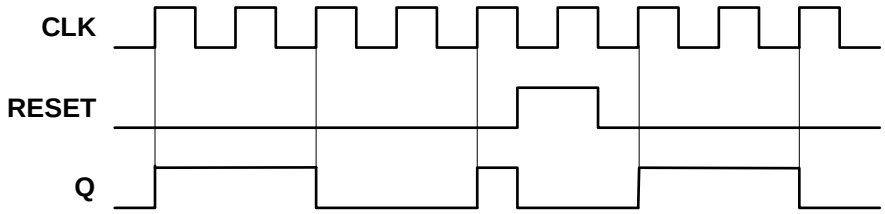
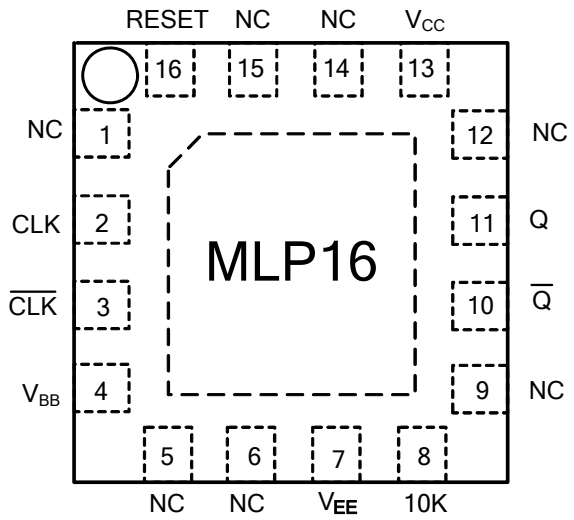


Figure 1. Timing Diagram

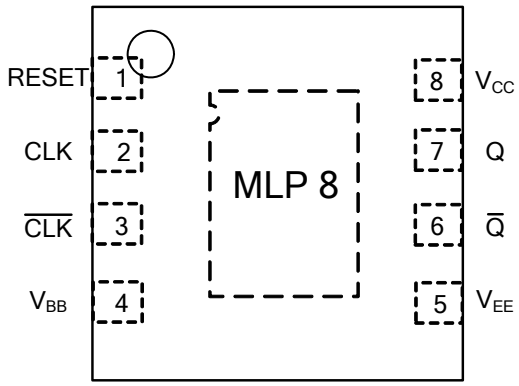
PACKAGE PINOUTS
TOP VIEW

AZ10/100LVEL33L



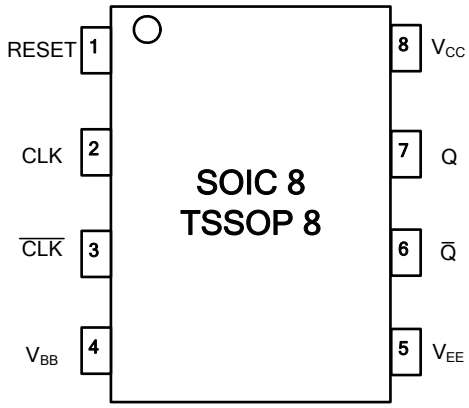
100K Mode: Leave the 10K pin open (NC)
10K Mode: Connect the 10K pin to V_{EE}
Bottom Center Pad may be left open or tied to V_{EE}.

AZ100LVEL33N

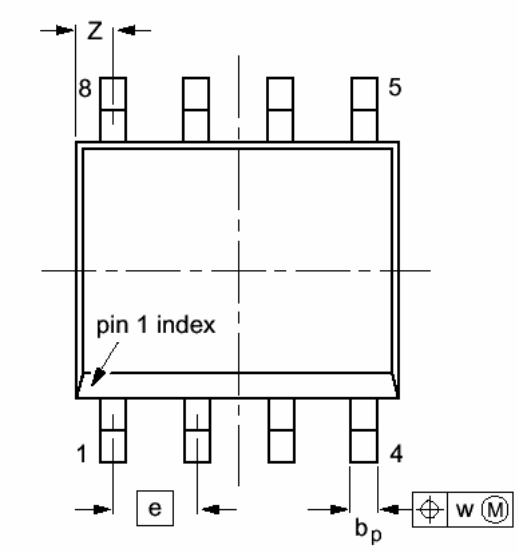


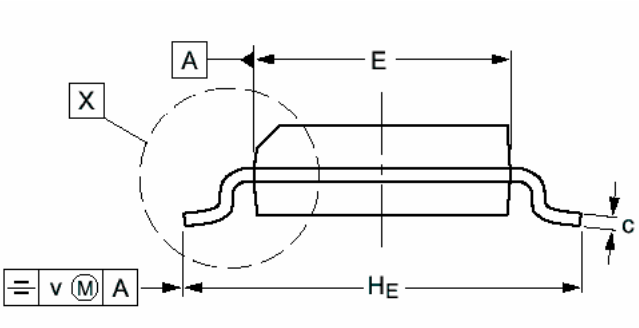
Bottom Center Pad may be left open or tied to V_{EE}.

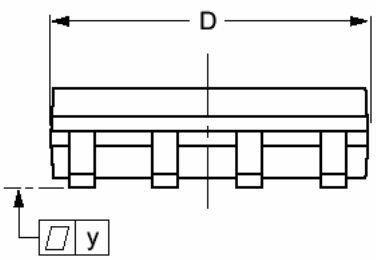
AZ10LVEL33D
AZ100LVEL33D
AZ10LVEL33T
AZ100LVEL33T

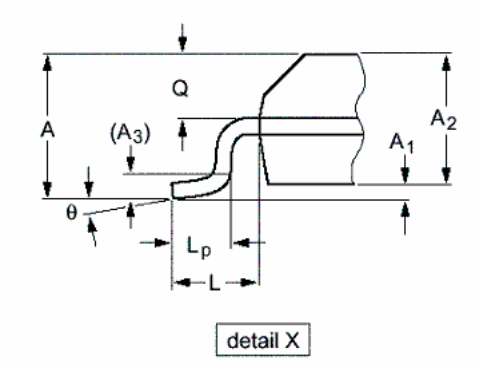


PACKAGE DIAGRAM
SOIC 8





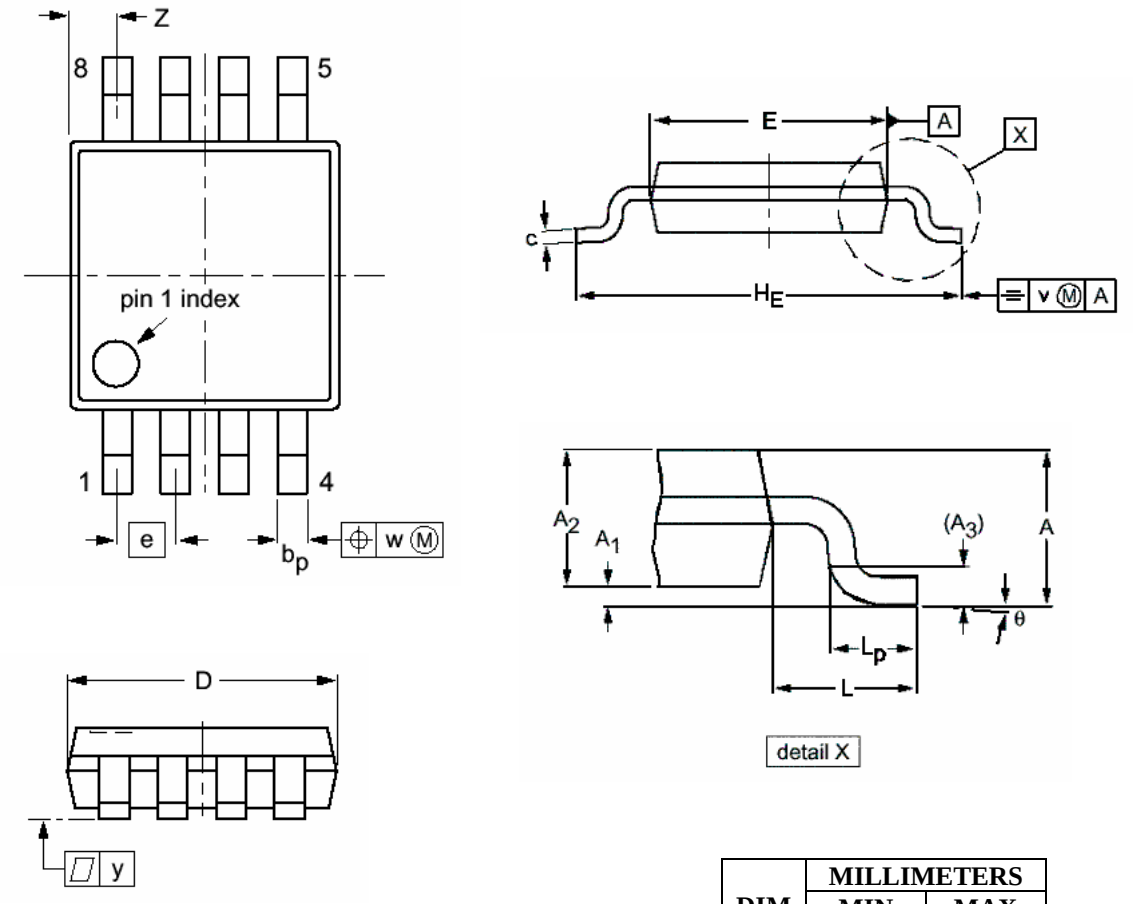




NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
2. MAXIMUM MOLD PROTRUSION FOR D IS 0.15mm.
3. MAXIMUM MOLD PROTRUSION FOR E IS 0.25mm.

	MILLIMETERS		INCHES	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A		1.75		0.069
A_1	0.10	0.25	0.004	0.010
A_2	1.25	1.45	0.049	0.057
A_3	0.25		0.01	
b_p	0.36	0.49	0.014	0.019
c	0.19	0.25	0.0075	0.0100
D	4.8	5.0	0.19	0.20
E	3.8	4.0	0.15	0.16
e	1.27		0.050	
H_E	5.80	6.20	0.228	0.244
L	1.05		0.041	
L_p	0.40	1.00	0.016	0.039
Q	0.60	0.70	0.024	0.028
v	0.25		0.01	
w	0.25		0.01	
y	0.10		0.004	
Z	0.30	0.70	0.012	0.028
θ	0^O	8^O	0^O	8^O

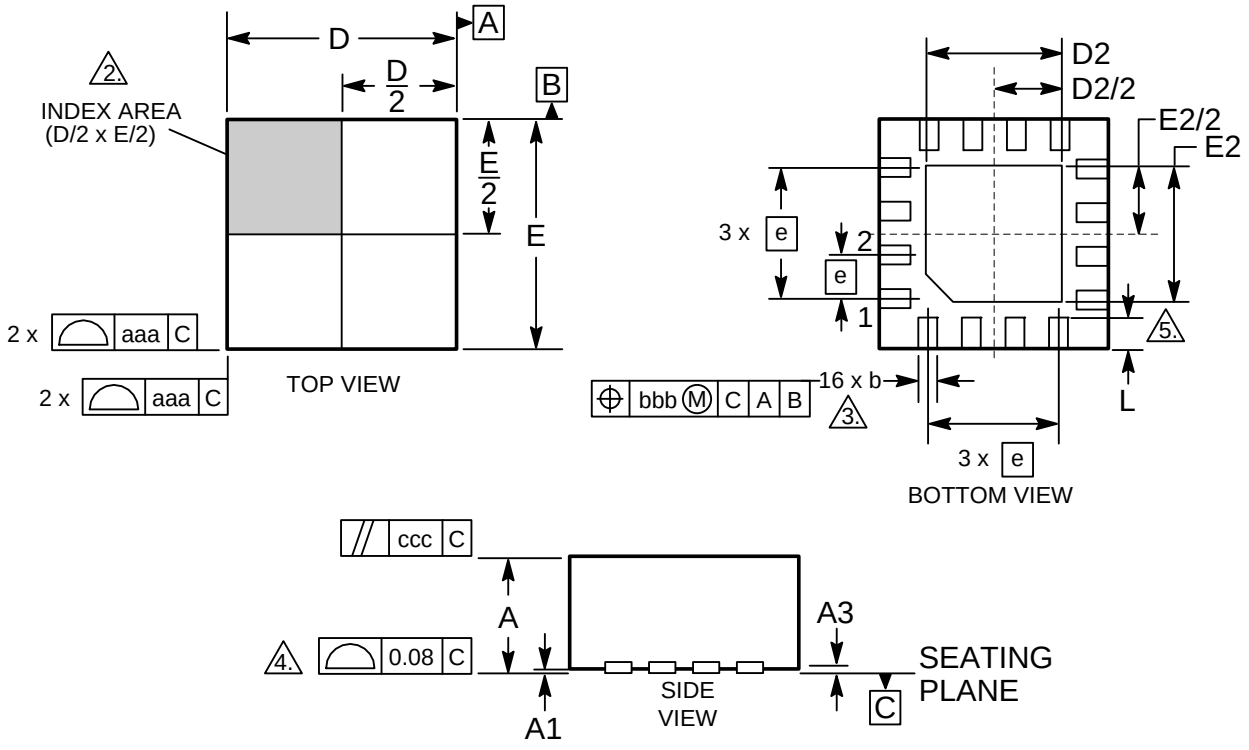
PACKAGE DIAGRAM
TSSOP 8



NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
2. MAXIMUM MOLD PROTRUSION FOR D IS 0.15mm.
3. MAXIMUM MOLD PROTRUSION FOR E IS 0.25mm.

DIM	MILLIMETERS	
	MIN	MAX
A		1.10
A_1	0.05	0.15
A_2	0.80	0.95
A_3	0.25	
b_p	0.25	0.45
c	0.15	0.28
D	2.90	3.10
E	2.90	3.10
e	0.65	
H_E	4.70	5.10
L	0.94	
L_p	0.40	0.70
v	0.10	
w	0.10	
y	0.10	
Z	0.35	0.70
θ	0^O	6^O

PACKAGE DIAGRAM
MLP 16

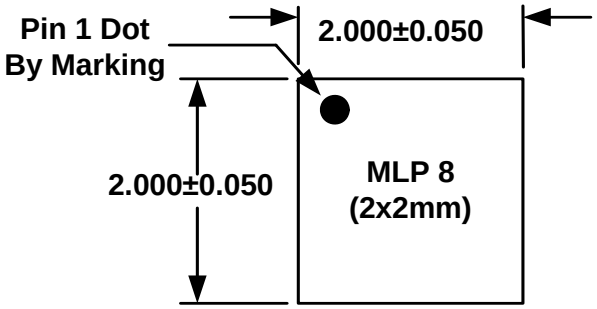


NOTES:

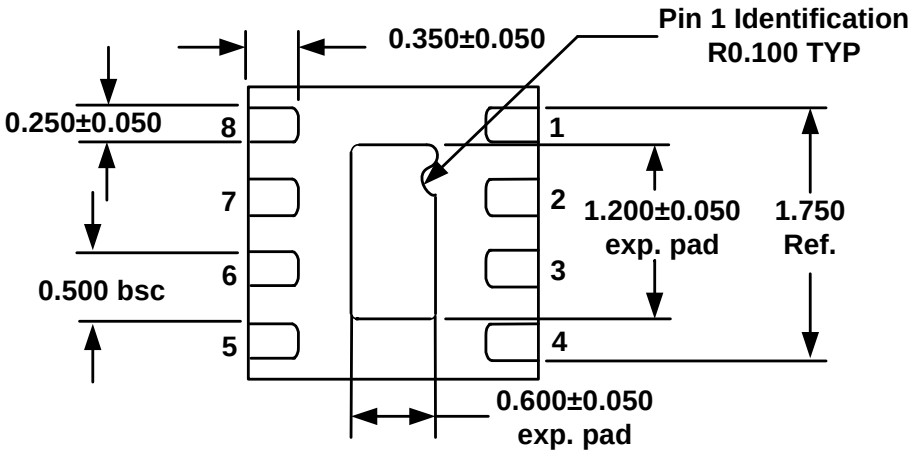
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME T14-1994.
2. THE TERMINAL #1 AND PAD NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012.
3. DIMENSION b APPLIES TO METALLIZED PAD AND IS MEASURED BETWEEN 0.25 AND 0.30 mm FROM PAD TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
5. INSIDE CORNERS OF METALLIZED PAD MAY BE SQUARE OR ROUNDED

	MILLIMETERS	
DIM	**MIN**	**MAX**
A	0.80	1.00
A1	0.00	0.05
A3	0.25 REF	
b	0.18	0.30
D	2.90	3.10
D2	0.25	1.95
E	2.90	3.10
E2	0.25	1.95
e	0.50 BSC	
L	0.30	0.50
aaa	0.25	
bbb	0.10	
ccc	0.10	

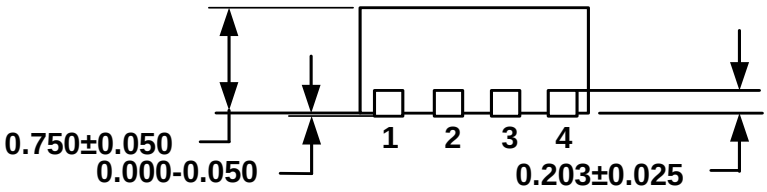
PACKAGE DIAGRAM
MLP 8 2x2mm



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Note: All dimensions are in mm