CS43L43

Low Voltage, Stereo DAC with Headphone Amp

Features

- ❑16-Pin TSSOP Package
- ❑1.8 to 3.3 Volt Supply
- ❑24-Bit Conversion / 96 kHz Sample Rate
- ❑94 dB Dynamic Range at 3 V Supply
- ❑-85 dB THD+N at 1.8 V Supply
- ❑Low Power Consumption
- ❑Digital Volume Control
  - 96 dB Attenuation, 1 dB Step Size
- ❑Digital Bass and Treble Boost
  - Selectable Corner Frequencies
  - Up to 12 dB Boost in 1 dB Increments
- ❑Peak Signal Limiting to Prevent Clipping
- ❑De-emphasis for 32 kHz, 44.1 kHz, and 48 kHz
- ❑Headphone Amplifier
  - up to 22 mW_{rms} Power Output into 16 Ω Load*
  - 25 dB Analog Attenuation and Mute
  - Zero Crossing Click-free Level Transitions
- ❑ATAPI Mixing Functions

* 1 kHz sine wave at 3.3V supply

Description

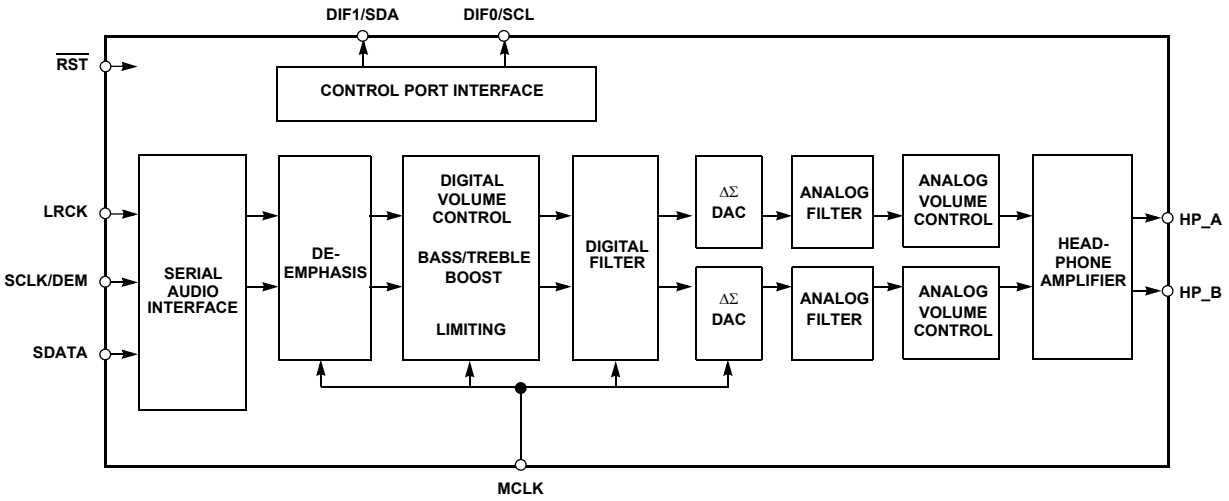
The CS43L43 is a complete stereo digital-to-analog output system including interpolation, 1-bit D/A conversion, analog filtering, volume control, and a headphone amplifier, in a 16-pin TSSOP package.

The CS43L43 is based on delta-sigma modulation, where the modulator output controls the reference voltage input to an ultra-linear analog low-pass filter. This architecture allows infinite adjustment of the sample rate between 2 kHz and 100 kHz simply by changing the master clock frequency.

The CS43L43 contains on-chip digital bass and treble boost, peak signal limiting and de-emphasis. The CS43L43 operates from a +1.8 V to +3.3 V supply and consumes only 16 mW of power with a 1.8 V supply. These features are ideal for portable CD, MP3 and MD players and other portable playback systems that require extremely low power consumption.

ORDERING INFORMATION

CS43L43-KZ	-10 to 70 °C	16-pin TSSOP
CS43L43-KZZ, Lead Free	-10 to 70 °C	16-pin TSSOP
CDB43L43		Evaluation Board



Preliminary Product Information

This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

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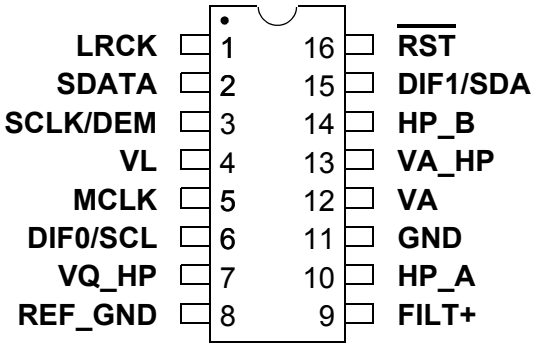
1.0 PIN DESCRIPTION



Pin Name	#	Pin Description
LRCK	1	**Left Right Clock** (*Input*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
SDATA	2	**Serial Audio Data** (*Input*) - Input for two's complement serial audio data.
SCLK	3	**Serial Clock** (*Input*) - Serial clock for the serial audio interface.
DEM	3	**De-emphasis Control** (*Input*) - Selects the standard 15µs/50µs digital de-emphasis filter response for 44.1 kHz sample rates.
VL	4	**Logic Power** (*Input*) - Positive power for the serial audio & control port interface.
MCLK	5	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters.
VQ_HP	7	**Headphone Quiescent Voltage** (*Output*) - Filter connection for internal headphone amp quiescent reference voltage.
REF_GND	8	**Reference Ground** (*Input*) - Ground reference for the internal sampling circuits.
FILT+	9	**Positive Voltage Reference** (*Output*) - Positive voltage reference for the internal sampling circuits.
HP_A **HP_B**	10 14	**Headphone Outputs** (*Output*) - The full-scale analog headphone output level is specified in the *Analog Characteristics* table.
GND	11	**Ground** (*Input*) - Ground reference.
VA	12	**Power** (*Input*) **-** Positive power for the analog & digital sections.
VA_HP	13	**Headphone Amp Power** (*Input*) - Positive power for the headphone amplifier.
$\overline{\text{RST}}$	16	**Reset** (*Input*) - Powers down device and resets registers to default conditions when enabled.
Stand-Alone Definitions		
DIF0 **DIF1**	6 15	**Digital Interface Format** (I*nput*) - Defines the required relationship between the Left Right Clock, Serial Clock, and Serial Audio Data.
Control Port Definitions		
SCL	6	**Serial Control Port Clock** (*Input*) - Serial clock for the control port interface.
SDA	15	**Serial Control Data I/O** (*Input*/*Output*) - Input/Output for I^2C data.

2.0 TYPICAL CONNECTION DIAGRAM

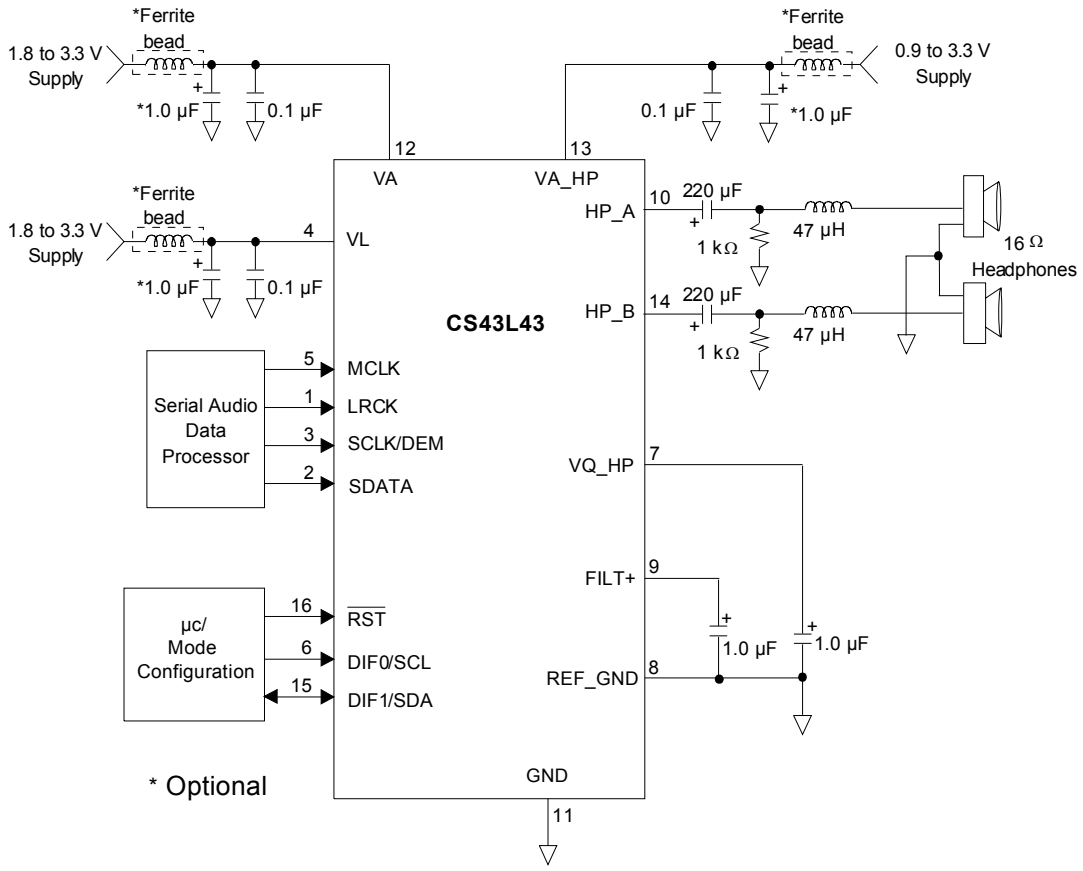


Figure 1. Typical Connection Diagram

3.0 APPLICATIONS

3.1 Sample Rate Range/Operational Mode Select

The device operates in one of two operational modes. Operation in either mode depends on the input sample rate and the ratio of the master clock to the left/right clock (see section 3.2). Sample rates outside the specified range for each mode are not supported.

Input Sample Rate (F_S)	MODE
2kHz - 50kHz	Single Speed Mode
50kHz - 100kHz	Double Speed Mode

Table 1. CS43L43 Operational Mode

3.2 System Clocking

The device requires external generation of the master (MCLK) and left/right (LRCK) clocks. The device also requires external generation of the serial clock (SCLK) if the internal serial clock is not used. The LRCK, defined also as the input sample rate F_S, must be synchronously derived from MCLK according to specified ratios. The specified ratios of MCLK to LRCK, along with several standard audio sample rates and the required MCLK frequency, are illustrated in Tables 2-3.

Sample Rate (kHz)	MCLK (MHz)				
	256x	384x	512x	768x*	1024x*
32	8.1920	12.2880	16.3840	24.5760	32.768
44.1	11.2896	16.9344	22.5792	33.8688	45.1584
48	12.2880	18.4320	24.5760	36.8640	49.1520

Table 2. Single-Speed Mode Standard Frequencies

Sample Rate (kHz)	MCLK (MHz)			
	128x	192x	256x*	384x*
64	8.1920	12.2880	16.3840	24.5760
88.2	11.2896	16.9344	22.5792	33.8688
96	12.2880	18.4320	24.5760	36.8640

Table 3. Double-Speed Mode Standard Frequencies

*Requires MCLKDIV bit = 1 in the Mode Control 2 register (address 0Bh).

3.2.1 Internal Serial Clock Mode

The device will enter the Internal Serial Clock Mode if no low to high transitions are detected on the SCLK pin for 2 consecutive periods of LRCK. In this mode, the SCLK is internally derived and synchronous with MCLK and LRCK. The SCLK/LRCK ratio is either 32, 48, or 64 depending upon the MCLK/LRCK ratio and the Digital Interface Format selection (see Table 4).

The internal serial clock is utilized when de-emphasis control is required. Operation in the Internal Serial Clock mode is identical to operation with an external SCLK synchronized with LRCK; however, External SCLK mode is the recommended system clocking application.

Input MCLK/LRCK Ratio	Digital Interface Format Selection					Internal SCLK/LRCK Ratio
	I^2S up to 24 Bits	*I^2S 16 Bits*	*Left Justified 24 Bits*	*Right Justified 24, 20, or 18 Bits*	*Right Justified 16 Bits*	
512, 256, 128		X			X	32
384, 192	X		X	X	X	48
512, 256, 128	X		X	X		64

Table 4. Internal SCLK/LRCK Ratio

3.2.2 External Serial Clock Mode

The device will enter the External Serial Clock Mode whenever 16 low to high transitions are detected on the SCLK pin during any phase of the LRCK period. The device will revert to Internal Serial Clock Mode if no low to high transitions are detected on the SCLK pin for 2 consecutive periods of LRCK.

3.3 Digital Interface Format

The device will accept audio samples in 1 of 4 digital interface formats in Stand-Alone mode, as illustrated in Table 5, and 1 of 7 formats in Control Port mode, as illustrated in Table 14.

3.3.1 Stand-Alone Mode

The desired format is selected via the DIF0 and DIF1 pins. For an illustration of the required relationship between the LRCK, SCLK and SDATA, see Figures 2-4.

DIF1	DIF0	DESCRIPTION	FORMAT	FIGURE
0	0	I^2S, up to 24-bit data	0	2
0	1	Left Justified, up to 24-bit data	1	3
1	0	Right Justified, 24-bit Data	2	4
1	1	Right Justified, 16-bit Data	3	4

Table 5. Digital Interface Format - Stand-Alone Mode

3.3.2 Control Port Mode

The desired format is selected via the DIF0, DIF1 and DIF2 bits in the Mode Control 2 register (see section 5.11.2) . For an illustration of the required relationship between LRCK, SCLK and SDATA, see Figures 2-4.

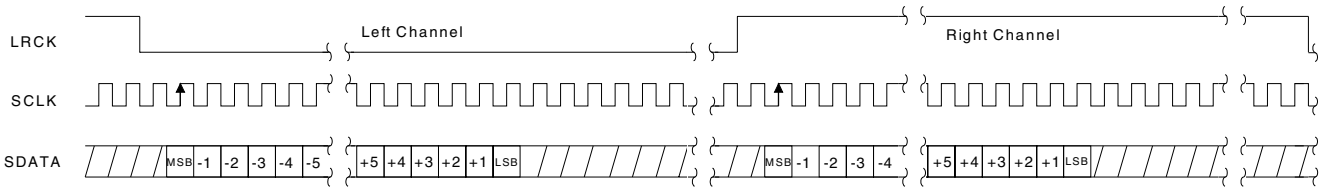


Figure 2. I²S Data

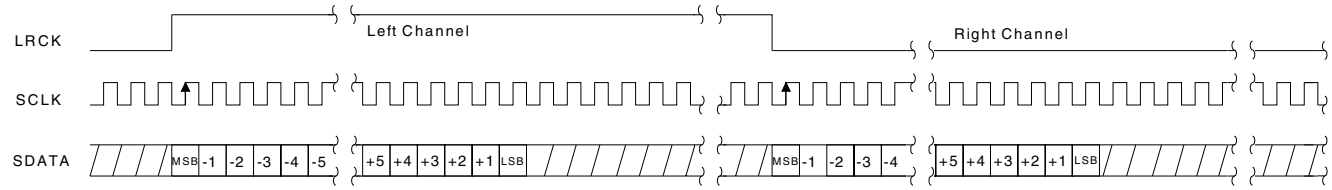


Figure 3. Left Justified up up to 24-Bit Data

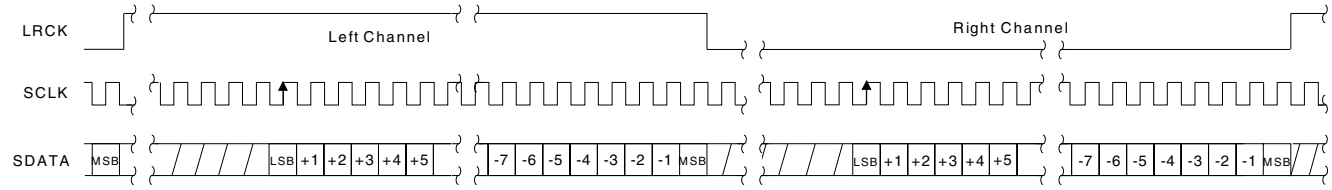


Figure 4. Right Justified Data

3.4 De-Emphasis Control

The device includes on-chip digital de-emphasis. Figure 5 shows the de-emphasis curve for F_s equal to 44.1 kHz. The frequency response of the de-emphasis curve will scale proportionally with changes in sample rate, Fs. De-emphasis is not available in double-speed mode.

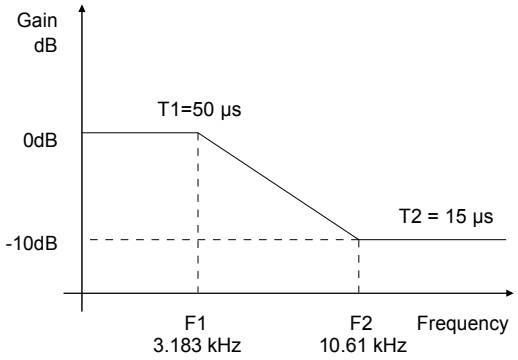


Figure 5. De-Emphasis Curve

3.4.1 Stand-Alone Mode

When using Internal Serial Clock (see section 3.2.1), pin 3 is available for de-emphasis control and selects the 44.1 kHz de-emphasis filter. Please see Table 6 for the desired de-emphasis control.

DEM	DESCRIPTION
0	Disabled
1	44.1 kHz

Table 6. De-Emphasis Control

3.4.2 Control Port Mode

The Mode Control bits select either the 32, 44.1, or 48 kHz de-emphasis filter. Please see section 5.7.4 for the desired de-emphasis control.

3.5 Recommended Power-up Sequence

3.5.1 Stand-Alone Mode

1. Hold $\overline{\text{RST}}$ low until the power supply and configuration pins are stable, and the master and left/right clocks are locked to the appropriate frequences, as discussed in section 3.2. In this state, the control port is reset to its default settings and VQ_HP will remain low.

2. Bring $\overline{\text{RST}}$ high. The device will remain in a low power state with VQ_HP low and will initiate the Stand-Alone power-up sequence after approximately 1024 LRCK cycles.

3.5.2 Control Port Mode

1. Hold $\overline{\text{RST}}$ low until the power supply is stable, and the master and left/right clocks are locked to the appropriate frequences, as discussed in section 3.2. In this state, the control port is reset to its default settings and VQ_HP will remain low.

2. Bring $\overline{\text{RST}}$ high. The device will remain in a low power state with VQ_HP low. The control port will be accessible at this time.

3. Wait approximately 2 LRCK cycles and then perform an I^2C write to the CP_EN bit prior to the completion of approximately 1024 LRCK cycles. The desired register settings can be loaded while keeping the PDN bit set to 1.

4. Set the PDN bit to 0. This will initiate the power-up sequence, which lasts approximately 50 µS when the POR bit is set to 0. If the POR bit is set to 1, see Section 3.6 for for a complete description of power-up timing.

3.6 Popguard® Transient Control

The CS43L43 uses Popguard® technology to minimize the effects of output transients during power-up and power-down. This technology, when used with external DC-blocking capacitors in series with the audio outputs, minimizes the audio transients commonly produced by single-ended single-supply converters. It is activated inside the DAC when the $\overline{\text{RST}}$ pin is enabled/disabled and requires no other external control, aside from choosing the appropriate DC-blocking capacitors.

3.6.1 Power-up

When the device is initially powered-up, the audio outputs, HP_A and HP_B, are clamped to GND. Following a delay of approximately 1000 sample periods, each output begins to ramp toward the quiescent voltage. Approximately 10,000 LRCK cycles later, the outputs reach V_Q and audio output begins. This gradual voltage ramping allows time for the external DC-blocking capacitors to charge to the quiescent voltage, minimizing the power-up transient.

3.6.2 Power-down

To prevent transients at power-down, the device must first enter its power-down state by setting the $\overline{\text{RST}}$ pin low. When this occurs, audio output ceases and the internal output buffers are disconnected from HP_A and HP_B. In their place, a soft-start current sink is substituted which allows the DC-blocking capacitors to slowly discharge. Once this charge is dissipated, the power to the device may be turned off and the system is ready for the next power-on.

3.6.3 Discharge Time

To prevent an audio transient at the next power-on, the DC-blocking capacitors must fully discharge before turning on the power or exiting the power-down state. If full discharge does not occur, a transient will occur when the audio outputs are initially clamped to GND. The time that the device must remain in the power-down state is related to the value of the DC-blocking capacitance and the output load. For example, with a 220 µF capacitor and a 16 Ω load, the minimum power-down time will be approximately 0.4 seconds.

3.6.4 Auxilliary Mute Control

For critical applications, the Popguard® Transient Control may not be sufficient in eliminating extraneous audible artifacts on the headphone outputs during power-up. For these applications, an optional external mute can be used to maintain an absolute minimum of extraneous clicks and pops. Please see Figures 6 and 7 for the suggested headphone mute circuit.

The Mute Control will need to be generated externally from a DSP or Microcontroller. See Figure 7 for /RST and Mute Control timing.

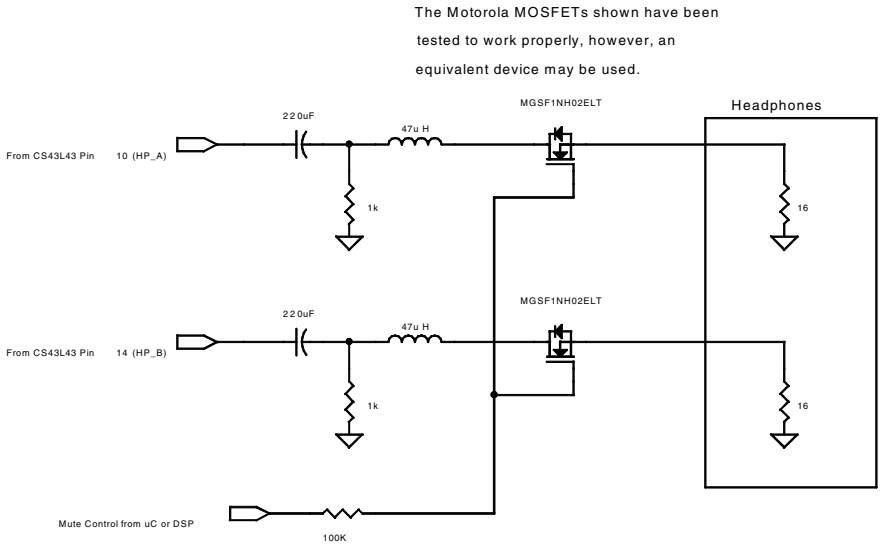


Figure 6. Optional Headphone Mute Circuit

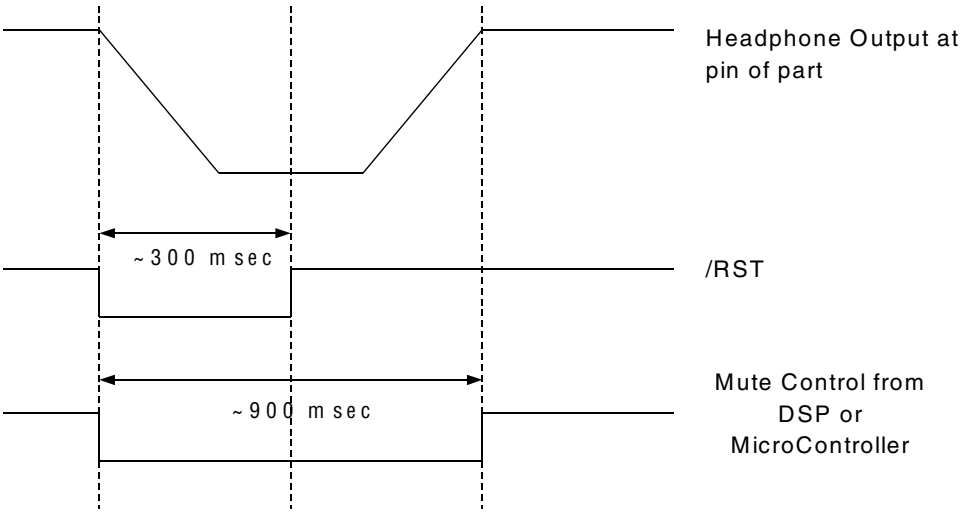


Figure 7. Timing for Headphone Mute

3.7 Grounding and Power Supply Arrangements

As with any high resolution converter, the CS43L43 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 shows the recommended power arrangements, with VA, VA_HP & VL connected to clean supplies. If the ground planes are split between digital ground and analog ground, the GND pins of the CS43L43 should be connected to the analog ground plane.

All signals, especially clocks, should be kept away from the FILT+ and VQ pins in order to avoid unwanted coupling into the modulators. The CDB43L43 evaluation board demonstrates the optimum layout and power supply arrangements.

Notes: The headphone outputs may clip when the value of VA_HP is below VA. It is recommended that these two supplies be tied together.

3.7.1 Capacitor Placement

Decoupling capacitors should be as close to the DAC as possible, with the low value ceramic capacitor being the closest. The FILT+ and VQ decoupling capacitors must be positioned to minimize the electrical path from FILT+ to REF_GND (and VQ to REF_GND). To further minimze impedance, these capacitors should be located on the same layer as the DAC.

3.8 Control Port Interface

The control port is used to load all the internal register settings. Data is clocked into and out of the bi-directional serial control data line, SDA, by the serial control port clock, SCL (see Figure 8 for the clock to data relationship). The operation of the control port may be completely asynchronous with the audio sample rate. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

Notes: LRCK & MCLK must always be applied to pins 1 & 5, respectively, during any communication with the control port.

3.8.1 Enabling the Control Port

The control port pins are shared with the stand-alone configuration pins. To dedicate these pins to control port functionality, enable the control port prior to the completion of the stand-alone power up sequence (see section 3.5 for the Recommended Power-up Sequence). To enable the control port, write 1 to the CP_EN bit using the I^2C protocol (see section 3.8.3).

Notes: Setting the CP_EN bit after the Stand-Alone power-up sequence has completed can cause audible artifacts.

3.8.2 MAP Auto Increment

The device has MAP (memory address pointer) auto increment capability enabled by the INCR bit (also the MSB) of the MAP. If INCR is set to 0, MAP will stay constant for successive I^2C writes or reads. If INCR is set to 1, MAP will auto increment after each byte is written, allowing block reads or writes of successive registers.

3.8.3 I²C Write

To write to the device, follow the procedure below while adhering to the control port Switching Specifications in section 6.

1) Initiate a START condition to the I²C bus followed by the address byte, 00100000. The eighth bit of the address byte is the R/$\overline{W}$ bit.

2) Wait for an acknowledge (ACK) from the part, then write to the memory address pointer, MAP. This byte points to the register to be written.

3) Wait for an acknowledge (ACK) from the part, then write the desired data to the register pointed to by the MAP.

4) If the INCR bit (see section 3.8.2) is set to 1, repeat the previous step until all the desired registers are written, then initiate a STOP condition to the bus.

5) If the INCR bit is set to 0 and further I²C writes to other registers are desired, it is necessary to initiate a repeated START condition and follow the procedure detailed from step 1. If no further writes to other registers are desired, initiate a STOP condition to the bus.

3.8.4 I²C Read

To read from the device, follow the procedure below while adhering to the control port Switching Specifications.

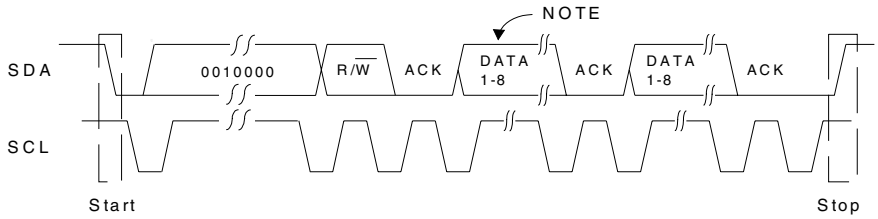
1) Initiate a START condition to the I²C bus followed by the address byte, 00100001. The eighth bit of the address byte is the R/$\overline{W}$ bit.

2) After transmitting an acknowledge (ACK), the device will then transmit the contents of the register pointed to by the MAP. The MAP will contain the address of the last register written to the MAP, or the default address (see section 3.9) if an I²C read is the first operation performed on the device.

3) Once the device has transmitted the contents of the register pointed to by the MAP, issue an ACK.

4) If the INCR bit is set to 1, the device will continue to transmit the contents of successive registers. Continue providing a clock and issue an ACK after each byte until all the desired registers are read, then initiate a STOP condition to the bus.

5) If the INCR bit is set to 0 and further I²C reads from other registers are desired, it is necessary to initiate a repeated START condition and follow the procedure detailed from step 1. If no further reads from other registers are desired, initiate a STOP condition to the bus.



NOTE: If operation is a write, this byte contains the Memory Address Pointer, MAP. If operation is a read, this byte contains the data of the register pointed to by the MAP.

Figure 8. Control Port Timing

3.9 Memory Address Pointer (MAP)

7	6	5	4	3	2	1	0
INCR	Reserved	Reserved	Reserved	MAP3	MAP2	MAP1	MAP0
0	0	0	0	0	0	0	0

3.9.1 INCR (Auto Map Increment Enable)

Default = '0'
0 - Disabled
1 - Enabled

3.9.2 MAP0-3 (Memory Address Pointer)

Default = '0000'

4.0 REGISTER QUICK REFERENCE

Addr	Function	7	6	5	4	3	2	1	0
0h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	default	0	0	0	0	0	0	0	0
1h	Power and Muting Control	AMUTE	SZC1	SZC0	POR	Reserved	Reserved	PDN	CP_EN
	default	1	1	0	1	0	0	1	0
2h	Channel A Analog Attenuation Control	VOLA7	VOLA6	VOLA5	VOLA4	VOLA3	VOLA2	VOLA1	VOLA0
	default	0	0	0	0	0	0	0	0
3h	Channel B Analog Attenuation Control	VOLB7	VOLB6	VOLB5	VOLB4	VOLB3	VOLB2	VOLB1	VOLB0
	default	0	0	0	0	0	0	0	0
4h	Channel A Digital Volume Control	DVOLA7	DVOLA6	DVOLA5	DVOLA4	DVOLA3	DVOLA2	DVOLA1	DVOLA0
	default	0	0	0	0	0	0	0	0
5h	Channel B Digital Volume Control	DVOLB7	DVOLB6	DVOLB5	DVOLB4	DVOLB3	DVOLB2	DVOLB1	DVOLB0
	default	0	0	0	0	0	0	0	0
6h	Tone Control	BB3	BB2	BB1	BB0	TB3	TB2	TB1	TB0
	default	0	0	0	0	0	0	0	0
7h	Mode Control	BBCF1	BBCF0	TBCF1	TBCF0	A=B	DEM1	DEM0	VCBYP
	default	0	0	0	0	0	0	0	0
8h	Limiter Attack Rate	ARATE7	ARATE6	ARATE5	ARATE4	ARATE3	ARATE2	ARATE1	ARATE0
	default	0	0	0	1	0	0	0	0
9h	Limiter Release Rate	RRATE7	RRATE6	RRATE5	RRATE4	RRATE3	RRATE2	RRATE1	RRATE0
	default	0	0	1	0	0	0	0	0
Ah	Volume and Mixing Control	TC1	TC0	TC_EN	LIM_EN	ATAPI3	ATAPI2	ATAPI1	ATAPI0
	default	0	0	0	0	1	0	0	1
Bh	Mode Control 2	MCLKDIV	Reserved	Reserved	Reserved	Reserved	DIF2	DIF1	DIF0
	default	0	0	0	0	0	0	0	0

5.0 REGISTER DESCRIPTIONS

5.1 POWER AND MUTING CONTROL (ADDRESS 01H)

7	6	5	4	3	2	1	0
AMUTE	SZC1	SZC0	POR	RESERVED	RESERVED	PDN	CP_EN
1	1	0	1	0	0	1	0

5.1.1 AUTO-MUTE (AMUTE) BIT 7

Default = 1
0 - Disabled
1 - Enabled

Function:

The Digital-to-Analog converter output will mute following the reception of 8192 consecutive audio samples of static 0 or -1. A single sample of non-static data will release the mute. Detection and muting is done independently for each channel. The quiescent voltage on the output will be retained. The muting function is affected, similar to volume control changes, by the Soft and Zero Cross bits in the Power and Muting Control register.

5.1.2 SOFT RAMP AND ZERO CROSS CONTROL (SZC) BIT 5-6

Default = 10
00 - Immediate Change
01 - Zero Cross Digital and Analog
10 - Ramped Digital and Analog
11 - Reserved

Function:

Immediate Change

When Immediate Change is selected all level changes will take effect immediately in one step.

Zero Cross Digital and Analog

Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a timeout period of 512 sample periods (10.7 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

Ramped Digital and Analog

Soft Ramp allows digital level changes, both muting and attenuation, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1dB per 8 left/right clock periods. Analog level changes will occur in 1 dB steps on a signal zero crossing. The analog level change will occur after a timeout period of 512 sample periods (10.7 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

NOTE: Ramped Digital and Analog is not available in Double-Speed mode.

5.1.3 POPGUARD® TRANSIENT CONTROL (POR) BIT 4

Default - 1
0 - Disabled
1 - Enabled

Function:

The Popguard® Transient Control allows the quiescent voltage to slowly ramp to and from 0 volts to the quiescent voltage during power-on or power-off when this feature is enabled. Please see section 3.6 for implementation details.

5.1.4 POWER DOWN (PDN) BIT 1

Default = 1
0 - Disabled
1 - Enabled

Function:

The entire device will enter a low-power state whenever this function is enabled, but the contents of the control registers will be retained in this mode. The power-down bit defaults to ‘enabled’ on power-up and must be disabled before normal operation will begin.

5.1.5 CONTROL PORT ENABLE (CP_EN) BIT 0

Default = 0
0 - Disabled
1 - Enabled

Function:

The Control Port will become active and reset to the default settings when this function is enabled.

5.2 CHANNEL A ANALOG ATTENUATION CONTROL (ADDRESS 02H) (VOLA)

5.3 CHANNEL B ANALOG ATTENUATION CONTROL (ADDRESS 03H) (VOLB)

7	6	5	4	3	2	1	0
VOLx7	VOLx6	VOLx5	VOLx4	VOLx3	VOLx2	VOLx1	VOLx0
0	0	0	0	0	0	0	0

Default = 0 dB (No attenuation)

Function:

The Analog Attenuation Control operates independently from the Digital Volume Control. The Analog Attenuation Control registers allow the user to attenuate the headphone output signal in 1 dB increments from 0 to -25 dB, using the analog volume control. Attenuation settings are decoded as shown in Table 7, using a 2's complement code. The volume changes are implemented as dictated by the Soft and Zero Cross bits in the Power and Muting Control register. All volume settings greater than zero are interpreted as zero.

Binary Code	Decimal Value	Volume Setting
00000000	0	0 dB
11110110	-10	-10 dB
11110001	-15	-15 dB

Table 7. Example Analog Volume Settings

NOTE: When the Analog Headphone Attenuation Control registers are set for attenuation levels greater than -10dB, the actual attenuation deviates from the register setting by more than 1dB.

5.4 CHANNEL A DIGITAL VOLUME CONTROL (ADDRESS 04H) (DVOLA)

5.5 CHANNEL B DIGITAL VOLUME CONTROL (ADDRESS 05H) (DVOLB)

7	6	5	4	3	2	1	0
DVOLx7	DVOLx6	DVOLx5	DVOLx4	DVOLx3	DVOLx2	DVOLx1	DVOLx0
0	0	0	0	0	0	0	0

Default = 0 dB (No attenuation)

Function:

The Digital Volume Control allows the user to alter the signal level in 1 dB increments from +18 to -96 dB, using the Digital Volume Control. Volume settings are decoded as shown in Table 8, using a 2's complement code. The volume changes are implemented as dictated by the Soft and Zero Cross bits in the Power and Muting Control register. All volume settings less than - 96 dB are equivalent to muting the channel via the ATAPI bits (See Section 5.10.4).

NOTE: Setting this register to values greater than +18 dB will cause distortion in the audio outputs.

Binary Code	Decimal Value	Volume Setting
00001010	12	+12 dB
00000111	7	+7 dB
00000000	0	0 dB
11000100	-60	-60 dB
10100110	-90	-90 dB

Table 8. Example Digital Volume Settings

5.6 TONE CONTROL (ADDRESS 06H)

7	6	5	4	3	2	1	0
BB3	BB2	BB1	BB0	TB3	TB2	TB1	TB0
0	0	0	0	0	0	0	0

5.6.1 BASS BOOST LEVEL (BB) BIT 4-7

Default = 0 dB (No Bass Boost)

Function:

The level of the shelving bass boost filter is set by Bass Boost Level. The level can be adjusted in 1 dB increments from 0 to +12 dB of boost. Boost levels are decoded as shown in Table 9. Levels above +12 dB are interpreted as +12 dB.

Binary Code	Decimal Value	Boost Setting
0000	0	0 dB
0010	2	+2 dB
0110	6	+6 dB
1001	9	+9 dB
1100	12	+12 dB

Table 9. Example Bass Boost Settings

5.6.2 TREBLE BOOST LEVEL (TB) BIT 0-3

Default = 0 dB (No Treble Boost)

Function:

The level of the shelving treble boost filter is set by Treble Boost Level. The level can be adjusted in 1 dB increments from 0 to +12 dB of boost. Boost levels are decoded as shown in Table 10. Levels above +12 dB are interpreted as +12 dB.

NOTE: Treble Boost is not available in Double-Speed Mode.

Binary Code	Decimal Value	Boost Setting
0000	0	0 dB
0010	2	+2 dB
1010	6	+6 dB
1001	9	+9 dB
1100	12	+12 dB

Table 10. Example Treble Boost Settings

5.7 MODE CONTROL (ADDRESS 07H)

7	6	5	4	3	2	1	0
BBCF1	BBCF0	TBCF1	TBCF0	A=B	DEM1	DEM0	VCBYP
0	0	0	0	0	0	0	0

5.7.1 BASS BOOST CORNER FREQUENCY (BBCF) BIT 6-5

Default = 00
00 - 50 Hz
01 - 100 Hz
10 - 200 Hz
11 - Reserved

Function:

The bass boost corner frequency is user selectable as shown above.

5.7.2 TREBLE BOOST CORNER FREQUENCY (TBCF) BIT 4-5

Default = 00
00 - 2 kHz
01 - 4 kHz
10 - 7 kHz
11 - Reserved

Function:

The treble boost corner frequency is user selectable as shown above. NOTE: Treble Boost is not available in Double-Speed Mode.

5.7.3 CHANNEL A VOLUME = CHANNEL B VOLUME (A=B) BIT 3

Default = 0
0 - Disabled
1 - Enabled

Function:

The HP_A and HP_B volume levels are independently controlled by the A and B Channel Volume Control Bytes when this function is disabled. The volume on both HP_A and HP_B are determined by the A Channel Attenuation and Volume Control Bytes. The B Channel Bytes are ignored when this function is enabled.

5.7.4 DE-EMPHASIS CONTROL (DEM) BIT 1-2

Default = 00
00 - Disabled
01 - 44.1 kHz
10 - 48 kHz
11 - 32 kHz

Function:

Selects the appropriate digital filter to maintain the standard 15 μs/50 μs digital de-emphasis filter response at 32, 44.1 or 48 kHz sample rates. (See Figure 5) NOTE: De-emphasis is not available in Double-Speed Mode.

5.7.5 DIGITAL VOLUME CONTROL BYPASS (VCBYP) BIT 0

Default = 0
0 - Disabled
1 - Enabled

Function:

When this function is enabled the digital volume control section is bypassed. This disables the digital volume control, muting, bass boost, treble boost, limiting and ATAPI functions. The analog attenuation control will remain functional.

5.8 LIMITER ATTACK RATE (ADDRESS 08H) (ARATE)

7	6	5	4	3	2	1	0
ARATE7	ARATE6	ARATE5	ARATE4	ARATE3	ARATE2	ARATE1	ARATE0
0	0	0	1	0	0	0	0

Default = 10h - 2 LRCK's per 1/8 dB

Function:

The limiter attack rate is user selectable. The rate is a function of sampling frequency, Fs, and the value in the Limiter Attack Rate register. Rates are calculated using the function RATE = 32/{value}. Where {value} is the decimal value in the Limiter Attack Rate register and RATE is in LRCK's per 1/8 dB of change. NOTE: A value of zero in this register is not recommended, as it will induce erratic behavior of the limiter. Use the LIM_EN bit to disable the limiter function (see Section 5.10.3).

Binary Code	Decimal Value	LRCK's per 1/8 dB
00000001	1	32
00010100	20	1.6
00101000	40	0.8
00111100	60	0.53
01011010	90	0.356

Table 11. Example Limiter Attack Rate Settings

5.9 LIMITER RELEASE RATE (ADDRESS 09H) (RRATE)

7	6	5	4	3	2	1	0
RRATE7	RRATE6	RRATE5	RRATE4	RRATE3	RRATE2	RRATE1	RRATE0
0	0	1	0	0	0	0	0

Default = 20h - 16 LRCK's per 1/8 dB

Function:

The limiter release rate is user-selectable. The rate is a function of sampling frequency, Fs, and the value in Limiter Release Rate register. Rates are calculated using the function RATE = 512/{value}. Where {value} is the decimal value in the Limiter Release Rate register and RATE is in LRCK's per 1/8 dB of change.

NOTE: A value of zero in this register is not recommended, as it will induce erratic behavior of the limiter. Use the LIM_EN bit to disable the limiter function (see Section 5.10.3).

Binary Code	Decimal Value	LRCK's per 1/8 dB
00000001	1	512
00010100	20	25
00101000	40	12
00111100	60	8
01011010	90	5

Table 12. Example Limiter Release Rate Settings

5.10 VOLUME AND MIXING CONTROL (ADDRESS 0AH)

7	6	5	4	3	2	1	0
TC1	TC0	TC_EN	LIM_EN	ATAPI3	ATAPI2	ATAPI1	ATAPI0
0	0	0	0	1	0	0	1

5.10.1 TONE CONTROL MODE (TC) BIT 6-7

Default = 00
00 - All settings are taken from user registers
01 - 12 dB of Bass Boost at 100 Hz and 6 dB of Treble Boost at 7 kHz
10 - 8 dB of Bass Boost at 100 Hz and 4 dB of Treble Boost at 7 kHz
11 - 4 dB of Bass Boost at 100 Hz and 2 dB of Treble Boost at 7 kHz

Function:

The Tone Control Mode bits determine how the Bass Boost and Treble Boost features are configured. The user-defined settings from the Bass and Treble Boost Level and Corner Frequency registers are used when these bits are set to '00'. Alternatively, one of three pre-defined settings may be used.

5.10.2 TONE CONTROL ENABLE (TC_EN) BIT 5

Default = 0
0 - Disabled
1 - Enabled

Function:

The Bass Boost and Treble Boost features are active when this function is enabled.

5.10.3 PEAK SIGNAL LIMITER ENABLE (LIM_EN) BIT 4

Default = 0
0 - Disabled
1 - Enabled

Function:

The CS43L43 will limit the maximum signal amplitude to prevent clipping when this function is enabled. Peak Signal Limiting is performed by first decreasing the Bass and Treble Boost Levels. If the signal is still clipping, then the digital attenuation is increased. The attack rate is determined by the Limiter Attack Rate register.

Once the signal has dropped below the clipping level, the attenuation is decreased back to the user selected level and then, the Bass Boost is increased back to the user selected level. The release rate is determined by the Limiter Release Rate register.

NOTE: The A=B bit should be set to '1' for optimal limiter performance.

5.10.4 ATAPI CHANNEL MIXING AND MUTING (ATAPI) BIT 0-3

Default = 1001 - HP_A = L, HP_B = R (Stereo)

Function:

The CS43L43 implements the channel mixing functions of the ATAPI CD-ROM specification. Refer to Table 13 and Figure 9 for additional information.

NOTE: All mixing functions occur prior to the digital volume control.

ATAPI3	ATAPI2	ATAPI1	ATAPI0	HP_A	HP_B
0	0	0	0	MUTE	MUTE
0	0	0	1	MUTE	R
0	0	1	0	MUTE	L
0	0	1	1	MUTE	[(L+R)/2]
0	1	0	0	R	MUTE
0	1	0	1	R	R
0	1	1	0	R	L
0	1	1	1	R	[(L+R)/2]
1	0	0	0	L	MUTE
1	0	0	1	L	R
1	0	1	0	L	L
1	0	1	1	L	[(L+R)/2]
1	1	0	0	[(L+R)/2]	MUTE
1	1	0	1	[(L+R)/2]	R
1	1	1	0	[(L+R)/2]	L
1	1	1	1	[(L+R)/2]	[(L+R)/2]

Table 13. ATAPI Decode

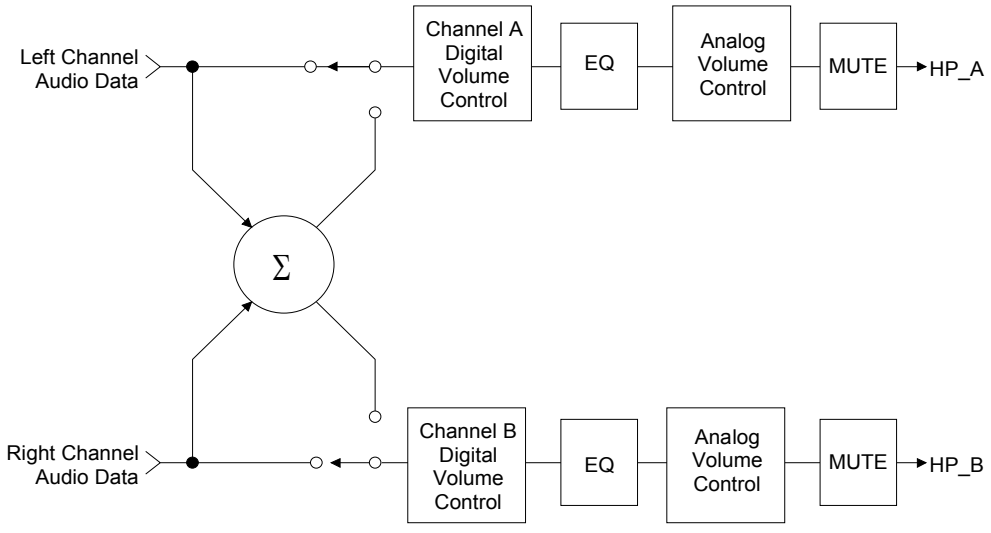


Figure 9. ATAPI Block Diagram

5.11 MODE CONTROL 2 (ADDRESS 0BH)

7	6	5	4	3	2	1	0
MCLKDIV	RESERVED	RESERVED	RESERVED	RESERVED	DIF2	DIF1	DIF0
0	0	0	0	0	0	0	0

5.11.1 MASTER CLOCK DIVIDE ENABLE (MCLKDIV) BIT 7

Default = 0
0 - Disabled
1 - Enabled

Function:

The MCLKDIV bit enables a circuit which divides the externally applied MCLK signal by 2 prior to all other internal circuitry.

NOTE: Internal SCLK is not available when this function is enabled.

5.11.2 DIGITAL INTERFACE FORMAT (DIF) BIT 0-2

Default = 000 - Format 0 (I^2S, up to 24-bit data, 64 x Fs Internal SLCK)

Function:

The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format and the options are detailed in Figures 2-4.

NOTE: Internal SCLK is not available when MCLKDIV is enabled.

DIF2	DIF1	DIF0	DESCRIPTION	Format	FIGURE
0	0	0	I^2S, up to 24-bit data, 64 x Fs Internal SLCK	0	2
0	0	1	I^2S, up to 16-bit data, 32 x Fs Internal SLCK	1	2
0	1	0	Left Justified, up to 24-bit data,	2	3
0	1	1	Right Justified, 24-bit data	3	4
1	0	0	Right Justified, 20-bit data	4	4
1	0	1	Right Justified, 16-bit data	5	4
1	1	0	Right Justified, 18-bit data	6	4
1	1	1	Identical to Format 1	1	2

Table 14. Digital Interface Format - Control Port Mode

6.0 CHARACTERISTICS AND SPECIFICATIONS

ANALOG CHARACTERISTICS (CS43L43-KZ, KZZ)

(Test conditions (unless otherwise specified): Input test signal is a 997 Hz sine wave at 0 dBFS; measurement bandwidth is 10 Hz to 20 kHz; test load R_L = 16Ω, C_L = 10 pF (see Figure 10). Typical performance characteristics are derived from measurements taken at T_A = 25°C, VL = VA_HP = VA = 3.0V and 1.8V. Min/Max performance characteristics are guaranteed over the specified operating temperature and voltages.)

Parameter		VA = 3.0V Min	VA = 3.0V Typ	VA = 3.0V Max	VA = 1.8V Min	VA = 1.8V Typ	VA = 1.8V Max	Unit
Single-Speed Mode	**Fs = 48kHz**							
Dynamic Range	(Note 1)							
18 to 24-Bit	unweighted	88	91	-	85	88	-	dB
	A-Weighted	90	93	-	88	91	-	dB
16-Bit	unweighted	-	89	-	-	86	-	dB
	A-Weighted	-	91	-	-	89	-	dB
Total Harmonic Distortion + Noise	(Note 1)							
18 to 24-Bit	0 dB	-	-76	-71	-	-82	-77	dB
	-20 dB	-	-71	-	-	-68	-	dB
	-60 dB	-	-31	-	-	-28	-	dB
16-Bit	0 dB	-	-74	-	-	-80	-	dB
	-20 dB	-	-69	-	-	-66	-	dB
	-60 dB	-	-29	-	-	-26	-	dB
Double-Speed Mode	**Fs = 96kHz**							
Dynamic Range	(Note 1)							
18 to 24-Bit	unweighted	88	92	-	85	89	-	dB
	A-Weighted	90	94	-	88	92	-	dB
16-Bit	unweighted	-	90	-	-	87	-	dB
	A-Weighted	-	92	-	-	90	-	dB
Total Harmonic Distortion + Noise	(Note 1)							
18 to 24-Bit	0 dB	-	-73	-68	-	-85	-80	dB
	-20 dB	-	-72	-	-	-69	-	dB
	-60 dB	-	-32	-	-	-29	-	dB
16-Bit	0 dB	-	-71	-	-	-83	-	dB
	-20 dB	-	-70	-	-	-67	-	dB
	-60 dB	-	-30	-	-	-27	-	dB

ANALOG CHARACTERISTICS (CS43L43-KZ, KZZ) (Continued)

Parameters		Min	Typ	Max	Units
Dynamic Performance for All Speed Modes					
Interchannel Isolation	(1 kHz)	-	66	-	dB
DC Accuracy					
Interchannel Gain Mismatch		-	0.1	-	dB
Gain Drift		-	±100	-	ppm/°C
Analog Output Characteristics					
Full Scale Output Voltage		0.5•VA	0.55•VA	0.6•VA	Vpp

Notes: 1. One-half LSB of triangular PDF dither is added to data.

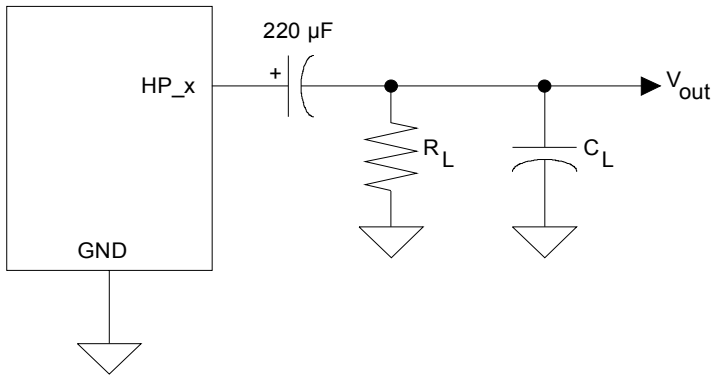


Figure 10. Output Test Load

COMBINED INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE (The filter characteristics and the X-axis of the response plots have been normalized to the sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs.)

Parameter		Min	Typ	Max	Unit
Single-Speed Mode - (2kHz to 50kHz sample rates)					
Passband					
	to -0.05 dB corner	0	-	0.4535	Fs
	to -3 dB corner	0	-	0.4998	Fs
Frequency Response 10 Hz to 20 kHz	(Note 2)	-0.02	-	+0.08	dB
StopBand		0.5465	-	-	Fs
StopBand Attenuation	(Note 3)	50	-	-	dB
Group Delay		-	9/Fs	-	s
Passband Group Delay Deviation	0 - 20 kHz	-	±0.36/Fs	-	s
De-emphasis Error (Relative to 1 kHz)	Fs = 32 kHz	-	-	+0.2/-0.1	dB
(Note 4)	Fs = 44.1 kHz	-	-	+0.05/-0.14	
	Fs = 48 kHz	-	-	+0/-0.22	
Double-Speed Mode - (50kHz to 100kHz sample rates)					
Passband					
	to -0.1 dB corner	0	-	0.4426	Fs
	to -3 dB corner	0	-	0.4984	Fs
Frequency Response 10 Hz to 20 kHz		0	-	+0.11	dB
StopBand		0.577	-	-	Fs
StopBand Attenuation	(Note 3)	55	-	-	dB
Group Delay		-	4/Fs	-	s
Passband Group Delay Deviation	0 - 40 kHz	-	±1.39/Fs	-	s
	0 - 20 kHz	-	±0.23/Fs	-	s

Notes: 2. Referenced to a 1 kHz, full-scale sine wave.

3. For Single-Speed Mode, the measurement bandwidth is 0.5465 Fs to 3 Fs.
   For Double-Speed Mode, the measurement bandwidth is 0.577 Fs to 1.4 Fs.

4. De-emphasis is only available in Single-Speed Mode.

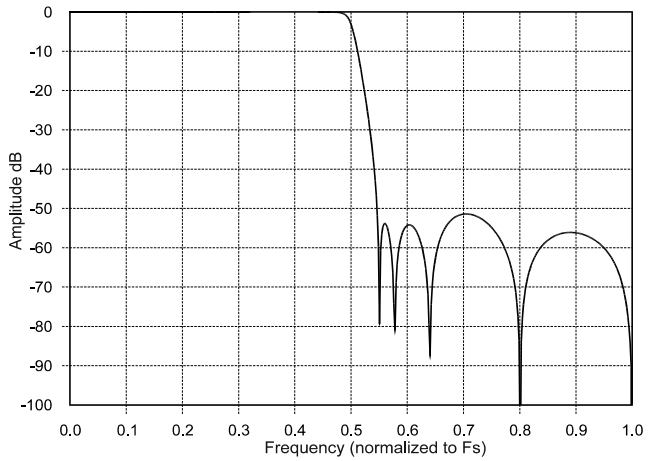


Figure 11. Single-Speed Stopband Rejection

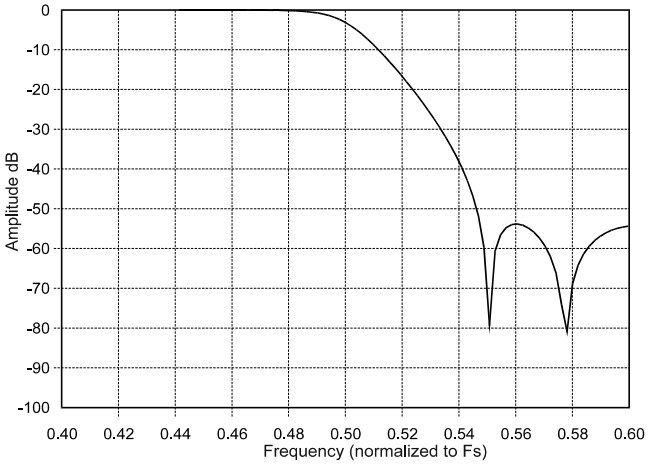


Figure 12. Single-Speed Transition Band

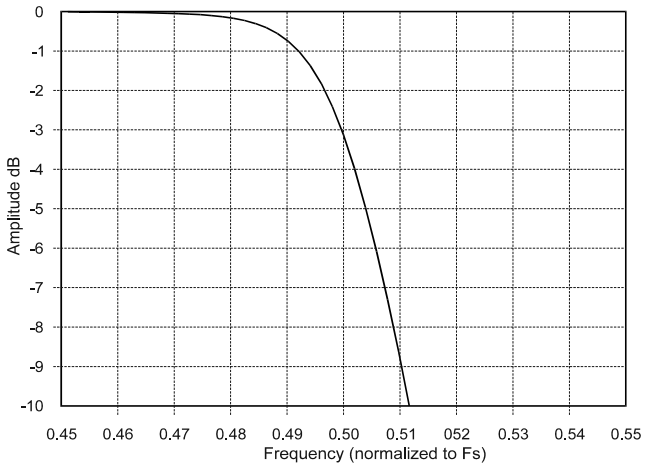


Figure 13. Single-Speed Transition Band (Detail)

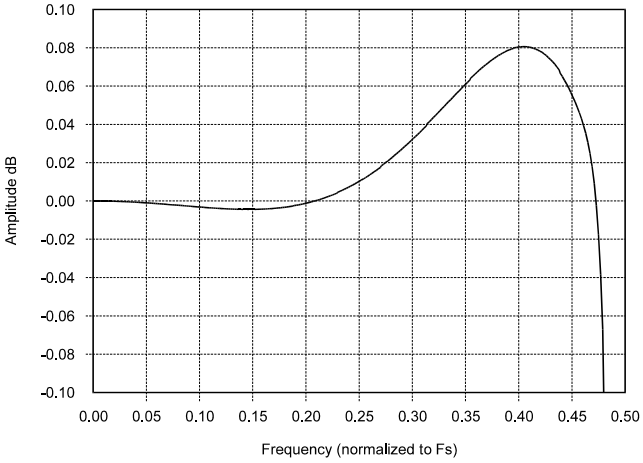


Figure 14. Single-Speed Passband Ripple

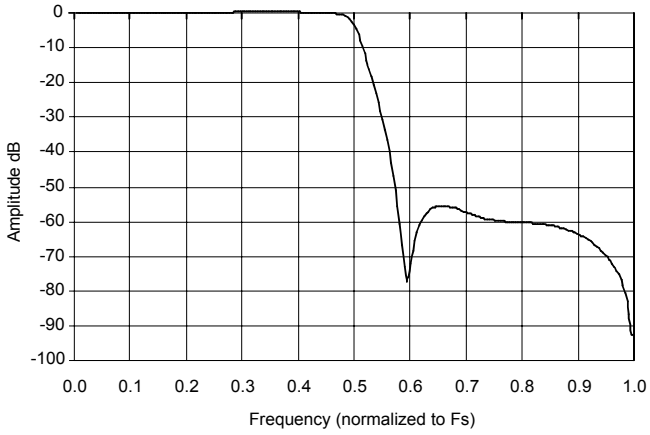


Figure 15. Double-Speed Stopband Rejection

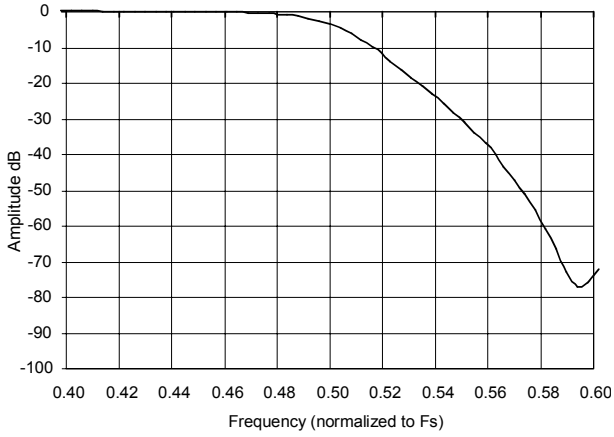


Figure 16. Double-Speed Transition Band

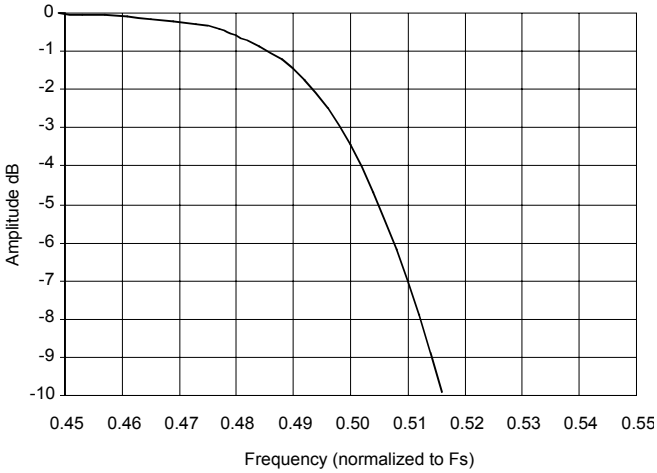


Figure 17. Double-Speed Transition Band (Detail)

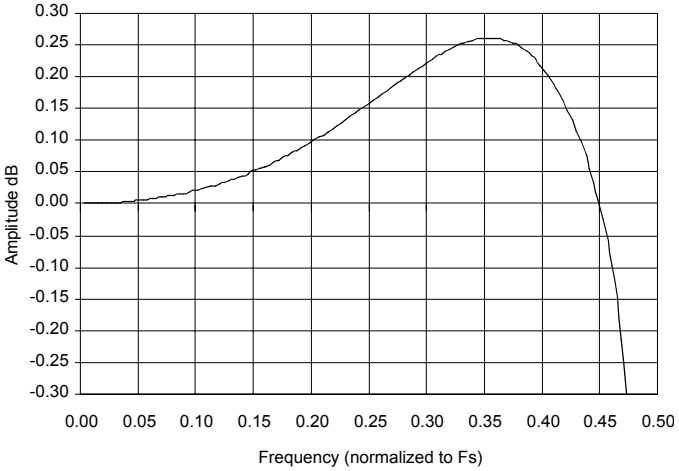


Figure 18. Double-Speed Passband Ripple

SWITCHING SPECIFICATIONS - SERIAL AUDIO INTERFACE (Inputs: Logic "0" = GND, Logic "1" = VL.)

Parameters		Symbol	Min	Max	Units
External SCLK Mode					
MCLK Frequency			1.024	51.2	MHz
MCLK Duty Cycle			45	55	%
Input Sample Rate	Single-Speed Mode Double-Speed Mode	Fs Fs	2 50	50 100	kHz kHz
LRCK Duty Cycle			40	60	%
SCLK Pulse Width Low		t_{sclkl}	20	-	ns
SCLK Pulse Width High		t_{sclkh}	20	-	ns
SCLK Period		t_{sclkw}	$\frac{2}{MCLK}$	-	s
SCLK Frequency			-	$\frac{MCLK}{2}$	Hz
SCLK Frequency	(Note 10)		-	$\frac{MCLK}{4}$	Hz
SCLK rising to LRCK edge delay		t_{slrd}	20	-	ns
SCLK rising to LRCK edge setup time		t_{slrs}	20	-	ns
SDATA valid to SCLK rising setup time		t_{sdlrs}	20	-	ns
SCLK rising to SDATA hold time		t_{sdh}	20	-	ns

Notes: 5. This serial clock is required only in Control Port Mode when the MCLK Divide bit is enabled.

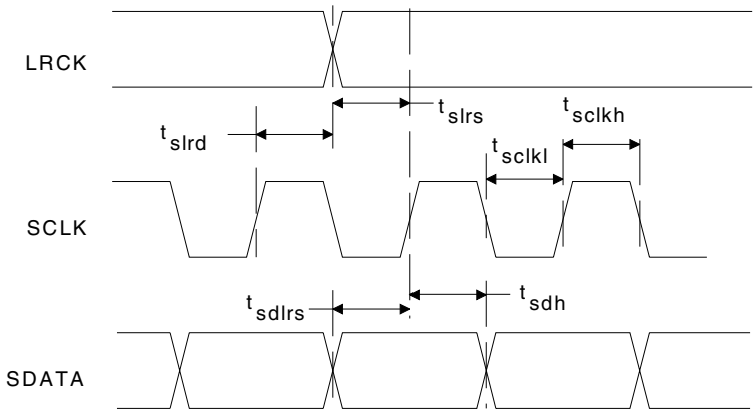


Figure 19. External Se- rial Mode Input Timing

SWITCHING CHARACTERISTICS - INTERNAL SERIAL CLOCK (Inputs: Logic "0" = GND, Logic "1" = VL.)

Parameters		Symbol	Min	Typ	Max	Units
Internal SCLK Mode						
LRCK Duty Cycle	(Note 6)		-	50	-	%
SCLK Period		t_{sclkw}	$\frac{1}{SCLK}$	-	-	s
SCLK rising to LRCK edge		t_{sclkr}	-	$\frac{tsclkw}{2}$	-	s
SDATA valid to SCLK rising setup time		t_{sdlrs}	$\frac{1}{(512)Fs} + 10$	-	-	ns
SCLK rising to SDATA hold time	Single-Speed Mode	t_{sdh}	$\frac{1}{(512)Fs} + 15$	-	-	ns
	Double-Speed Mode	t_{sdh}	$\frac{1}{(384)Fs} + 15$	-	-	ns

Notes: 6. In Internal SCLK Mode, the LRCK duty cycle must be 50% +/– 1/2 MCLK Period.

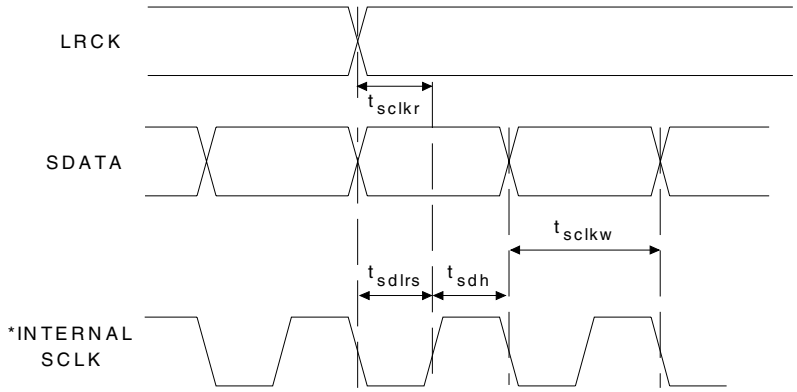


Figure 20. Internal Serial Mode Input Timing

*The SCLK pulses shown are internal to the CS43L43.

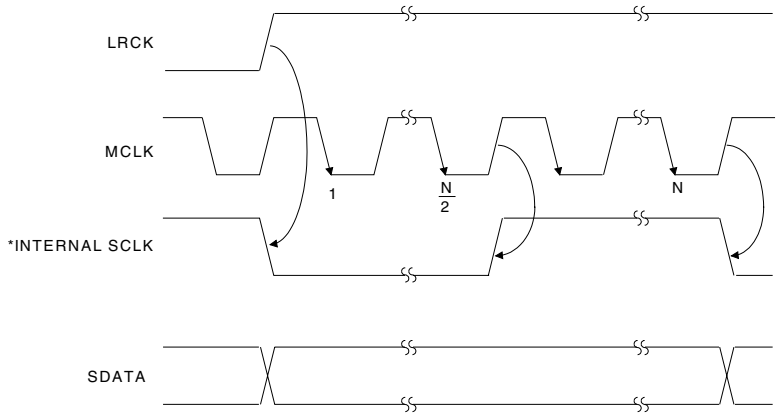


Figure 21. Internal Serial Clock Generation

* The SCLK pulses shown are internal to the CS43L43.
N equals MCLK divided by SCLK

SWITCHING SPECIFICATIONS - CONTROL PORT INTERFACE

(Inputs: Logic "0" = GND, Logic "1" = VL.)

Parameter	Symbol	Min	Max	Unit
I²C Mode				
SCL Clock Frequency	f_{scl}	-	100	kHz
$\overline{RST}$ Rising Edge to Start	t_{irs}	$\frac{1}{(2)Fs}$	-	s
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 7)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of SCL	t_{rc}	-	25	ns
Fall Time of SCL	t_{fc}	-	25	ns
Rise Time SDA	t_{rd}	-	1	µs
Fall Time of SDA	t_{fd}	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs

7. Data must be held for sufficient time to bridge the transition time, t_{fc}, of SCL.

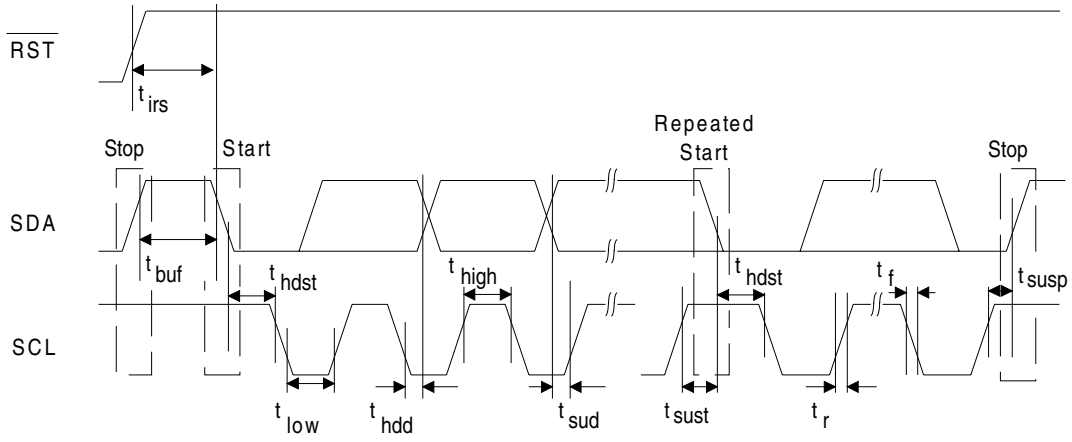


Figure 22. Control Port Timing - I²C Mode

DC ELECTRICAL CHARACTERISTICS (GND = 0V; all voltages with respect to GND.)

Parameters		Symbol	Min	Typ	Max	Units
Normal Operation (Note 8)						
Power Supply Current	VA=1.8V	I_A	-	7.3	-	mA
	VA_HP=1.8V	I_{A_HP}	-	1.5	-	mA
	VL=1.8V	I_{D_L}	-	4	-	µA
Power Supply Current	VA=3.0V	I_A	-	10.5	-	mA
	VA_HP=3.0V	I_{A_HP}	-	1.5	-	mA
	VL=3.0V	I_{D_L}	-	9.3	-	µA
Total Power Dissipation	All Supplies=1.8V		-	16	20	mW
	All Supplies=3.0V		-	36	50	mW
Power-down Mode (Note 9)						
Power Supply Current	VA=1.8V	I_A	-	2.0	-	µA
	VA_HP=1.8V	I_{A_HP}	-	9.3	-	µA
	VL=1.8V	I_{D_L}	-	2.2	-	µA
Power Supply Current	VA=3.0V	I_A	-	3.4	-	µA
	VA_HP=3.0V	I_{A_HP}	-	9.8	-	µA
	VL=3.0V	I_{D_L}	-	7.6	-	µA
Total Power Dissipation	All Supplies=1.8V		-	24.3	-	µW
	All Supplies=3.0V		-	62.4	-	µW
All Modes of Operation						
Power Supply Rejection Ratio (Note 10)	1 kHz	PSRR	-	60	-	dB
	60 Hz		-	40	-	dB
V_Q Nominal Voltage		V_{Q_HP}	-	0.5•VA	-	V
Output Impedance			-	250	-	kΩ
Maximum allowable DC current source/sink			-	0.01	-	mA
Filt+ Nominal Voltage			-	VA	-	V
Output Impedance			-	250	-	kΩ
Maximum allowable DC current source/sink			-	0.01	-	mA

DIGITAL INPUT CHARACTERISTICS AND SPECIFICATIONS (GND = 0V; all voltages with respect to GND.)

Parameters	Symbol	Min	Typ	Max	Units
Input Leakage Current	I_{in}	-	-	±10	µA
Input Capacitance		-	8	-	pF
High-Level Input Voltage	V_{IH}	0.7 x VL	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.3 x VL	V

THERMAL CHARACTERISTICS AND SPECIFICATIONS

Parameters		Symbol	Min	Typ	Max	Units
Package Thermal Resistance		θ_{JA}	-	75	-	°C/Watt
Ambient Operating Temperature	(Power Applied)	T_A	-10	-	+70	°C

RECOMMENDED OPERATING CHARACTERISTICS (GND = 0V; all voltages with respect to GND.)

Parameters	Symbol	Min	Typ	Max	Units
DC Power Supply					
Analog	VA	1.7	1.8	1.9	V
		2.25	2.5	2.75	V
		3.0	3.3	3.6	V
Headphone (Note 11)	VA_HP	0.9	-	3.6	V
Logic	VL	1.7	1.8	1.9	V
		2.25	2.5	2.75	V
		3.0	3.3	3.6	V

ABSOLUTE MAXIMUM RATINGS (GND = 0 V; all voltages with respect to AGND. Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.)

Parameters	Symbol	Min	Max	Units
DC Power Supplies: Positive Analog	VA	-0.3	4.0	V
Headphone	VA_HP	-0.3	4.0	V
Digital I/O	VL	-0.3	4.0	V
Input Current, Any Pin Except Supplies	I_{in}	-	±10	mA
Digital Input Voltage	V_{IND}	-0.3	VL + 0.4	V
Ambient Operating Temperature (power applied)	T_A	-55	125	°C
Storage Temperature	T_{stg}	-65	150	°C

Notes:
8. Normal operation is defined as $\overline{RST}$ = HI with a 997 Hz, 0dBFS input sampled at F_s = 48kHz, and open outputs, unless otherwise stated.
9. Power Down Mode is defined as $\overline{RST}$ = LO with all clocks and data lines held static.
10. Valid with the recommended capacitor values on FILT+ and VQ_HP as shown in Figure 1. Increasing the capacitance will also increase the PSRR. NOTE: Care should be taken when selecting capacitor type, as any leakage current in excess of 1.0 µA will cause degradation in analog performance.
11. To prevent clipping the outputs, VA_HP_{MIN} is limited by the Full-Scale Output Voltage V_{FS_HP}, where VA_HP must be 200 mV greater than V_{FS_HP}. However, if distortion is not a concern, VA_HP may be as low as 0.9 V at any time.

7.0 PARAMETER DEFINITIONS

Total Harmonic Distortion + Noise (THD+N)

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10Hz to 20kHz), including distortion components. Expressed in decibels.

Dynamic Range

The ratio of the full scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with all zeros to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full scale analog output for a full scale digital input.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

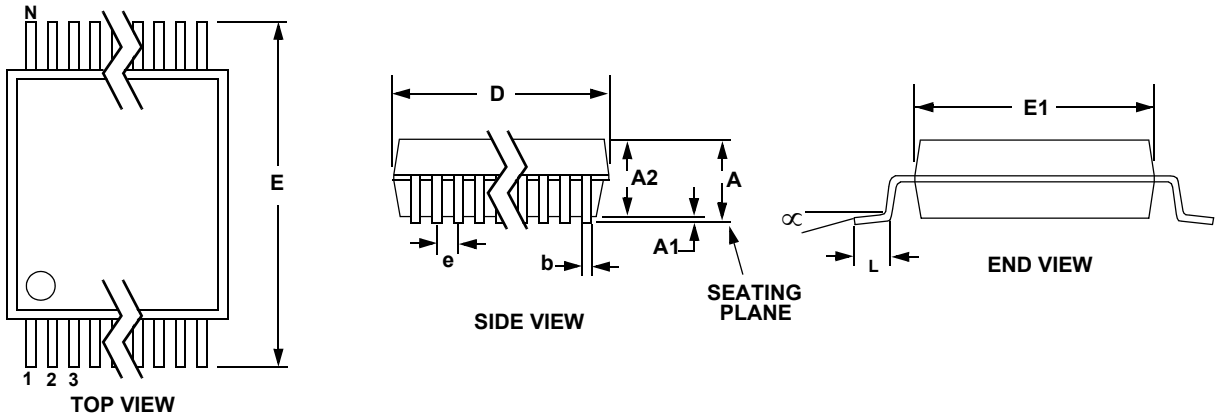
8.0 REFERENCES

1) CDB43L43 Evaluation Board Datasheet

2) "The I^2C-Bus Specification: Version 2.1" Philips Semiconductors, January 2000. http://www.semiconductors.philips.com

9.0 PACKAGE DIMENSIONS

16L TSSOP PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.043	--	--	1.10	
A1	0.002	--	0.006	0.05	--	0.15	
A2	0.033	0.035	0.037	0.85	0.90	0.95	
b	0.008	--	0.012	0.19	--	0.30	2,3
D	--	0.197	--	--	5.00	--	1
E	--	0.252	--	--	6.40	--	
E1	0.169	0.173	0.177	4.30	4.40	4.50	1
e	--	0.026	--	--	0.65	--	
L	0.020	0.024	0.028	0.50	0.60	0.70	
∝	0°	--	8°	0°	--	8°	

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Notes:
1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.
2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.
3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.