

Structure Silicon Monolithic Integrated Circuit

Product Name Audio Management for cellular phone

Type **BU7831KN**

Features Voice or audio input/output selector (6input and 5output)
Include multi mixing function

○Absolute Maximum Ratings (Ta=25 °C)

Parameter	Symbol	Rating	Unit	Condition
Supply Voltage	VDD	-0.3 to 4.5	V	
Input Voltage	VIN	VSS-0.3 to VDD+0.3	V	
Input Current	IIN	-1 to 1	mA	
Power Dissipation	Pd	530(*1)	mW	
Compensation Temperature Range	Tstg	-55 to 125	°C	
Operation Temperature Range	Topr	-20 to 85	°C	

(*1) To use at a temperature higher than Ta=25 °C, delete 5.3mW/°C
This value is the package on ROHM standard board.

○Recommended operating conditions (Ta=-20 to 85 °C)

Parameter	Symbol	Rating			Unit	Condition
		Min.	Typ.	Max.		
Supply Voltage	VDD	2.5	3.0	3.3	V	

This product isn't designed to protect itself against radioactive rays.

Status of this document

The Japanese version of this document is the formal specification.
A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document, formal version takes priority.

Application example

The product described in this specification is designed to be used with ordinary electronic equipment or devices (such as audio-visual equipment, office-automation equipment, communications devices, electrical appliances, and electronic toys).
Should you intend to use this product with equipment or devices which require an extremely high level of reliability and the malfunction of which would directly endanger human life (such as medical instruments, transportation equipment, aerospace machinery, nuclear-reactor controllers, fuel controllers and other safety devices), please be sure to consult with our sales representative in advance.

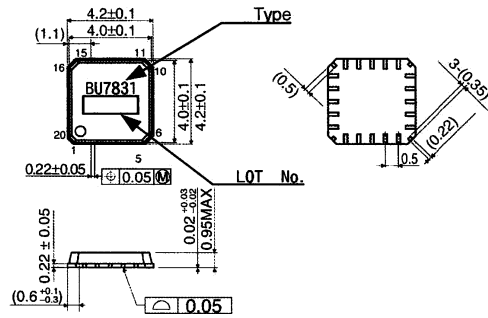
○Electrical Characteristics

Unless otherwise specified, Ta=25 °C, VDD= 3.0V, f=1kHz, VIN=-10dBV, BW=10Hz to 20kHz

Parameters	Symbol	Specification			Unit	Conditions
		Min.	Typ.	Max.		
Circuit Current						
Stand-by current	Istb	-	-	3	μA	stand-by mode
Operation current 1	Idd1	-	0.26	0.42	mA	BIAS part, No signal
Operation current 2	Idd2	-	2.3	3.7	mA	Headphone AMP part, No signal (*1)
ATT1L, R						
Number of volume steps	Stg1	-	2	-	dB	
ATT2L, R						
Number of volume steps	Stg2	-	6	-	dB	
ATT3L, R						
Number of volume steps	Stg3	-	6	-	dB	
ATT4L, R						
Number of volume steps	Stg4	-	2	-	dB	
Muting level	Mut4	-	-95	-80	dB	At mute setting
ATT5						
Number of volume steps	Stg5	-	2	-	dB	
Muting level	Mut5	-	-95	-80	dB	At mute setting
ATT6L, R						
Number of volume steps	Stg6	-	2	-	dB	
Muting level	Mut6	-	-95	-80	dB	At mute setting
Headphone AMP						
Total Harmonic Distortion 1	THDhp1	-	0.05	0.5	%	VO=-10dBV, VDD=3.0V 20kHz LPF
Output Power 1	PO1	-	10	-	mW	THD=10%, RL=16Ω, VDD=3.0V
Output Noise Voltage	VNO	-	-94	-80	dBV	JIS A weighting
SPO						
Maximum Output Level 1	VOMAX1	2.0	-	-	V _{P-P}	1kHz, 10kΩLoad, THD≤1%, VDD=3.0V
EXTO						
Maximum Output Level 2	VOMAX2	2.0	-	-	V _{P-P}	1kHz, 600ΩLoad, THD≤1% VDD=3.0V
Digital Input Operation DC						
Digital Input Voltage "L"	VIL	-	-	0.7	V	
Digital Input Voltage "H"	VIH	2.1	-	-	V	
Input Leak Current 1	IIN	-	-	±2	μA	0V, 3V Force

(*1) The Path from ST1R, ST1L to HPR, HPL (excluding Idd1)

External dimensions



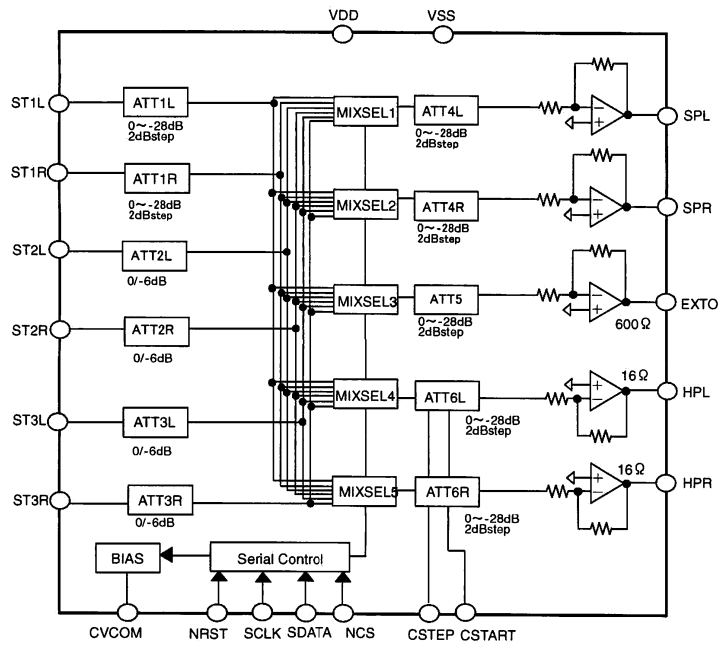
Note) Un-recommended installation at enclosed area with a dotted line.

VQFN20 (Unit : mm)

Terminals

PIN	PIN Name	PIN	PIN Name
1	SCLK	11	CVCOM
2	SDATA	12	CSTEP
3	NCS	13	HPR
4	NRST	14	VSS
5	ST1R	15	VDD
6	ST1L	16	HPL
7	ST2R	17	CSTART
8	ST2L	18	EXTO
9	ST3R	19	SPR
10	ST3L	20	SPL

Block diagram



○Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Power supply and GND line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. Pay attention to the interference by common impedance of layout pattern when there are plural power supplies and GND lines. Especially, when there are GND pattern for small signal and GND pattern for large current included the external circuits, please separate each GND pattern. Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use a capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(3) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(4) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(5) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(6) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(7) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(8) Other cautions on use

Please consult supplementary documents such as technical notebook, function manual and application notebook of this LSI.

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